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Pages 1 to 45

INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS 4-BIT LATCH/4-TO-16-LINE DECODER,

BASED ON TYPE 4515B

ESA/SCC Detail Specification No. 9205/011

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 3	May 1993		
Revision 'A'	November 1994		
Revision 'B'	April 2001		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 2 and incorporates all modifications defined in Revision 'A' to Issue 2 and the following DCR's:-		
		Cover Page		None
		DCN		None
		Para. 1.10	Last sentence rewritten to include ESD Class and Minimum Critical Path Failure Voltage	23385
		Table 1(a)	Table amended	22398
			Lead Material and/or Finish amended	23465
		Table 1(b)	No. 9, package soldering temperatures changed	22314
			Notes - Note 6 added	22314
		Figure 2(a)	Table corrected	23247/ 23270
		Figure 2(b)	"CKT A" deleted from Title	22398
		Figure 2(c)	Figure deleted in toto	22398
		Figure 2(d)	Title amended to "2(c)"	22398
			Table corrected	23247
		Notes to Figures	In Title and Note 1, 2(d) amended to "2(c)"	22398
		Figure 3(b)	"(See Notes)" deleted from Title	23520
			Truth Table and Notes deleted and new Truth Table and Notes added	23520
		Figure 3(c)	In Circuit A, entry deleted.	23520
			Drawing from Figure 3(d) Circuit A added and output logic coding corrected	23520
		Figure 3(d)	Drawing transferred to Figure 3(c) Circuit A and new drawing added	23520
		Figures 3(c), (d), (e)	Circuit A heading and Circuit B heading and drawing deleted	22398
		Para. 4.2.2	Deviation deleted, "None." added	22360/ 21048
		Para. 4.2.4	Deviation deleted, "None." added	22919
		Para. 4.2.5	Deviation deleted, "None." added	22919
		Para. 4.4.2	Material Type and Finishes amended	23465
		Para. 4.5.2	Third sentence amended to read "...2(c)"	22398
		Tables 2, 3(a), (b)	Where applicable, Conditions format standardised	23520
			Nos. 1 and 2, in Conditions, "dc" added to voltage	23520
			Nos. 31 to 36, 63 to 78, 79 to 94, new Conditions added	23520
			Nos. 95 to 110, 111 to 126, Note No. corrected to "4"	23520
		Table 2	Nos. 131 to 136, Limits column amended	22398
			Nos. 137 to 142, "CKT A" deleted from first measurement and "CKT B" entry deleted in toto	22398
			Nos. 149 and 151, Characteristics corrected	23520
			Nos. 149, 151, 153, 154, Conditions corrected	23520
			Nos. 150 and 152, Characteristics corrected	23520
			, Conditions completed	23520
		Figure 4(b)	In Note 1, Ground amended to "V_{SS}"	23520
			Note sequence reversed	23520
		Figure 4(e)	Note 2 corrected	23520
		Figures 4(e), (g)	Input to "V_{DD}" marked "Strobe Input" added	23520
			Input to "V_{SS}" marked "Inhibit Input" added	23520

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	CHANGE Reference	Item	Approved DCR No.
		Figures 4(g), (h)	: Outputs circuits amended	23076
		Figures 4(i), (j)	: "Strobe Input" added to Grounded connection	23520
		Figure 4(j)	: "V_{THN}" corrected to "V_{THP}"	23520
		Figures 4(l), (n)	: Circuit A heading and Circuit B heading and drawing deleted	22398
		Figure 4(n)	: Existing Waveforms deleted and new Waveforms added	23520
		Tables 5(a), (b)	: Titles amended	23162
		Table 5(a)	: No. 2 deleted and all subsequent tests renumbered	23520
			: No. 3, (Now 2), Pin "8" added to Characteristics and Condition amended to "Open"	23520
		Table 5(b)	: No. 2, Pin "8" added to Characteristics and Condition amended to "Open"	23520
			: No. 3 deleted and all subsequent tests renumbered	23520
			: Nos. 4 and 5 (Now 3 and 4) reversed in sequence	23520
		Table 5(c)	: No. 5, Condition corrected to "V_{GEN2}"	23520
			: No. 6, Condition corrected to "V_{GEN1}"	23520
			: Nos. 8 and 9, combined as No. 8 and all subsequent tests renumbered	23520
			: No. 10 (Now 9), Pin Number corrected to "24"	23520
			: No. 11 (Now 10), Pin Number corrected to "12"	23520
		Figures 5(a), (b)	: Titles amended	23162
			: Resistors added to inputs	23520
			: Outputs made "Open"	23520
		Figure 5(c)	: "$V_{GEN/2}$" corrected to "V_{GEN2}"	23520
			: "V_{GEN}" corrected to "V_{GEN1}"	23520
			: Resistors added to Pins 2 and 3	23520
		Paras. 4.8.4 and 4.8.5	: Reference to Table and Figure amended to '5(c)"	23520
		Table 6	: Nos. 63 to 78, "N-Channel" added to Characteristics	23520
'A'	Nov. '94	P1. Cover Page		None
		P2A. DCN		None
		P6. Table 1(a)	: Lead Material and/or Finish amended	221049
		P16. Para. 4.3.2	: Weights amended	23539
		Para. 4.4.2	: Lead Finish, Types amended	221049
'B'	Apr. '01	P1. Cover Page	: Page count increased 1	221602
		P2A. DCN		None
		P4. T of C	: Appendices entry amended	221602
		P5. Para. 1.3	: New sentence added	221602
		P6. Table 1(a)	: Variants 08 and 09 added	221562
		Table 1(b)	: No. 8, Maximum temperature amended	221602
		P9. Figure 2(c)	: In the drawing, Pin No. 28 location corrected	221550
		P10. Notes to Figures	: Title amended	221562
			: Note 1 rewritten	221562
		P10A. Figure 2(d)	: New page added	221562
		P11. Figure 3(a)	: Left-hand drawing Title amended	221562
			: "SO" added to comparison Titles	221562
		P16. Para. 4.3.2	: SO package added to the text	221562
		Para. 4.4.2	: SO package added to the text	221562
		Para. 4.5.2	: SO package added to the text	221562
		P43. Para. 4.8.6	: Last sentence deleted, new text added	221602
		P45. Appendix 'A'	: Appendix added	221602

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TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, CMOS 4-Bit Latch/4-to-16-Line Decoder, having fully buffered outputs, based on Type 4515B. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESA/SCC Generic Specification.

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. These components are Catagorised as Class 1 with a Minimum Critical Path Failure Voltage of 400 Volts.

1.11 INPUT PROTECTION NETWORK

Double diode protection shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	FLAT	2(a)	G2 or G8
02	FLAT	2(a)	G4
03	D.I.L.	2(b)	G2 or G8
04	D.I.L.	2(b)	G4
07	CHIP CARRIER	2(c)	2
08	SO CERAMIC	2(d)	G2
09	SO CERAMIC	2(d)	G4

TABLE 1(b) - MAXIMUM RATINGS

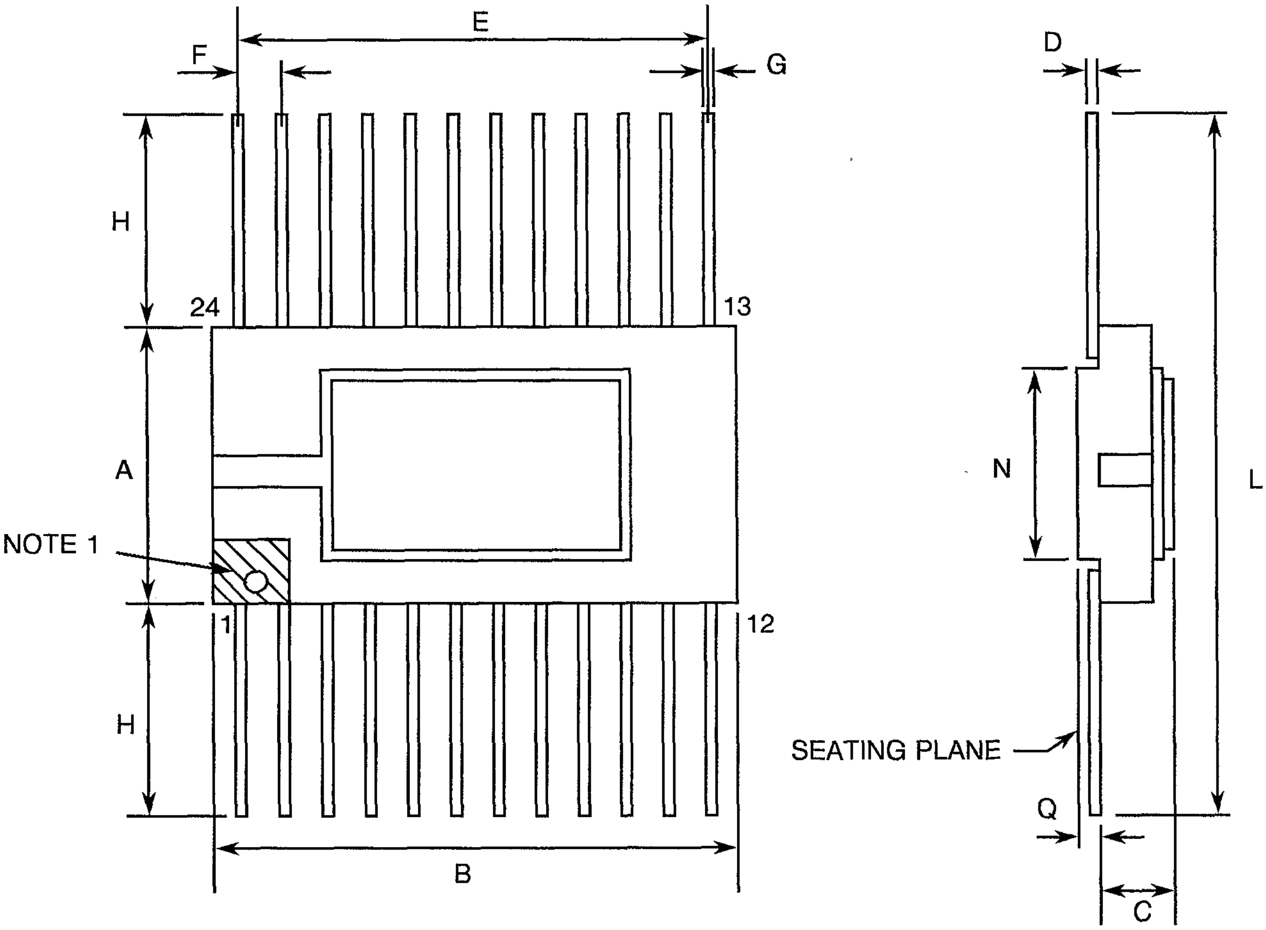
NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{DD}	-0.5 to +18	V	Note 1
2	Input Voltage	V_{IN}	-0.5 to V_{DD} + 0.5	V	Note 2 Power on
3	D.C. Input Current	$\pm I_{IN}$	10	mA	-
4	D.C. Output Current	$\pm I_O$	10	mA	Note 3
5	Device Dissipation	P_D	200	mWdc	Per Package
6	Output Dissipation	P_{DSO}	100	mWdc	Note 4
7	Operating Temperature Range	T_{op}	-55 to +125	°C	-
8	Storage Temperature Range	T_{stg}	-65 to +150	°C	-
9	Soldering Temperature For FP and DIP For CCP	T_{sol}	 +300 +245	°C	 Note 5 Note 6

NOTES

1. Device is functional from +3V to +15V with reference to V_{SS}.
2. V_{DD} + 0.5V should not exceed +18V.
3. The maximum output current of any single output.
4. The maximum power dissipation of any single output.
5. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
6. Duration 30 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 24-PIN

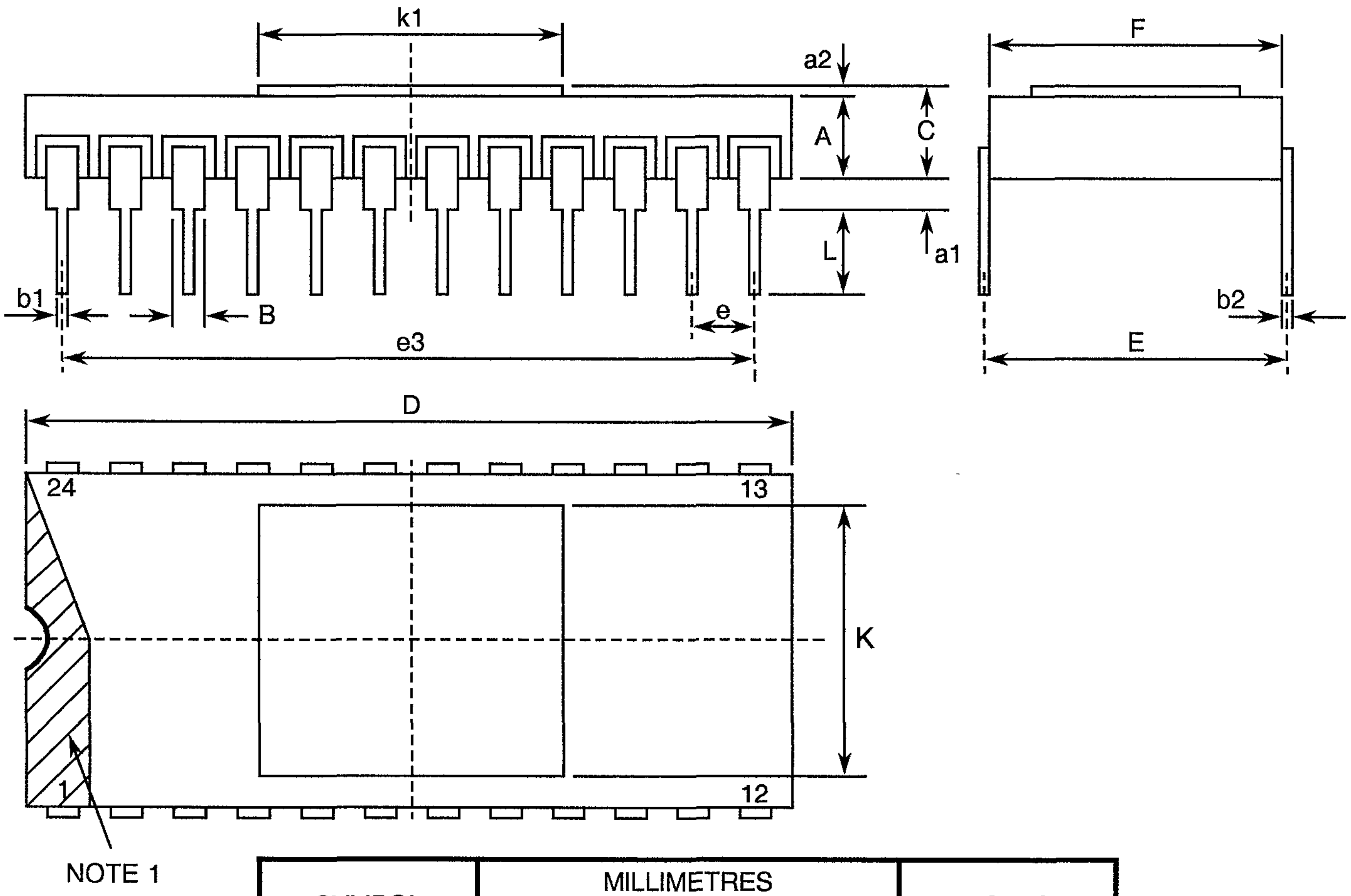


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	10.70	11.30	
B	15.30	15.70	
C	1.45	1.90	
D	0.23	0.30	
E	13.84	14.10	
F	1.22	1.32	4
G	0.45	0.55	3
H	7.25	8.25	
L	25.00	28.00	
N	7.00	TYPICAL	
Q	0.45	0.55	2

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 24-PIN

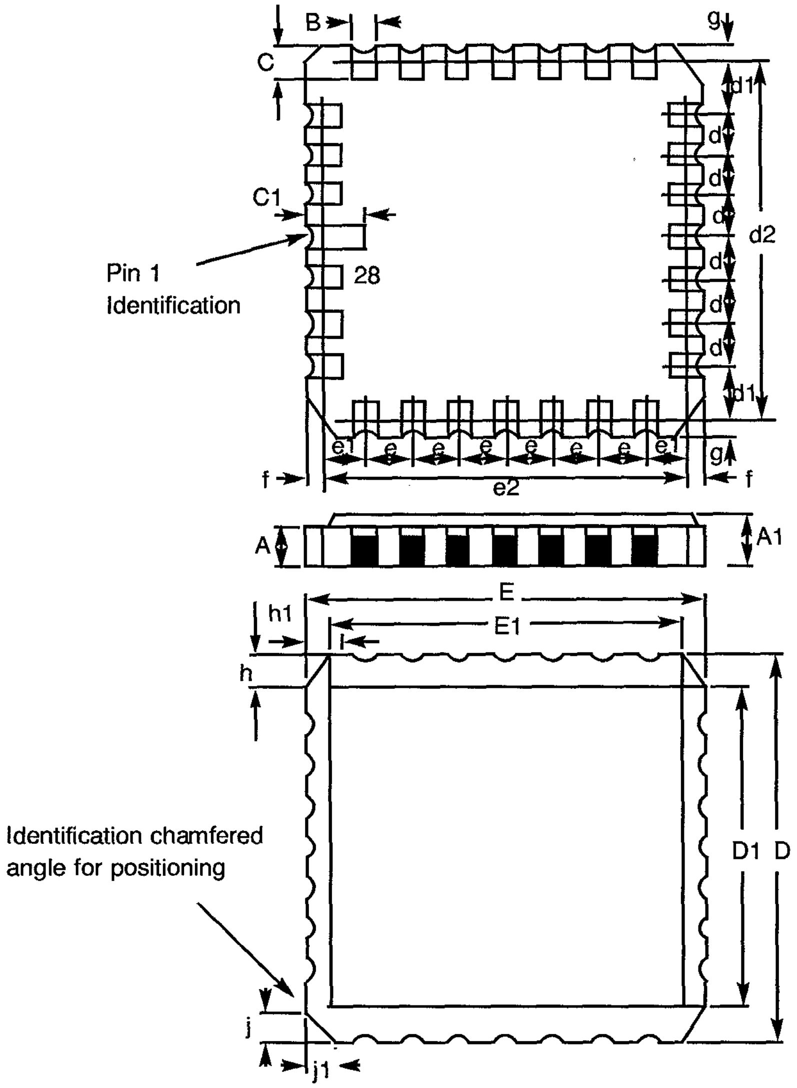


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.931	2.387	
a1	1.016	1.524	2
a2	0.274	0.340	
B	1.274	TYPICAL	3
b1	0.407	0.507	3
b2	0.229	0.304	3
C	2.205	2.727	
D	30.176	30.784	
E	14.986	15.494	
e	2.413	2.667	4
e3	27.813	28.067	
F	14.859	15.367	
L	3.0	3.8	
K	12.6	13.0	
k1	12.6	13.0	

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - CHIP CARRIER - 28-TERMINAL



DIMENSIONS	MILLIMETRES		NOTES
	MIN	MAX	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	3
C	1.06	1.47	3
C_1	1.91	2.41	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27	TYPICAL	4
d2	7.62	TYPICAL	
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27	TYPICAL	4
e2	7.62	TYPICAL	
f, g	-	0.76	
h, h1	1.01	TYPICAL	6
j, j1	0.51	TYPICAL	5

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(d) INCLUSIVE

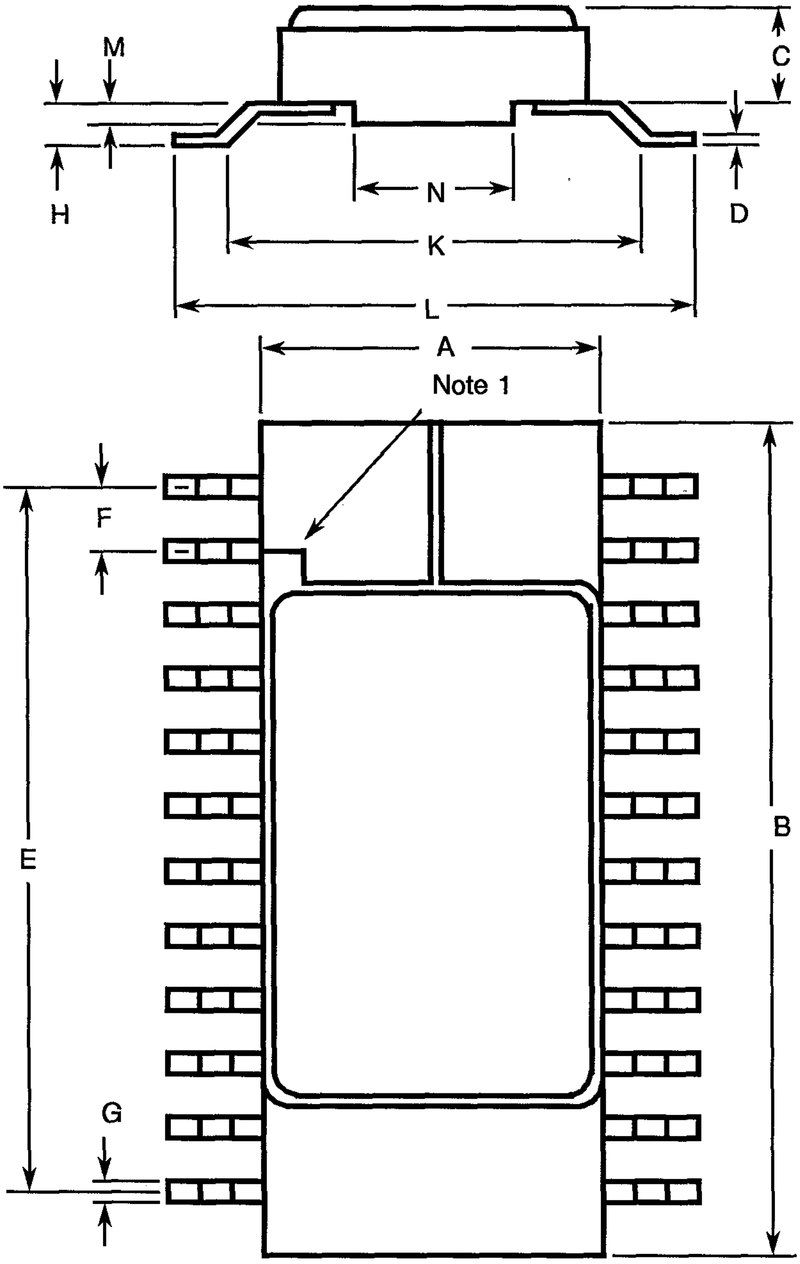
1. Index area; a notch, letter, metallised tab or dot shall be located adjacent to Pin 1 or 2 and shall be within the shaded area shown.

   For chip carrier packages the index shall be as defined in Figure 2(c).

   For SO packages, a dot shall also be located adjacent to Pin 1 on the bottom of the package.
2. The dimension shall be measured from the seating plane to the base plane.
3. All leads or terminals.
4. 24 pin packages : 22 spaces
   28 terminal packages : 16 spaces
5. Index corner only.
6. Three non-index corners.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(d) - SMALL OUTLINE CERAMIC PACKAGE, 24-PIN

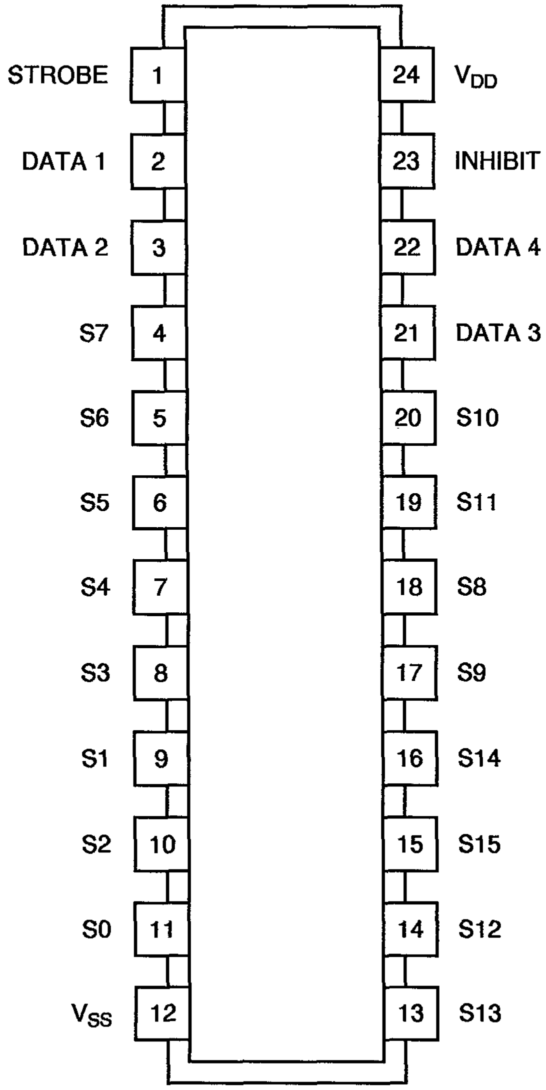


SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	7.30	7.60	
B	15.20	15.60	
C	1.58	1.88	
D	0.17	0.23	3
E	13.82	14.12	
F	1.27 TYPICAL		4
G	0.37	0.47	3
H	0.60	0.90	3
K	9.00 TYPICAL		
L	10	10.65	
M	0.55 TYPICAL		
N	4.31 TYPICAL		

NOTES: See Page 10.

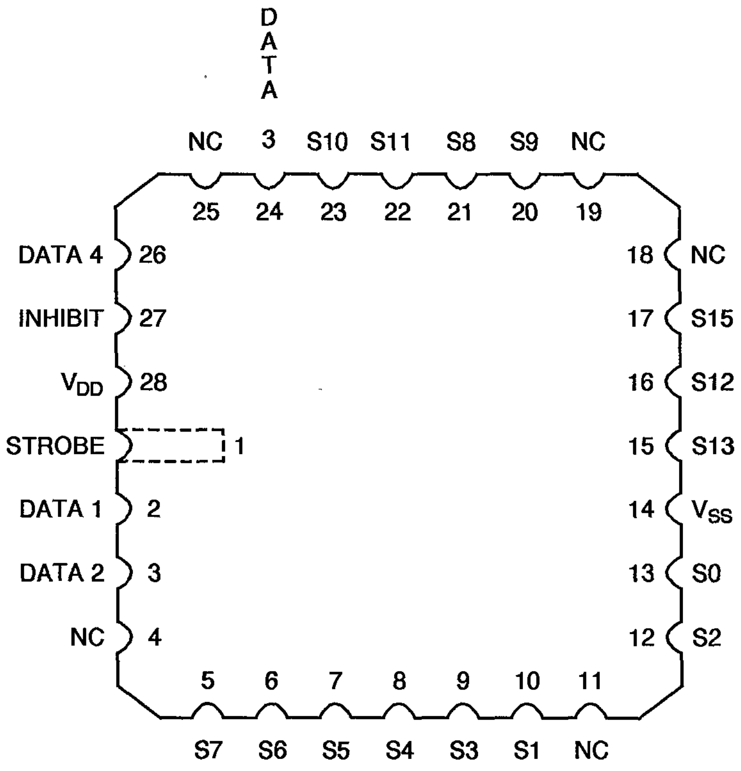
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE, SO AND FLAT PACKAGES



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE, SO AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
CHIP CARRIER PIN OUTS	1	2	3	5	6	7	8	9	10	12	13	14	15	16	17	19	20	21	22	23	24	26	27	28

FIGURE 3(b) - TRUTH TABLE

INHIBIT	DATA INPUTS				SELECTED OUTPUT = L (STROBE = H)
	4	3	2	1	
L	L	L	L	L	S0
L	L	L	L	H	S1
L	L	L	H	L	S2
L	L	L	H	H	S3
L	L	H	L	L	S4
L	L	H	L	H	S5
L	L	H	H	L	S6
L	L	H	H	H	S7
L	H	L	L	L	S8
L	H	L	L	H	S9
L	H	L	H	L	S10
L	H	L	H	H	S11
L	H	H	L	L	S12
L	H	H	L	H	S13
L	H	H	H	L	S14
L	H	H	H	H	S15
H	X	X	X	X	ALL OUTPUTS = H

NOTES

1. Logic Level Definitions: L = Low Level, H = High Level, X = Don't Care.

FIGURE 3(c) - CIRCUIT SCHEMATIC

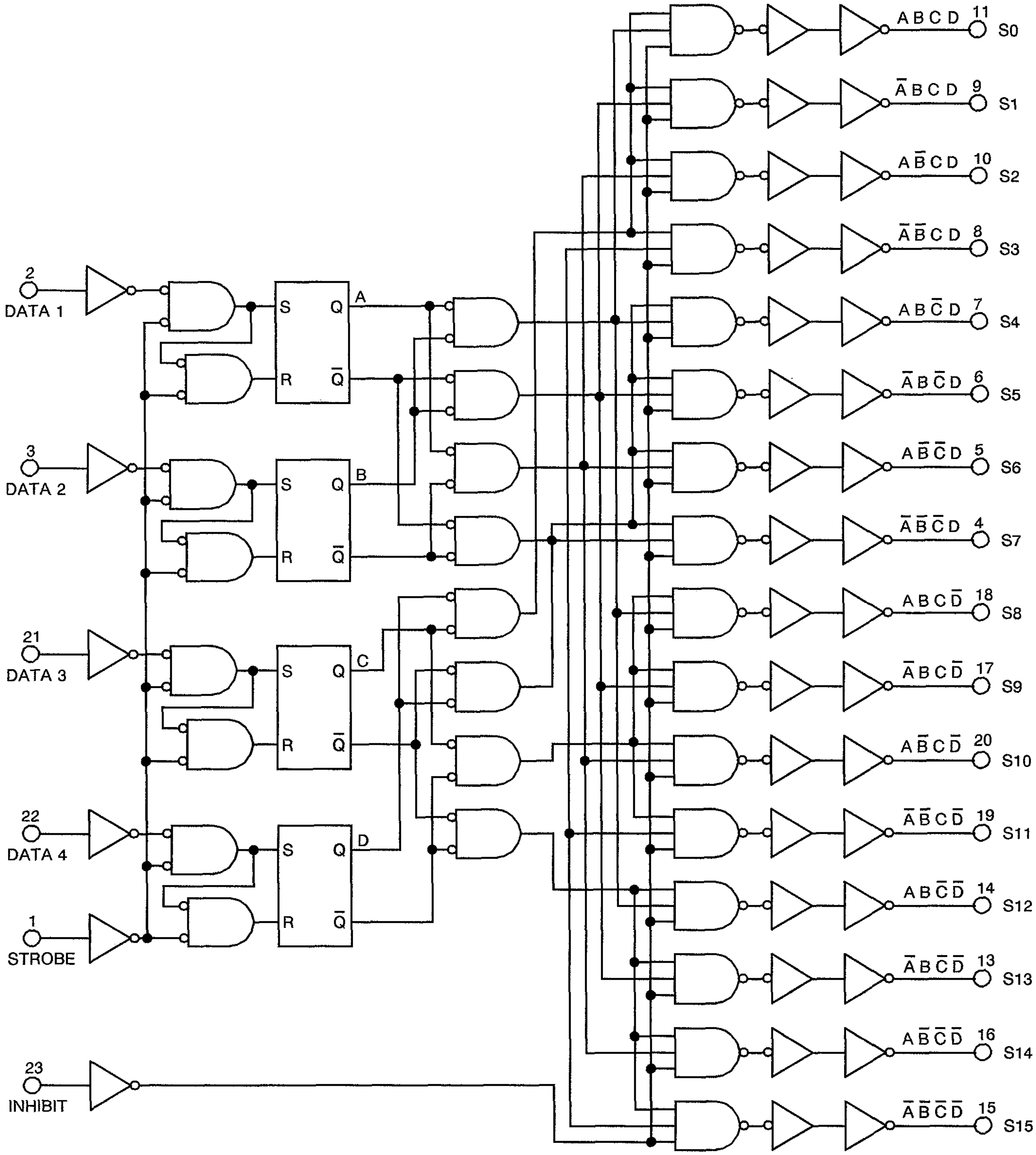


FIGURE 3(d) - FUNCTIONAL DIAGRAM

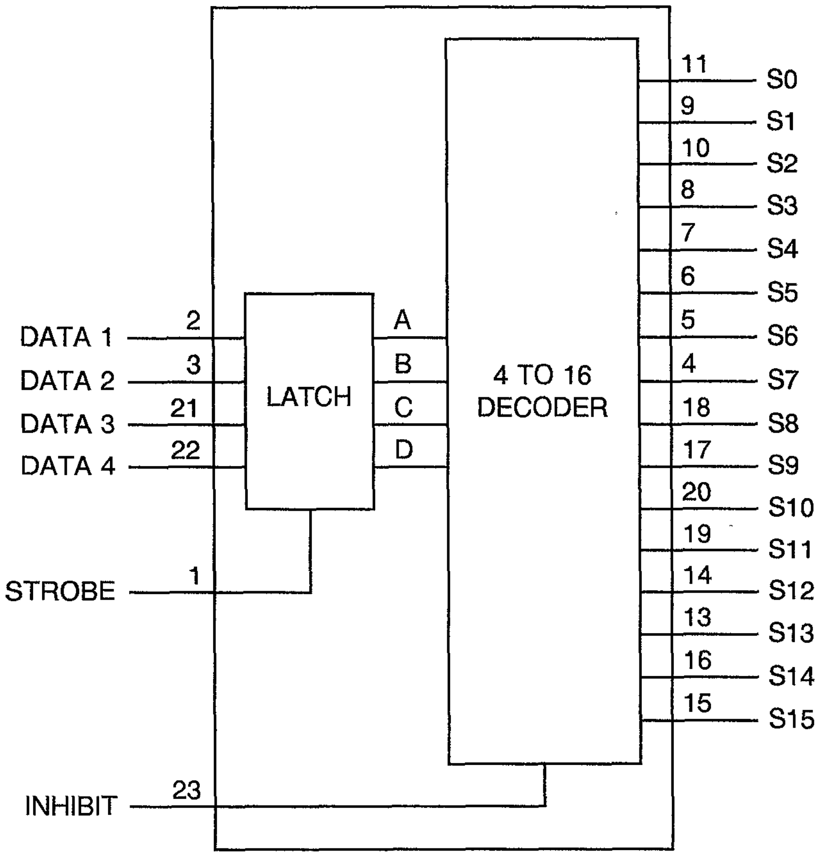
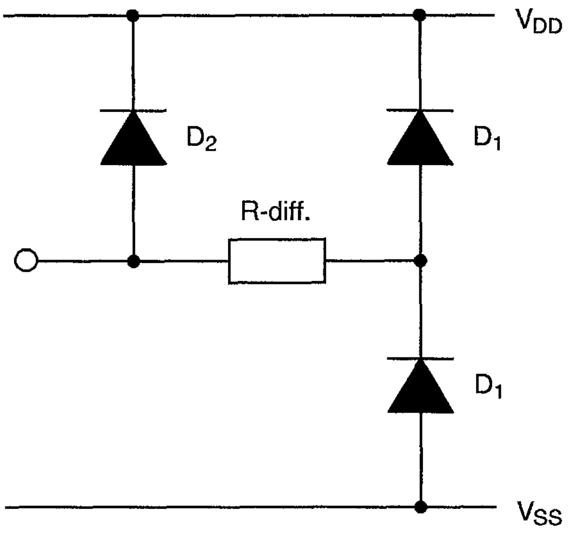


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} - Input Clamp Voltage
P_{DSO} - Single Output Power Dissipation
CKT - Circuit

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirement and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

4.2.3.1 Deviations from High Temperature Reverse Bias (H.T.R.B.)

Prior to operating power burn-in, a high temperature reverse bias (H.T.R.B.) screen at +125°C shall be added for the N-Channel and then for the P-Channel in accordance with Tables 5(a) and 5(b) of this specification. Each exposure to H.T.R.B. shall be 72 hours and Table 4 Parameter Drift Values shall be applied at 0 and 144 hours.

4.2.4 Deviations from Qualification, Environmental and Endurance Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 4.25 grammes for the dual-in-line package, 1.55 grammes for the flat package, 1.1 grammes for the SO package and 0.79 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed or preform-soldered.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with either Type '4' or Type '2 or 8' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with ESA/SCC Basic Specification No. 23500. For SO ceramic packages, the material shall be Type 'G' with either Type '2' or Type '4' finish in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line, flat and SO packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:-

920501101B

Detail Specification Number

Type Variant, as applicable

Testing Level (B or C, as appropriate)

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0\text{-}5)$ °C and -55(+5-0) °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $+22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. and Burn-in

The requirements for H.T.R.B. and Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and Burn-in shall be as specified in Tables 5(a), 5(b) and 5(c) of this specification.

4.7.3 Electrical Circuits for H.T.R.B. and Burn-in

Circuits for use in performing the H.T.R.B. and Burn-in tests are shown in Figures 5(a), 5(b) and 5(c) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 18	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 12) (Pin C 14)	-	1.0	µA
19 to 24	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0Vdc V_{IN} (Remaining Inputs) = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	-50	nA
25 to 30	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 15Vdc V_{IN} (Remaining Inputs) = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	50	nA
31 to 46	Output Voltage Low Level	V_{OL}	3007	4(e)	Input Conditions as per Table 4(e) V_{IH} = 15Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 15Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-	0.05	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
47 to 62	Output Voltage High Level	V_{OH}	3006	4(f)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 15Vdc V_{IN} (Inhibit) = 15Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	14.95	-	V
63 to 78	Output Drive Current N-Channel	I_{OL1}	-	4(g)	Input Conditions as per Table 4(e) V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 5Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = 0.4Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	0.51	-	mA
79 to 94	Output Drive Current N-Channel	I_{OL2}	-	4(g)	Input Conditions as per Table 4(e) V_{IH} = 15Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 15Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = 1.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	3.4	-	mA
95 to 110	Output Drive Current P-Channel	I_{OH1}	-	4(h)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 5Vdc V_{IN} (Inhibit) = 5Vdc V_{OUT} = 4.6Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-0.51	-	mA

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
111 to 126	Output Drive Current P-Channel	I_{OH2}	-	4(h)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 15Vdc V_{IN} (Inhibit) = 15Vdc V_{OUT} = 13.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-3.4	-	mA
127	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	-	4(a)	V_{IL} = 1.5Vdc V_{IH} = 3.5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}				-	0.5	
128	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL2}	-	4(a)	V_{IL} = 4Vdc V_{IH} = 11Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH2}				-	1.5	
129	Threshold Voltage N-Channel	V_{THN}	-	4(i)	Strobe Input at Ground: All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10µA (Pin D/F 12) (Pin C 14)	-0.7	-3.0	V
130	Threshold Voltage P-Channel	V_{THP}	-	4(j)	Strobe Input at Ground: All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10µA (Pin D/F 24) (Pin C 28)	0.7	3.0	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
131 to 136	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(k)	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0Vdc All Other Pins Open (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	-2.0	V
137 to 142	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(l)	V_{IN} (Under Test) = 6Vdc V_{SS} = Open, R = 30kΩ (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	3.0	-	V

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
143 to 148	Input Capacitance	C_{IN}	3012	4(m)	V_{IN} (Not under Test) = 0Vdc $V_{DD} = V_{SS} = 0Vdc$ Note 6 (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	7.5	pF
149	Propagation Delay Low to High (Data 1 to S0)	t_{PLH1}	3003	4(n)	V_{IN} (Under Test) = Pulse Generator $V_{IL} = 0Vdc$, $V_{IH} = 5Vdc$ V_{IN} (Strobe) = 5Vdc V_{IN} (All Other Inputs) = 0Vdc $V_{DD} = 5Vdc$, $V_{SS} = 0Vdc$ Note 7 Pins D/F Pins C 2 to 11 2 to 13	-	920	ns
150	Propagation Delay Low to High (Inhibit to S0)	t_{PLH2}	3003	4(n)	V_{IN} (Under Test) = Pulse Generator $V_{IL} = 0Vdc$, $V_{IH} = 5Vdc$ V_{IN} (Strobe) = 5Vdc V_{IN}(All Other Inputs) = 0Vdc $V_{DD} = 5Vdc$, $V_{SS} = 0Vdc$ Note 7 Pins D/F Pins C 23 to 11 27 to 13	-	450	ns
151	Propagation Delay High to Low (Data 1 to S0)	t_{PHL1}	3003	4(n)	V_{IN} (Under Test) = Pulse Generator $V_{IL} = 0Vdc$, $V_{IH} = 5Vdc$ V_{IN} (Strobe) = 5Vdc V_{IN} (All Other Inputs) = 0Vdc $V_{DD} = 5Vdc$, $V_{SS} = 0Vdc$ Note 7 Pins D/F Pins C 2 to 11 2 to 13	-	920	ns
152	Propagation Delay High to Low (Inhibit to S0)	t_{PHL2}	3003	4(n)	V_{IN} (Under Test) = Pulse Generator $V_{IL} = 0Vdc$, $V_{IH} = 5Vdc$ V_{IN} (Strobe) = 5Vdc V_{IN}(All Other Inputs) = 0Vdc $V_{DD} = 5Vdc$, $V_{SS} = 0Vdc$ Note 7 Pins D/F Pins C 23 to 11 27 to 13	-	450	ns

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
153	Transition Time Low to High	t_{TLH}	3004	4(n)	V_{IN} (Under Test) = Pulse Generator V_{IL} = 0Vdc, V_{IH} = 5Vdc V_{IN} (Strobe) = 5Vdc V_{IN} (All Other Inputs) = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 7 (Pin D/F 11) (Pin C 13)	-	150	ns
154	Transition Time High to Low	t_{THL}	3004	4(n)	V_{IN} (Under Test) = Pulse Generator V_{IL} = 0Vdc, V_{IH} = 5Vdc V_{IN} (Strobe) = 5Vdc V_{IN} (All Other Inputs) = 0Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 7 (Pin D/F 11) (Pin C 13)	-	150	ns

NOTES

1. GO-NO-GO Test, each pattern of Test Table 4(a).
   $V_{OH} \geq V_{DD} - 0.5\text{Vdc}$ $\qquad$ $V_{OL} \leq 0.5\text{Vdc}$
2. Maximum time to output comparator strobe 300μsec.
3. Test each pattern of Test Table 4(b).
4. Interchange of forcing and measuring function is permitted.
5. This is performed as a Functional Test in which extreme V_{IN} conditions are applied and output voltage is measured.
6. Measurement performed on a sample basis, LTPD7 or less, with a Capacitance Bridge connected between each input under test and V_{SS}, only for Lots where LAT Level 2 is to be performed. (For LTPD sampling plan, see Annexe I of ESA/SCC 9000).
7. Measurement performed on a sample basis, LTPD7 or less, (see Annexe I of ESA/SCC 9000).

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 3Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. V_{DD} = 15Vdc, V_{SS} = 0Vdc Notes 1 and 2	-	-	-
3 to 18	Quiescent Current	I_{DD}	3005	4(b)	V_{IL} = 0Vdc, V_{IH} = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 3 (Pin D/F 12) (Pin C 14)	-	30	µA
19 to 24	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0Vdc V_{IN} (Remaining Inputs) = 15Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	-100	nA
25 to 30	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 15Vdc V_{IN} (Remaining Inputs) = 0Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	100	nA
31 to 46	Output Voltage Low Level	V_{OL}	3007	4(e)	Input Conditions as per Table 4(e) V_{IH} = 15Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 15Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-	0.05	V

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
47 to 62	Output Voltage High Level	V_{OH}	3006	4(f)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 15Vdc V_{IN} (Inhibit) = 15Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	14.95	-	V
63 to 78	Output Drive Current N-Channel	I_{OL1}	-	4(g)	Input Conditions as per Table 4(e) V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 5Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = 0.4Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	0.36	-	mA
79 to 94	Output Drive Current N-Channel	I_{OL2}	-	4(g)	Input Conditions as per Table 4(e) V_{IH} = 15Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 15Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = 1.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	2.4	-	mA
95 to 110	Output Drive Current P-Channel	I_{OH1}	-	4(h)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 5Vdc V_{IN} (Inhibit) = 5Vdc V_{OUT} = 4.6Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-0.36	-	mA

NOTES: See Page 23.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
111 to 126	Output Drive Current P-Channel	I_{OH2}	-	4(h)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 15Vdc V_{IN} (Inhibit) = 15Vdc V_{OUT} = 13.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-2.4	-	mA
127	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	-	4(a)	V_{IL} = 1.5Vdc V_{IH} = 3.5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}				-	0.5	
128	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL2}	-	4(a)	V_{IL} = 4Vdc V_{IH} = 11Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH2}				-	1.5	
129	Threshold Voltage N-Channel	V_{THN}	-	4(i)	Strobe Input at Ground: All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10µA (Pin D/F 12) (Pin C 14)	-0.3	-3.5	V
130	Threshold Voltage P-Channel	V_{THP}	-	4(j)	Strobe Input at Ground: All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10µA (Pin D/F 24) (Pin C 28)	0.3	3.5	V

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 3Vdc$, $V_{SS} = 0Vdc$ Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 15Vdc$, $V_{SS} = 0Vdc$ Notes 1 and 2	-	-	-
3 to 18	Quiescent Current	I_{DD}	3005	4(b)	$V_{IL} = 0Vdc$, $V_{IH} = 15Vdc$ $V_{DD} = 15Vdc$, $V_{SS} = 0Vdc$ Note 3 (Pin D/F 12) (Pin C 14)	-	1.0	μA
19 to 24	Input Current Low Level	I_{IL}	3009	4(c)	V_{IN} (Under Test) = 0Vdc V_{IN} (Remaining Inputs) = 15Vdc $V_{DD} = 15Vdc$, $V_{SS} = 0Vdc$ (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	-50	nA
25 to 30	Input Current High Level	I_{IH}	3010	4(d)	V_{IN} (Under Test) = 15Vdc V_{IN} (Remaining Inputs) = 0Vdc $V_{DD} = 15Vdc$, $V_{SS} = 0Vdc$ (Pins D/F 1-2-3-21-22-23) (Pins C 1-2-3-24-26-27)	-	50	nA
31 to 46	Output Voltage Low Level	V_{OL}	3007	4(e)	Input Conditions as per Table 4(e) $V_{IH} = 15Vdc$, $V_{IL} = 0Vdc$ V_{IN}(Strobe) = 15Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = Open $V_{DD} = 15Vdc$, $V_{SS} = 0Vdc$ (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-	0.05	V

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
47 to 62	Output Voltage High Level	V_{OH}	3006	4(f)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 15Vdc V_{IN} (Inhibit) = 15Vdc V_{OUT} = Open V_{DD} = 15Vdc, V_{SS} = 0Vdc (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	14.95	-	V
63 to 78	Output Drive Current N-Channel	I_{OL1}	-	4(g)	Input Conditions as per Table 4(e) V_{IH} = 5Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 5Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = 0.4Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	0.64	-	mA
79 to 94	Output Drive Current N-Channel	I_{OL2}	-	4(g)	Input Conditions as per Table 4(e) V_{IH} = 15Vdc, V_{IL} = 0Vdc V_{IN}(Strobe) = 15Vdc V_{IN}(Inhibit) = 0Vdc V_{OUT} = 1.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	4.2	-	mA
95 to 110	Output Drive Current P-Channel	I_{OH1}	-	4(h)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 5Vdc V_{IN} (Inhibit) = 5Vdc V_{OUT} = 4.6Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-0.64	-	mA

NOTES: See Page 23.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
111 to 126	Output Drive Current P-Channel	I_{OH2}	-	4(h)	V_{IN} (Data Inputs) = 0Vdc V_{IN} (Strobe) = 15Vdc V_{IN} (Inhibit) = 15Vdc V_{OUT} = 13.5Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	-4.2	-	mA
127	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	-	4(a)	V_{IL} = 1.5Vdc V_{IH} = 3.5Vdc V_{DD} = 5Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}				-	0.5	
128	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL2}	-	4(a)	V_{IL} = 4Vdc V_{IH} = 11Vdc V_{DD} = 15Vdc, V_{SS} = 0Vdc Note 5 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH2}				-	1.5	
129	Threshold Voltage N-Channel	V_{THN}	-	4(i)	Strobe Input at Ground: All Other Inputs: V_{IN} = 5Vdc V_{DD} = 5Vdc, I_{SS} = -10µA (Pin D/F 12) (Pin C 14)	-0.7	-3.5	V
130	Threshold Voltage P-Channel	V_{THP}	-	4(j)	Strobe Input at Ground: All Other Inputs: V_{IN} = -5Vdc V_{SS} = -5Vdc, I_{DD} = 10µA (Pin D/F 24) (Pin C 28)	0.7	3.5	V

NOTES: See Page 23.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - FUNCTIONAL TEST TABLE

PATTERN NO.	PIN NUMBERS																						D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23	12	24
1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	V_{DD}
2	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	0	0	↓	↓
3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1		
4	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	0	0		
5	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	0	0		
6	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0		
7	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1		
8	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0		
9	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0		
10	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0		
11	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1		
12	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0		
13	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0		
14	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0		
15	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1		
16	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0		
17	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
18	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
19	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1		
20	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
21	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
22	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
23	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1		
24	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
25	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
26	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
27	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1		
28	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
29	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
30	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
31	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1		
32	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0		
33	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0		
34	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0		
35	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1		
36	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0		
37	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	0		
38	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	0		
39	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1		
40	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	0		
41	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	0		
42	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0		
43	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1		
44	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0		
45	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0		

NOTES: See Page 31.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONT'D)

FIGURE 4(a) - FUNCTIONAL TEST TABLE (CONT'D)

PATTERN NO.	PIN NUMBERS																						D.C. SUPPLY	
	1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	21	22	23	12	24
46	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	V_{DD}
47	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	↓	↓
48	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0		
49	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0		
50	1	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0		
51	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
52	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0		
53	0	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0		
54	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0		
55	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
56	0	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0		
57	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0		
58	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0		
59	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
60	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0		
61	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0		
62	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0		
63	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
64	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0		
65	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0		

NOTES

1. Figure 4(a) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - QUIESCENT CURRENT TEST TABLE

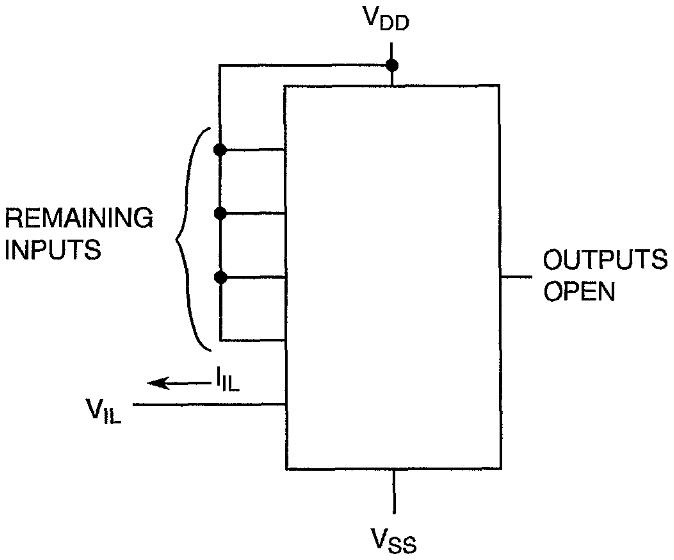
PATTERN NO.	PIN NUMBERS																						D.C. SUPPLY	
	INPUTS						OUTPUTS																	
	1	2	3	21	22	23	4	5	6	7	8	9	10	11	13	14	15	16	17	18	19	20	12	24
1	1	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	V_{SS}	V_{DD}
2	1	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
3	1	0	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
4	1	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
5	1	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
6	1	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
7	1	0	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
8	1	1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
9	1	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
10	1	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
11	1	0	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
12	1	1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
13	1	0	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
14	1	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
15	1	0	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
16	1	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		

NOTES

1. Figure 4(b) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
2. Logic Level Definitions: $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$, X = Don't Care.

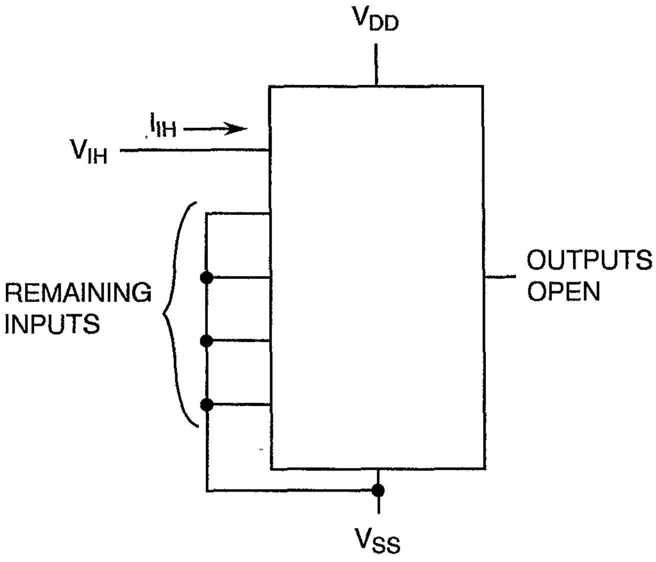
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(c) - LOW LEVEL INPUT CURRENT



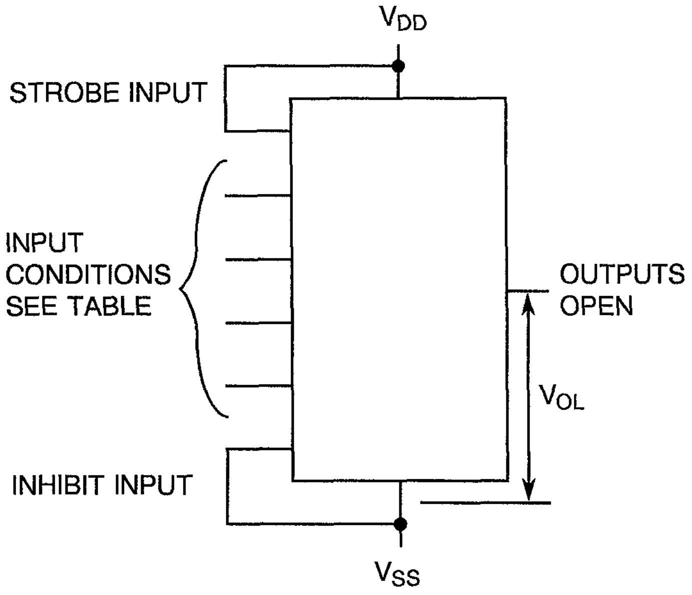
NOTES
1. Each input to be tested separately.

FIGURE 4(d) - HIGH LEVEL INPUT CURRENT



NOTES
1. Each input to be tested separately.

FIGURE 4(e) - LOW LEVEL OUTPUT VOLTAGE



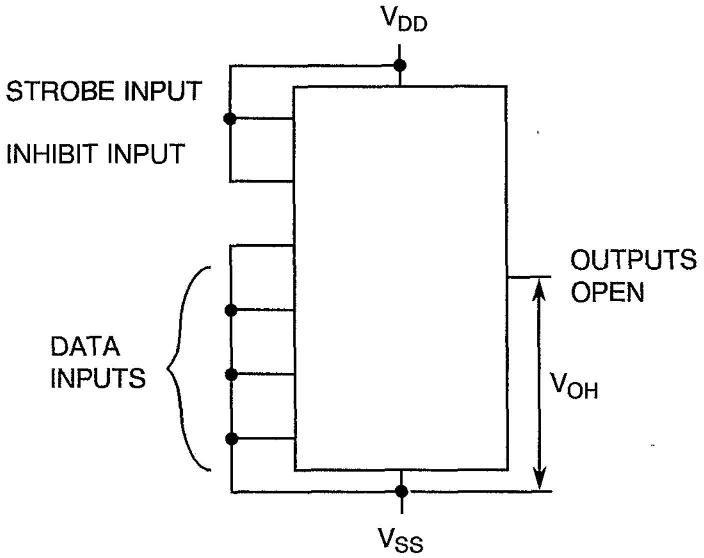
NOTES
1. Each output to be tested separately.
2. $1 = V_{IH} = V_{DD}$, $0 = V_{IL} = V_{SS}$.

TABLE 4(e)

TEST NO.	INPUT CONDITIONS			
	D1	D2	D3	D4
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

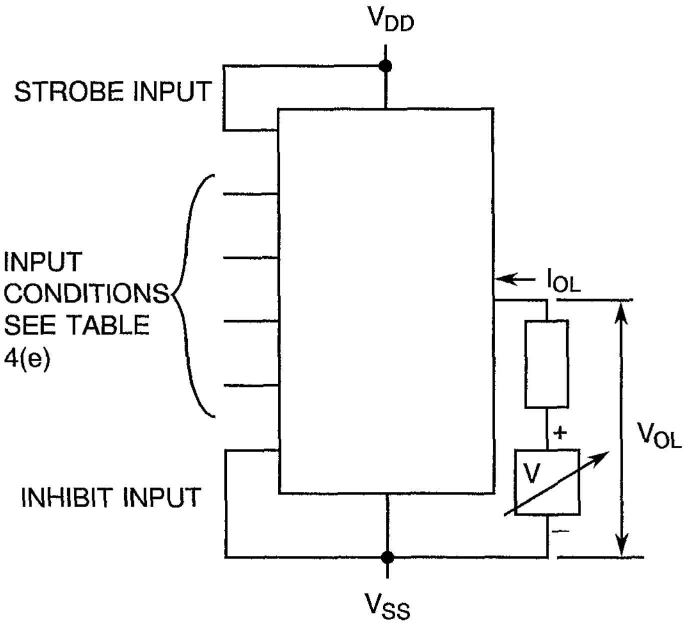
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - HIGH LEVEL OUTPUT VOLTAGE



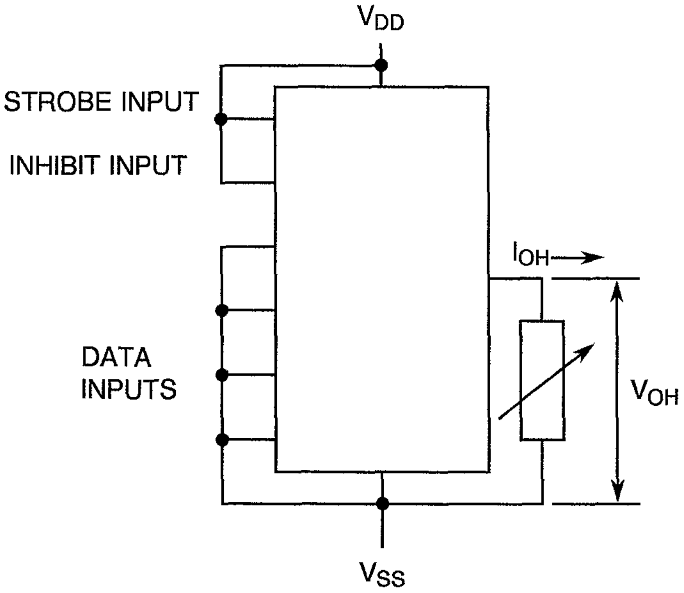
NOTES
1. Each output to be tested separately.

FIGURE 4(g) - LOW LEVEL OUTPUT CURRENT



NOTES
1. Each output to be tested separately.

FIGURE 4(h) - HIGH LEVEL OUTPUT CURRENT



NOTES
1. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - THRESHOLD VOLTAGE N-CHANNEL

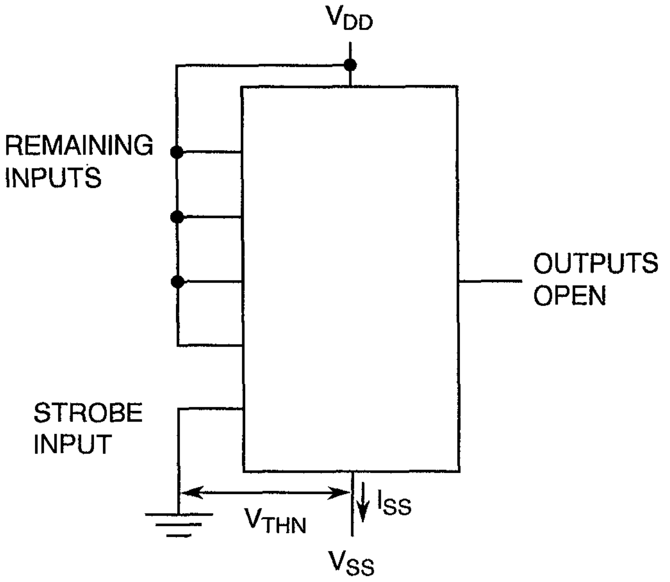


FIGURE 4(j) - THRESHOLD VOLTAGE P-CHANNEL

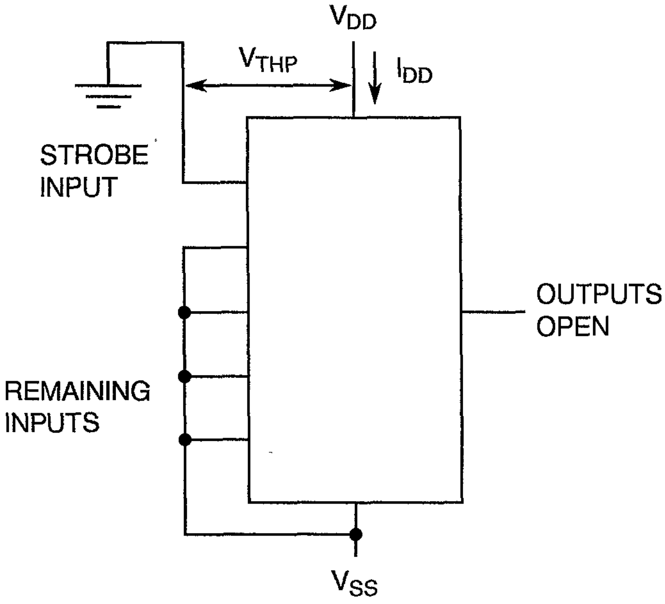
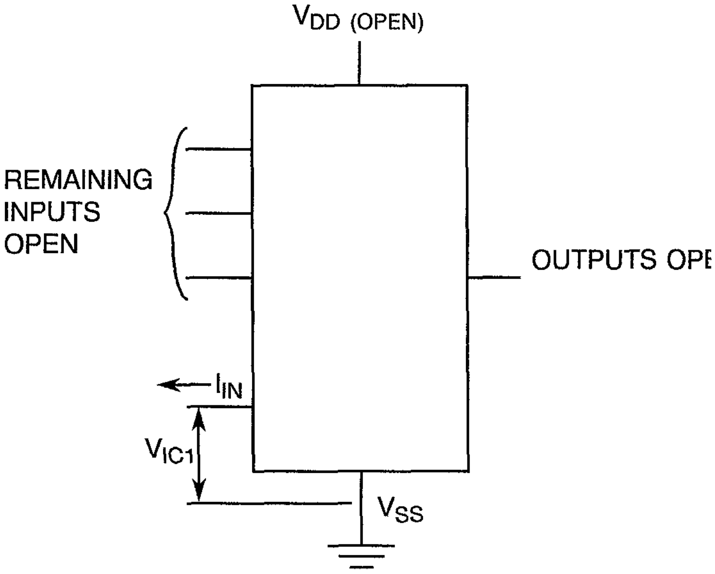


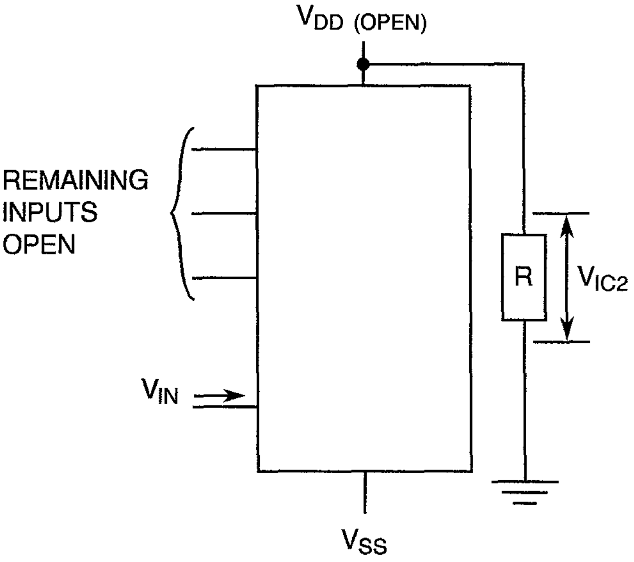
FIGURE 4(k) - INPUT CLAMP VOLTAGE (V_{SS})



NOTES

1. Each input to be tested separately.

FIGURE 4(l) - INPUT CLAMP VOLTAGE (V_{DD})

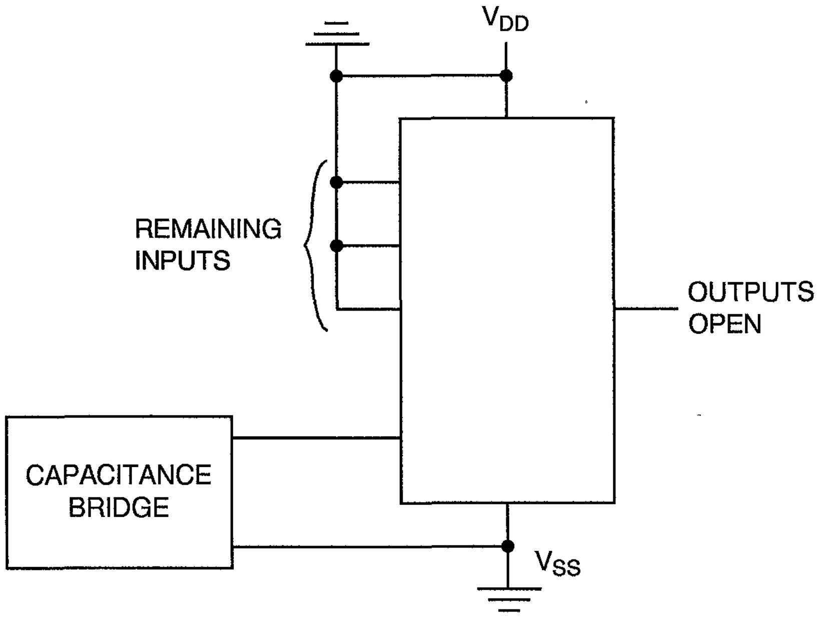


NOTES

1. Each input to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

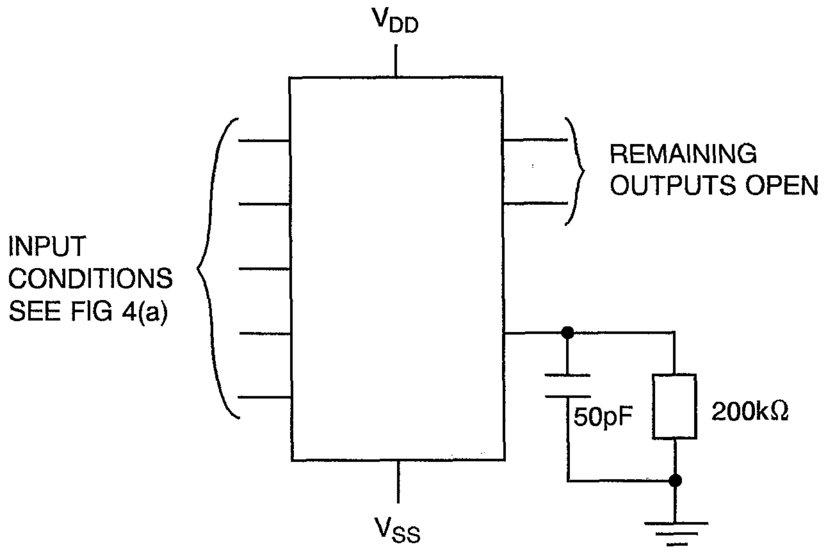
FIGURE 4(m) - INPUT CAPACITANCE



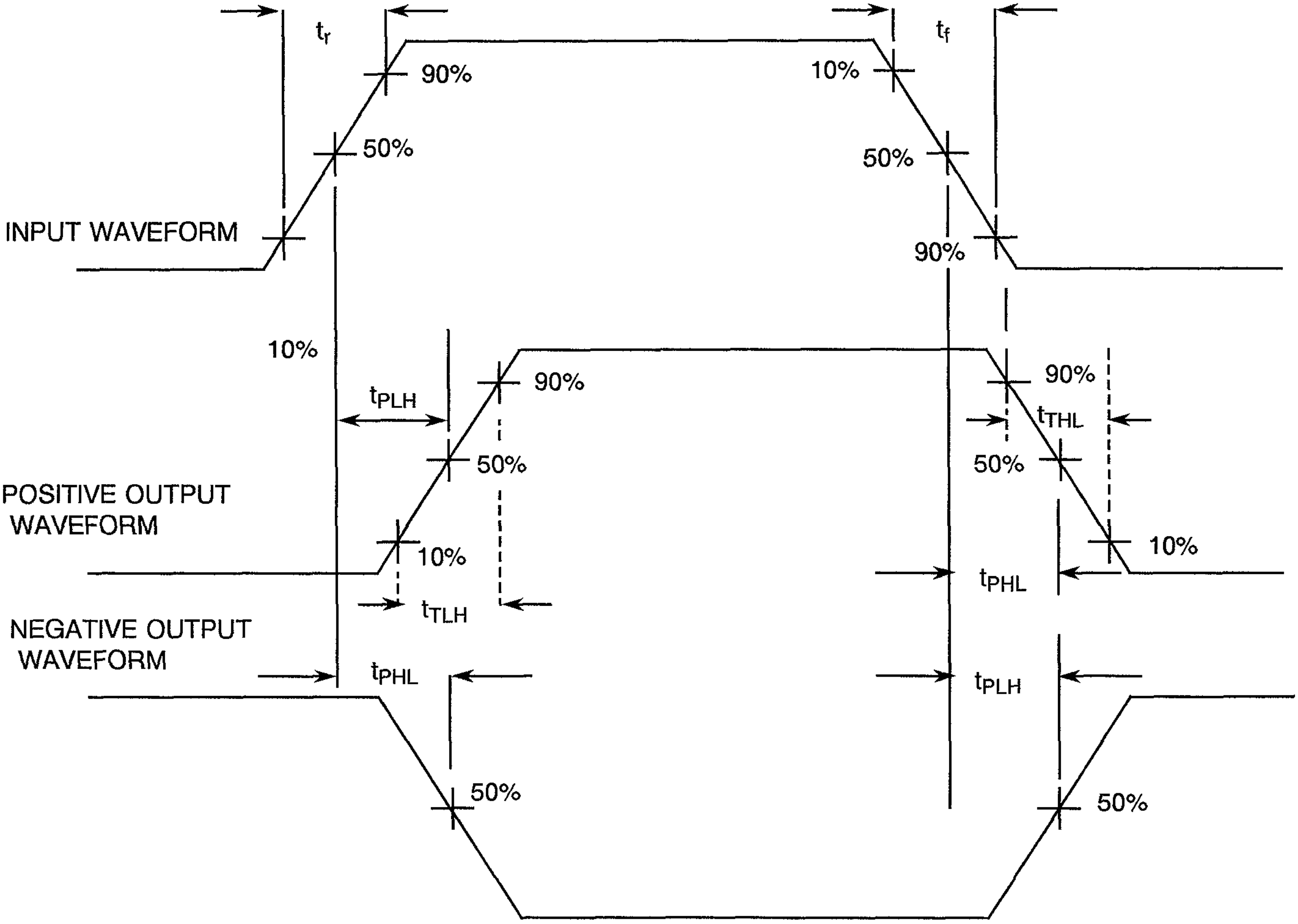
NOTES
1. Each input to be tested separately.
2. f = 100kHz to 1MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(n) - PROPAGATION DELAY AND TRANSITION TIME



VOLTAGE WAVEFORMS



NOTES

1. Pulse Generator - $V_P = 0$ to V_{DD}, t_r and $t_f \leq$ 15ns, f = 500kHz.

TABLE 4 - PARAMETER DRIFT VALUES

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
3 to 18	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	± 150	nA
63 to 78	Output Drive Current N-Channel	I_{OL1}	As per Table 2	As per Table 2	± 15 (1)	%
95 to 110	Output Drive Current P-Channel	I_{OH1}	As per Table 2	As per Table 2	± 15 (1)	%
129	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	± 0.3	V
130	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	± 0.3	V

NOTES

1. Percentage of limit value if voltage is the measurement function.

TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125 (+0-5)	°C
2	Outputs - (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	V_{OUT}	Open	-
3	Inputs - (Pins D/F 21-22-23) (Pins C 24-26-27)	V_{IN}	Ground	Vdc
4	Inputs - (Pins D/F 1-2-3) (Pins C 1-2-3)	V_{IN}	V_{DD}	Vdc
5	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{DD}	15	Vdc
6	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	V_{SS}	Ground	Vdc

NOTES

1. Input Load = Protection Resistor = 2kΩ minimum to 47kΩ maximum.

TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125 (+0-5)	°C
2	Outputs - (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	V_{OUT}	Open	-
3	Inputs - (Pins D/F 21-22-23) (Pins C 24-26-27)	V_{IN}	V_{DD}	Vdc
4	Inputs - (Pins D/F 1-2-3) (Pins C 1-2-3)	V_{IN}	Ground	Vdc
5	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{DD}	15	Vdc
6	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	V_{SS}	Ground	Vdc

NOTES

1. Input Load = Protection Resistor = 2kΩ minimum to 47kΩ maximum.

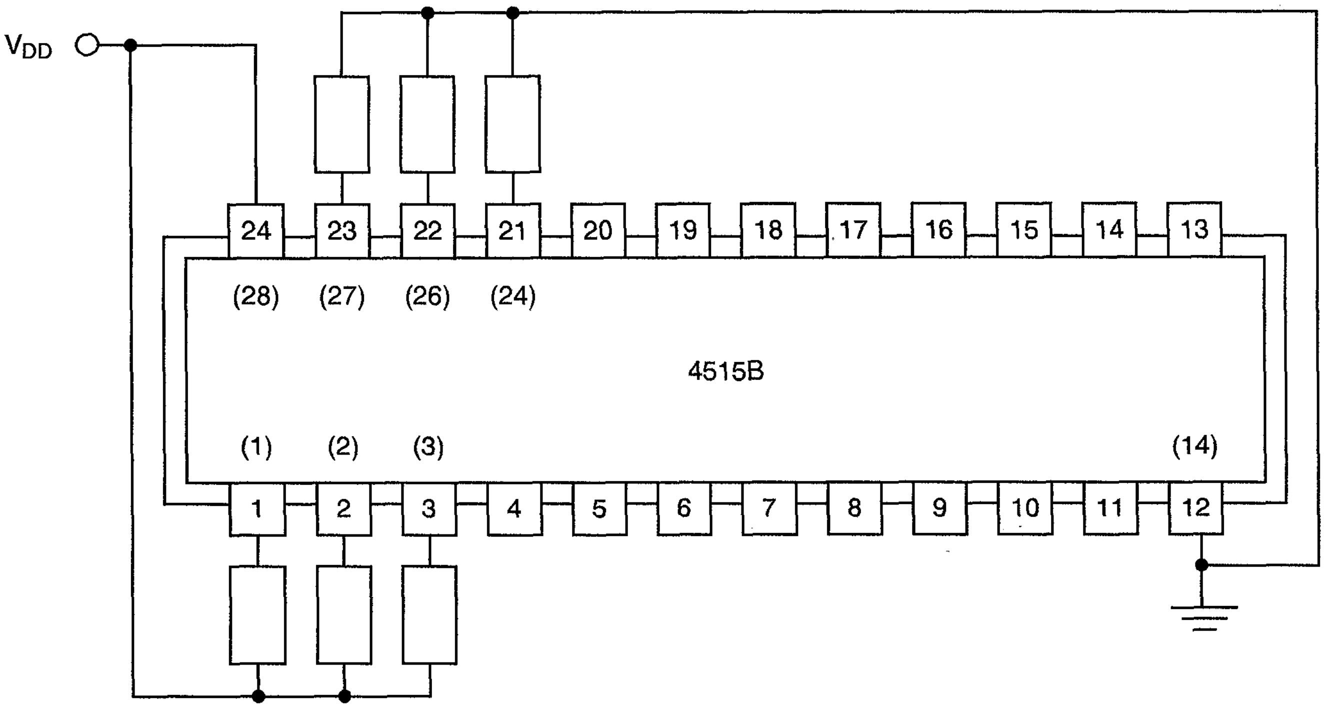
TABLE 5(c) - CONDITIONS FOR BURN-IN DYNAMIC

NO.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	+125 (+0-5)	°C
2	Outputs - (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-8-9-10-12-13-15-16-17-19-20-21-22-23)	V_{OUT}	$V_{DD/2}$	Vdc
3	Inputs - (Pins D/F 2-3) (Pins C 2-3)	V_{IN}	Ground	Vdc
4	Inputs - (Pins D/F 21-22) (Pins C 24-26)	V_{IN}	V_{DD}	Vdc
5	Input - (Pin D/F 23) (Pin C 27)	V_{IN}	V_{GEN2}	Vac
6	Input - (Pin D/F 1) (Pin C 1)	V_{IN}	V_{GEN1}	Vac
7	Pulse Voltage	V_{GEN}	0 to V_{DD}	Vac
8	Pulse Frequency Square Wave	f_{GEN1} f_{GEN2}	$50k \leq f < 1M$ 50% Duty Cycle $25k \leq f < 0.5M$ 50% Duty Cycle	Hz
9	Positive Supply Voltage (Pin D/F 24) (Pin C 28)	V_{DD}	15	Vdc
10	Negative Supply Voltage (Pin D/F 12) (Pin C 14)	V_{SS}	Ground	Vdc

NOTES

1. Input Load = Output Load = 2kΩ minimum to 47kΩ maximum.

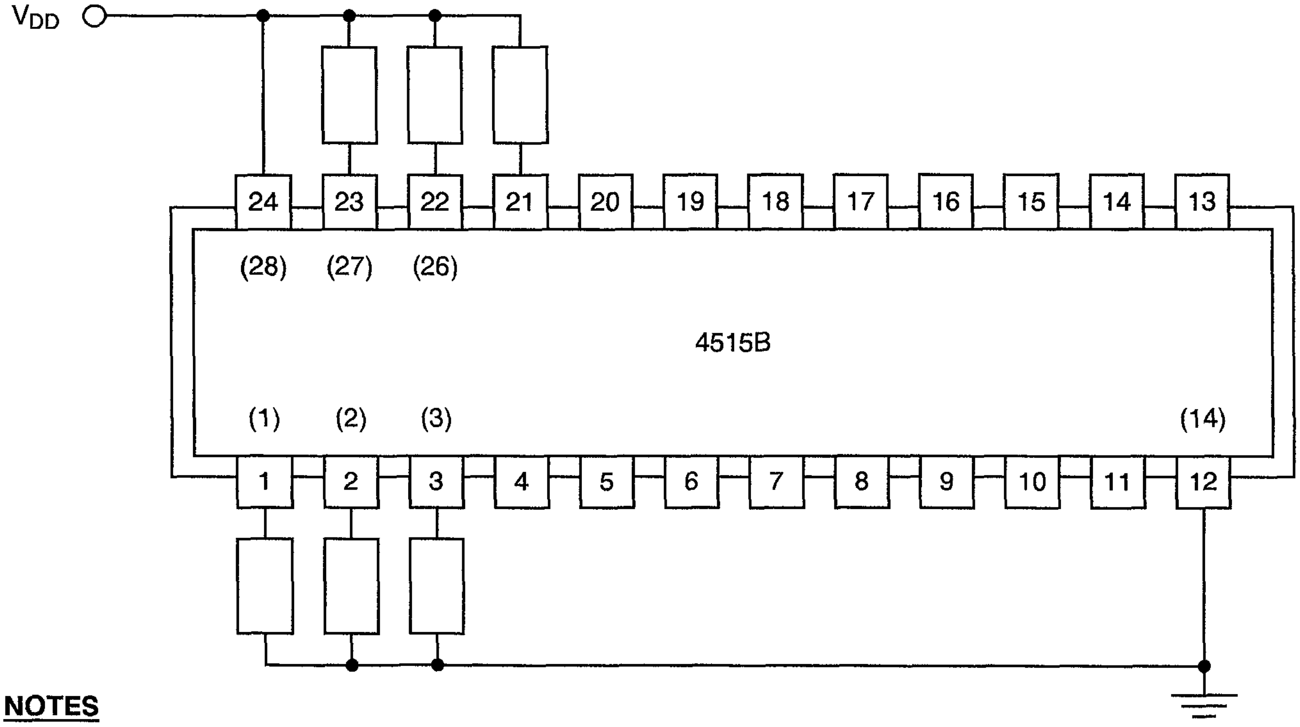
FIGURE 5(a) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.

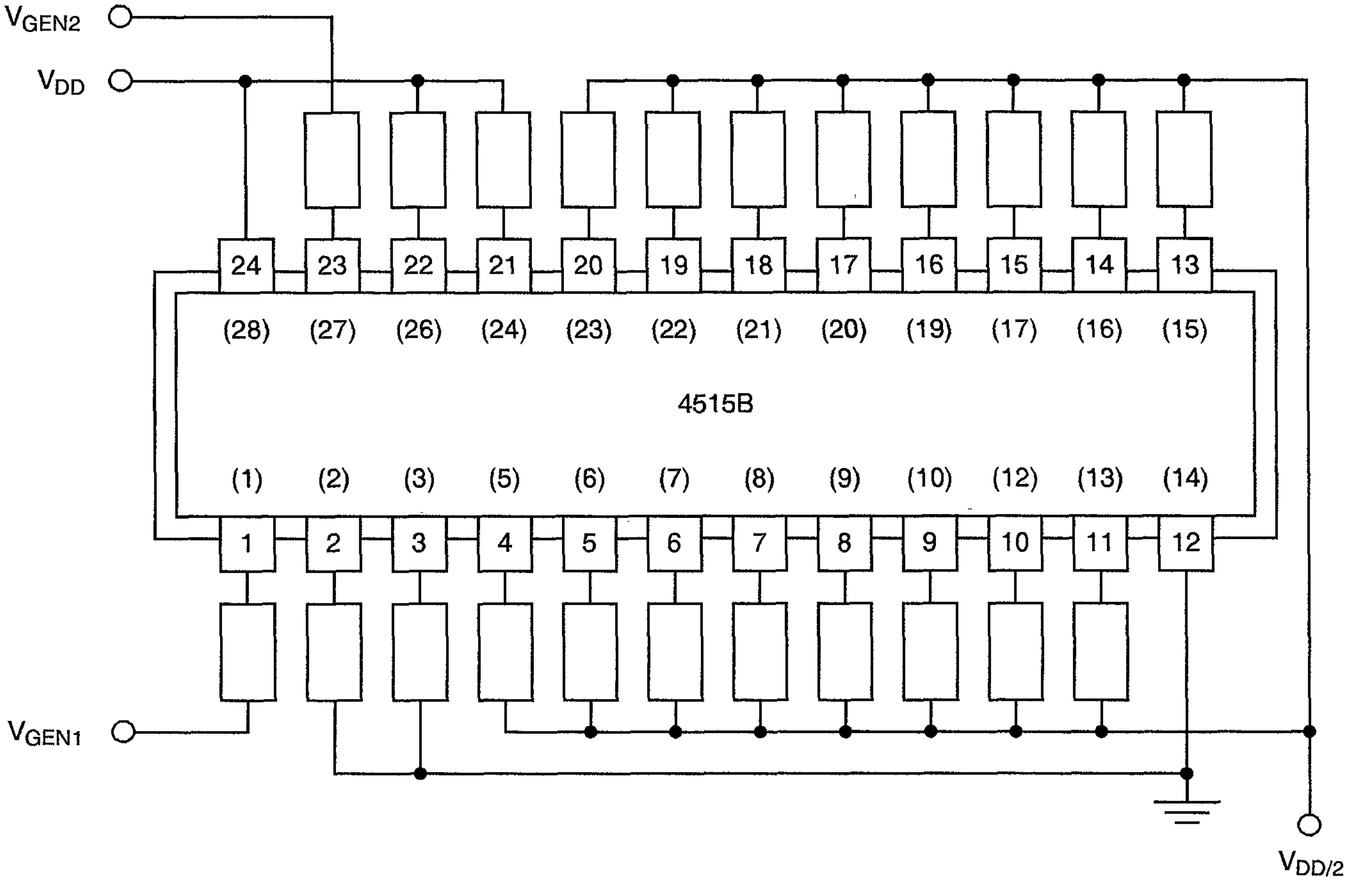
FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.

FIGURE 5(c) - ELECTRICAL CIRCUIT FOR BURN-IN DYNAMIC



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Test

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)			UNIT
						MIN	MAX	
1	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
3 to 18	Quiescent Current	I_{DD}	As per Table 2	As per Table 2	± 150	-	-	nA
19 to 24	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	-	-	-50	nA
25 to 30	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	-	-	50	nA
31 to 46	Output Voltag Low Level	V_{OL}	As per Table 2	As per Table 2	-	-	0.05	V
47 to 62	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	-	14.95	-	V
63 to 78	Output Drive Current N-Channel	I_{OL1}	As per Table 2	As per Table 2	± 15 (1)	-	-	%
79 to 94	Output Drive Current N-Channel	I_{OL2}	As per Table 2	As per Table 2	± 15 (1)	-	-	%
95 to 110	Output Drive Current P-Channel	I_{OH1}	As per Table 2	As per Table 2	± 15 (1)	-	-	%
111 to 126	Output Drive Current P-Channel	I_{OH2}	As per Table 2	As per Table 2	± 15 (1)	-	-	%
127	Input Voltage Low Level (Noise Immunity) (Functional Test)	V_{IL1}	As per Table 2	As per Table 2	-	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V_{IH1}			-	-	0.5	
129	Threshold Voltage N-Channel	V_{THN}	As per Table 2	As per Table 2	±0.3	-	-	V
130	Threshold Voltage P-Channel	V_{THP}	As per Table 2	As per Table 2	±0.3	-	-	V

NOTES

1. Percentage of limit value if voltage is the measurement function.

APPENDIX 'A'

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AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATION
Para. 4.2.3	Para. 9.23, High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used. Para. 9.24, Power Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.4	Para. 9.21.1, Operating Life during Qualification Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.5	Para. 9.21.2, Operating Life during Lot Acceptance Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.