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Pages 1 to 49

**INTEGRATED CIRCUITS, SILICON MONOLITHIC,  
CMOS DUAL 4-STAGE STATIC SHIFT REGISTER,  
WITH SERIAL INPUT/PARALLEL OUTPUT  
BASED ON TYPE 4015B**

**ESA/SCC Detail Specification No. 9306/015**



**space components  
coordination group**

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		SCCG Chairman	ESA Director General or his Deputy
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**DOCUMENTATION CHANGE NOTICE**

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		DCN		None
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		Table 1(a)	: Variants 10 and 11 added	221565
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		Appendix 'A'	: Appendix added	221602

**TABLE OF CONTENTS**

	<u>Page</u>
<b>1. <u>GENERAL</u></b>	<b>5</b>
1.1 Scope	5
1.2 Component Type Variants	5
1.3 Maximum Ratings	5
1.4 Parameter Derating Information	5
1.5 Physical Dimensions	5
1.6 Pin Assignment	5
1.7 Truth Table	5
1.8 Circuit Schematic	5
1.9 Functional Diagram	5
1.10 Handling Precautions	5
1.11 Input Protection Network	5
<b>2. <u>APPLICABLE DOCUMENTS</u></b>	<b>17</b>
<b>3. <u>TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS</u></b>	<b>17</b>
<b>4. <u>REQUIREMENTS</u></b>	<b>17</b>
4.1 General	17
4.2 Deviations from Generic Specification	17
4.2.1 Deviations from Special In-process Controls	17
4.2.2 Deviations from Final Production Tests	17
4.2.3 Deviations from Burn-in Tests	17
4.2.4 Deviations from Qualification Tests	17
4.2.5 Deviations from Lot Acceptance Tests	18
4.3 Mechanical Requirements	18
4.3.1 Dimension Check	18
4.3.2 Weight	18
4.4 Materials and Finishes	18
4.4.1 Case	18
4.4.2 Lead Material and Finish	18
4.5 Marking	18
4.5.1 General	18
4.5.2 Lead Identification	18
4.5.3 The SCC Component Number	19
4.5.4 Traceability Information	19
4.6 Electrical Measurements	19
4.6.1 Electrical Measurements at Room Temperature	19
4.6.2 Electrical Measurements at High and Low Temperatures	19
4.6.3 Circuits for Electrical Measurements	19
4.7 Burn-in Tests	19
4.7.1 Parameter Drift Values	19
4.7.2 Conditions for H.T.R.B. and Burn-in	19
4.7.3 Electrical Circuits for H.T.R.B. and Burn-in	19
4.8 Environmental and Endurance Tests	47
4.8.1 Electrical Measurements on Completion of Environmental Tests	47
4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests	47
4.8.3 Electrical Measurements on Completion of Endurance Tests	47
4.8.4 Conditions for Operating Life Test	47
4.8.5 Electrical Circuits for Operating Life Tests	47
4.8.6 Conditions for High Temperature Storage Test	47

**TABLES**

	<u>Page</u>
1(a) Type Variants	6
1(b) Maximum Ratings	6
2 Electrical Measurements at Room Temperature, d.c. Parameters	20
Electrical Measurements at Room Temperature, a.c. Parameters	24
3(a) Electrical Measurements at High Temperature	26
3(b) Electrical Measurements at Low Temperature	30
4 Parameter Drift Values	42
5(a) Conditions for Burn-in High Temperature Reverse Bias, N-Channels	43
5(b) Conditions for Burn-in High Temperature Reverse Bias, P-Channels	43
5(c) Conditions for Burn-in Dynamic	44
6 Electrical Measurements on Completion of Environmental Tests and at Intermediate Points and on Completion of Endurance Testing	48

**FIGURES**

1 Not applicable	
2 Physical Dimensions	7
3(a) Pin Assignment	13
3(b) Truth Table	13
3(c) Circuit Schematic	14
3(d) Functional Diagram	15
3(e) Input Protection Network	16
4 Circuits for Electrical Measurements	34
5(a) Electrical Circuit for Burn-in High Temperature Reverse Bias, N-Channels	45
5(b) Electrical Circuit for Burn-in High Temperature Reverse Bias, P-Channels	45
5(c) Electrical Circuit for Burn-in Dynamic	46

**APPENDICES (Applicable to specific Manufacturers only)**

'A' Agreed Deviations for STMicroelectronics (F)	49
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**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, CMOS Dual 4-Stage Static Shift Register, with Serial Input and Parallel Output, having fully buffered outputs, based on Type 4015B. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

**1.2 COMPONENT TYPE VARIANTS**

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

**1.3 MAXIMUM RATINGS**

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

Maximum ratings shall only be exceeded during testing to the extent specified in this specification and when stipulated in Test Methods and Procedures of the applicable ESA/SCC Generic Specification.

**1.4 PARAMETER DERATING INFORMATION (FIGURE 1)**

Not applicable.

**1.5 PHYSICAL DIMENSIONS**

As Per Figure 2.

**1.6 PIN ASSIGNMENT**

As per Figure 3(a).

**1.7 TRUTH TABLE**

As per Figure 3(b).

**1.8 CIRCUIT SCHEMATIC**

As per Figure 3(c).

**1.9 FUNCTIONAL DIAGRAM**

As per Figure 3(d).

**1.10 HANDLING PRECAUTIONS**

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 400Volts.

**1.11 INPUT PROTECTION NETWORK**

Double diode protection shall be incorporated into each input as shown in Figure 3(e).

**TABLE 1(a) - TYPE VARIANTS**

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	FLAT	2(a)	G2 or G8
02	FLAT	2(a)	G4
03	D.I.L.	2(b)	G2 or G8
04	D.I.L.	2(b)	G4
07	CHIP CARRIER	2(c)	2
08	D.I.L.	2(d)	G2
09	D.I.L.	2(d)	G4
10	SO CERAMIC	2(e)	G2
11	SO CERAMIC	2(e)	G4

**TABLE 1(b) - MAXIMUM RATINGS**

NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	$V_{DD}$	-0.5 to +18	V	Note 1
2	Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$	V	Note 2 Power on
3	D.C. Input Current	$\pm I_{IN}$	10	mA	-
4	D.C. Output Current	$\pm I_O$	10	mA	Note 3
5	Device Dissipation	$P_D$	200	mWdc	Per Package
6	Output Dissipation	$P_{DSO}$	100	mWdc	Note 4
7	Operating Temperature Range	$T_{op}$	-55 to +125	°C	-
8	Storage Temperature Range	$T_{stg}$	-65 to +150	°C	-
9	Soldering Temperature For FP and DIP For CCP	$T_{sol}$	+300 +245	°C	Note 5 Note 6

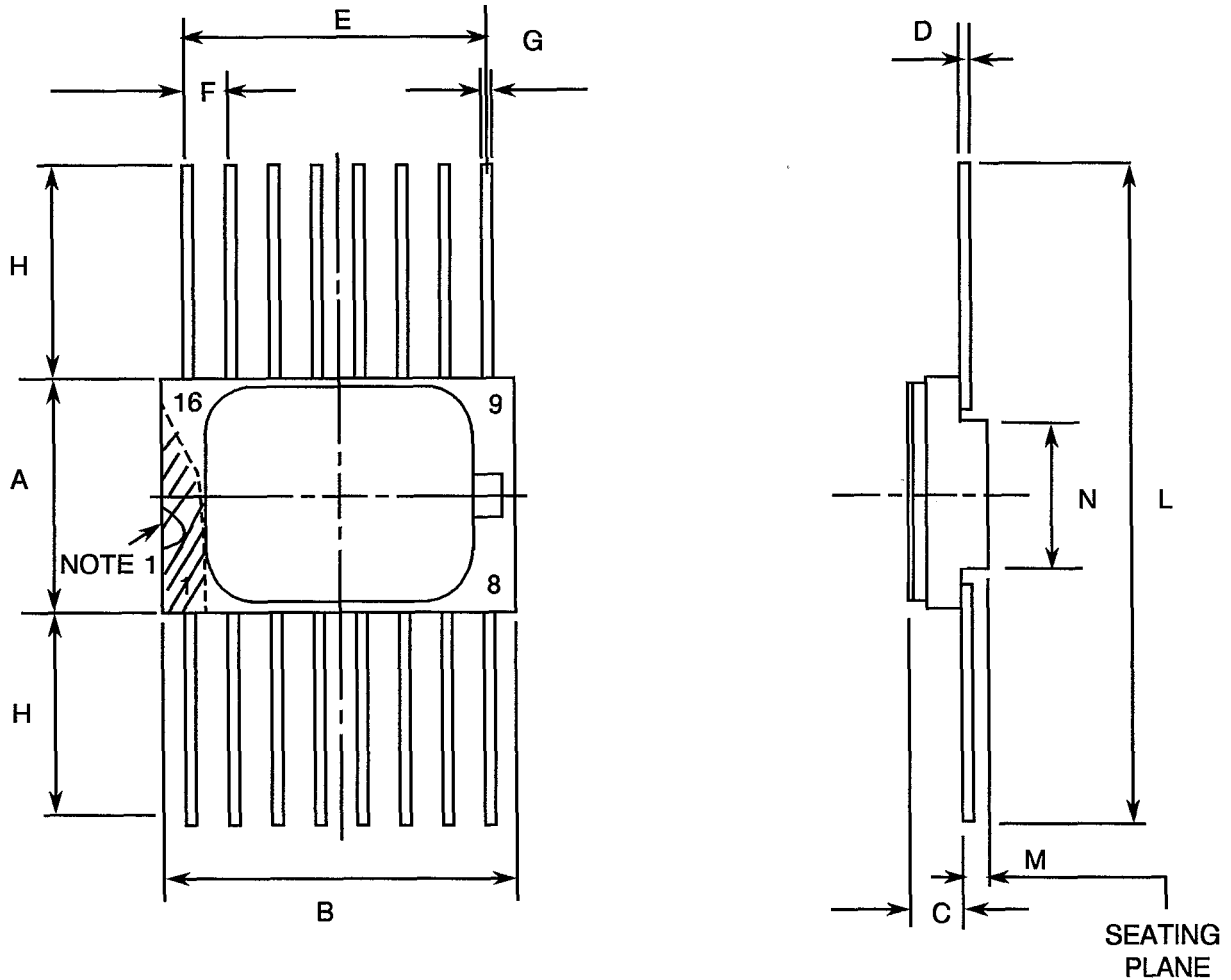
**NOTES**

- Device is functional from +3V to +15V with reference to  $V_{SS}$ .
- $V_{DD} + 0.5V$  should not exceed +18V.
- The maximum output current of any single output.
- The maximum power dissipation of any single output.
- Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
- Duration 30 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.



**FIGURE 2 - PHYSICAL DIMENSIONS**

**FIGURE 2(a) - FLAT PACKAGE, 16-PIN**



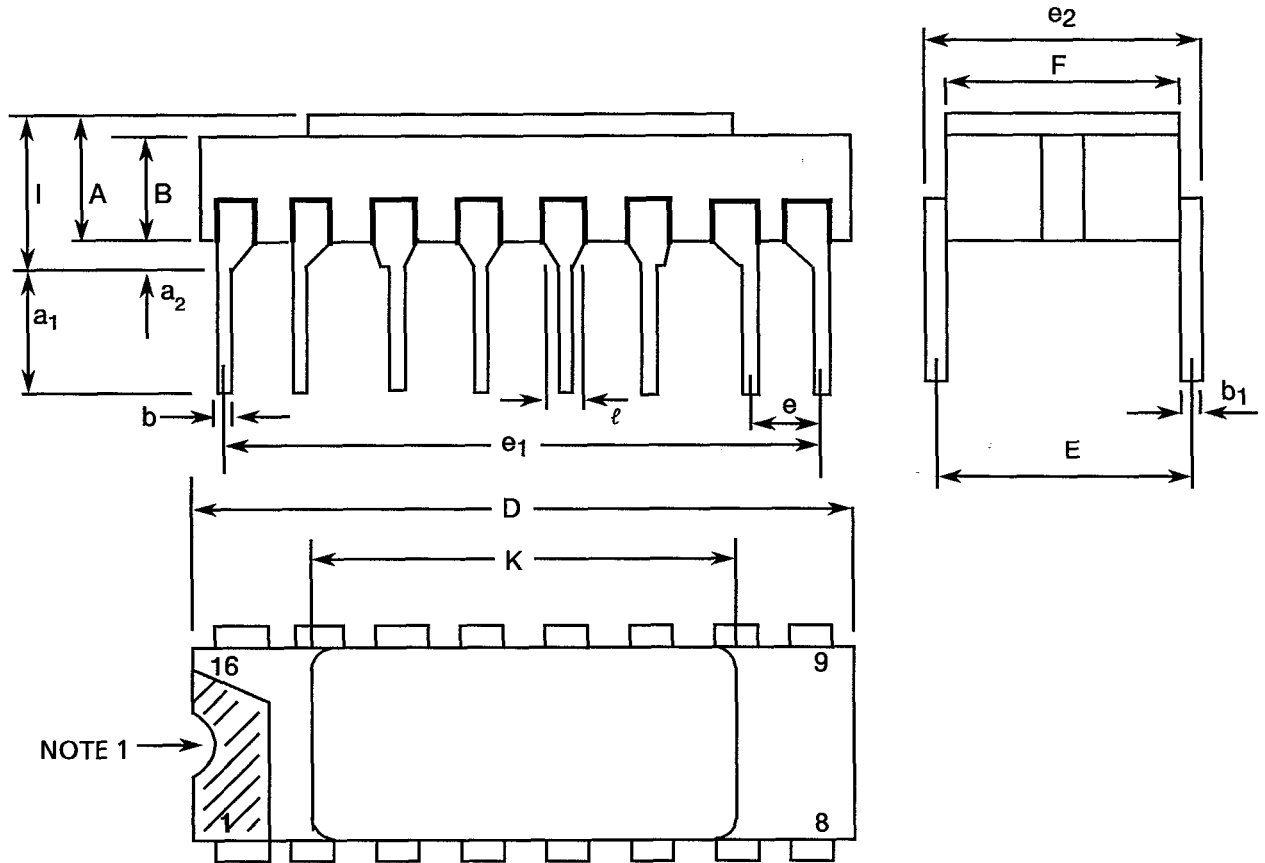
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.102	0.152	3
E	8.76	9.01	
F	1.27	TYPICAL	4
G	0.38	0.48	3
H	6.0	-	3
L	18.75	22.0	
M	0.33	0.43	
N	4.31	TYPICAL	

**NOTES:** See Page 12.



**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

**FIGURE 2(b) - DUAL-IN-LINE PACKAGE, 16-PIN**



NOTE 1 →

SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	2.10	2.54	
a <sub>1</sub>	3.0	3.7	
a <sub>2</sub>	0.63	1.14	2
B	1.82	2.23	
b	0.40	0.50	3
b <sub>1</sub>	0.20	0.30	3
D	18.79	19.20	
E	7.36	7.87	
e	2.41	2.67	4
e <sub>1</sub>	17.65	17.90	
e <sub>2</sub>	7.62	8.12	
F	7.11	7.62	
I	-	3.70	
K	10.90	12.10	
ℓ	1.27	TYPICAL	

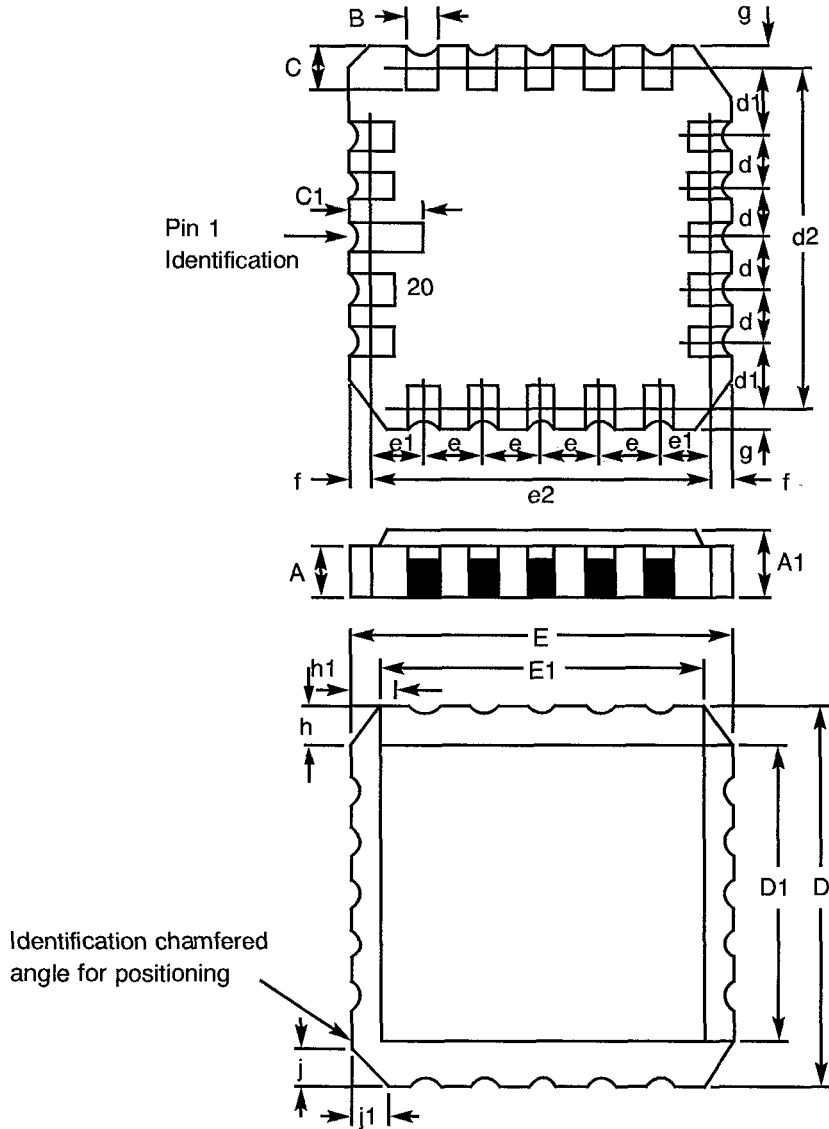
**NOTES:** See Page 12.





**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

**FIGURE 2(c) - CHIP CARRIER - 20-TERMINAL**



Identification chamfered angle for positioning

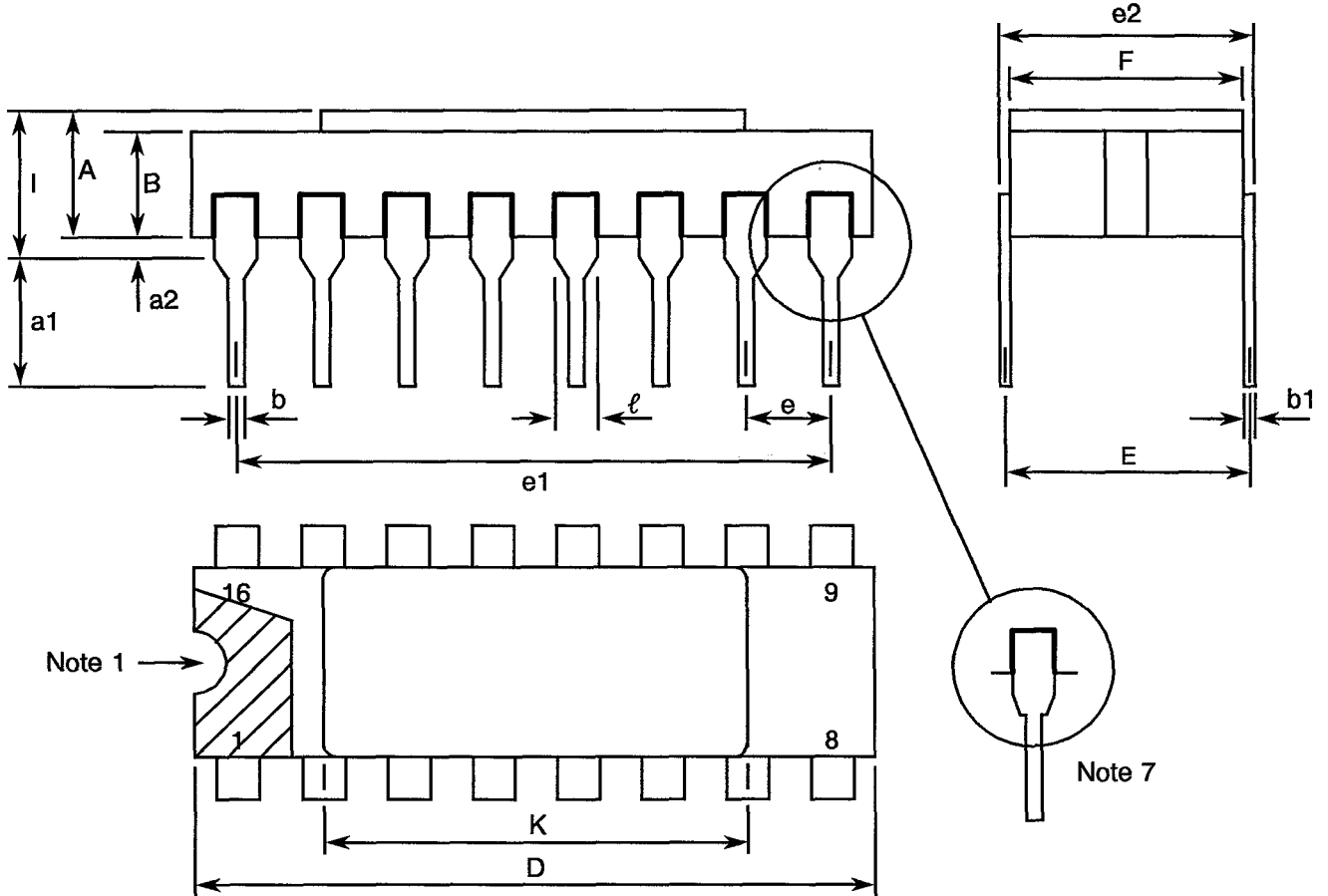
DIMENSIONS	MILLIMETRES		NOTES
	MIN	MAX	
A	1.14	1.95	
A1	1.63	2.36	
B	0.55	0.72	3
C	1.06	1.47	3
C <sub>1</sub>	1.91	2.41	
D	8.67	9.09	
D1	7.21	7.52	
d, d1	1.27	TYPICAL	4
d2	7.62	TYPICAL	
E	8.67	9.09	
E1	7.21	7.52	
e, e1	1.27	TYPICAL	4
e2	7.62	TYPICAL	
f, g	-	0.76	
h, h1	1.01	TYPICAL	6
j, j1	0.51	TYPICAL	5

**NOTES:** See Page 12.



**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

**FIGURE 2(d) - DUAL-IN-LINE PACKAGE, 16-PIN**



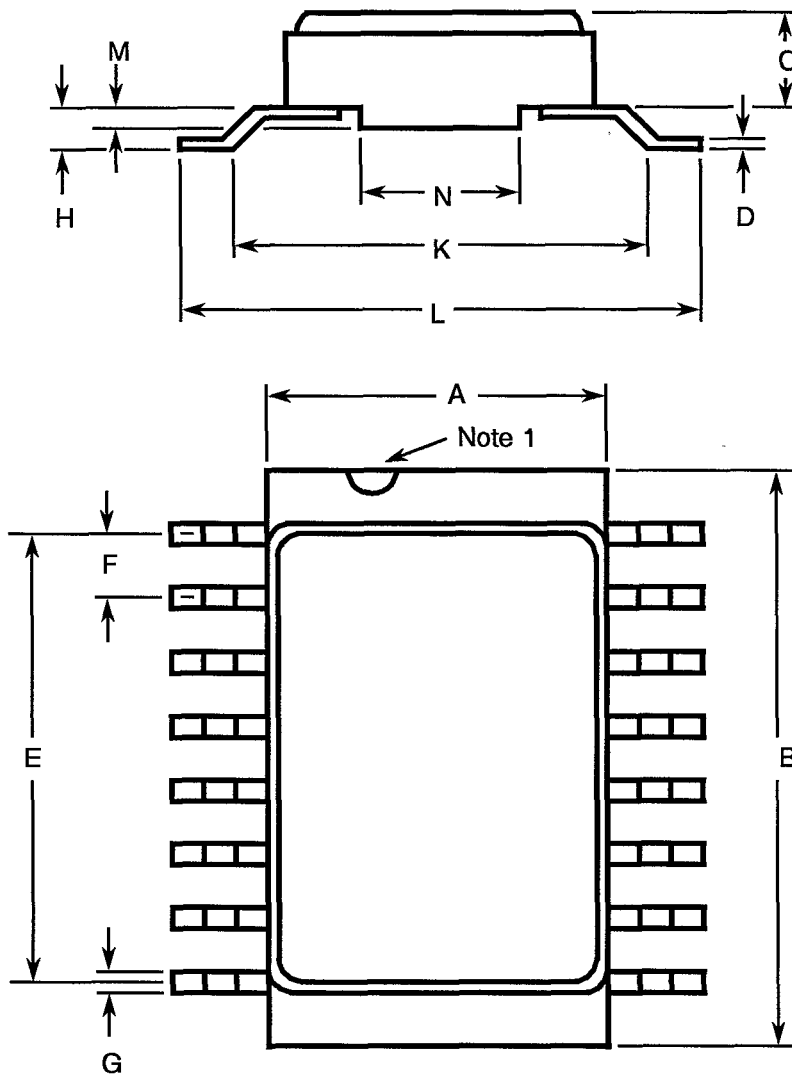
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	2.10	2.71	
a1	3.00	3.70	
a2	0.63	1.14	2
B	1.82	2.39	
b	0.40	0.50	3
b1	0.20	0.30	3
D	20.06	20.58	
E	7.36	7.87	
e	2.54 TYPICAL		4
e1	17.65	17.90	
e2	7.62	8.12	
F	7.29	7.70	
I	-	3.83	
K	10.90	12.10	
l	1.14	1.50	

**NOTES:** See Page 12.




**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

**FIGURE 2(e) - SMALL OUTLINE CERAMIC PACKAGE, 16-PIN**



SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	6.75	7.06	
B	9.76	10.14	
C	1.49	1.95	
D	0.102	0.152	3
E	8.76	9.01	
F	1.27 TYPICAL		4
G	0.38	0.48	3
H	0.60	0.90	3
K	9.00 TYPICAL		
L	10	10.65	
M	0.33	0.43	
N	4.31 TYPICAL		

**NOTES:** See Page 12.

	<p style="text-align: center;">ESA/SCC Detail Specification No. 9306/015</p>		<p>PAGE 12 ISSUE 3</p>
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**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

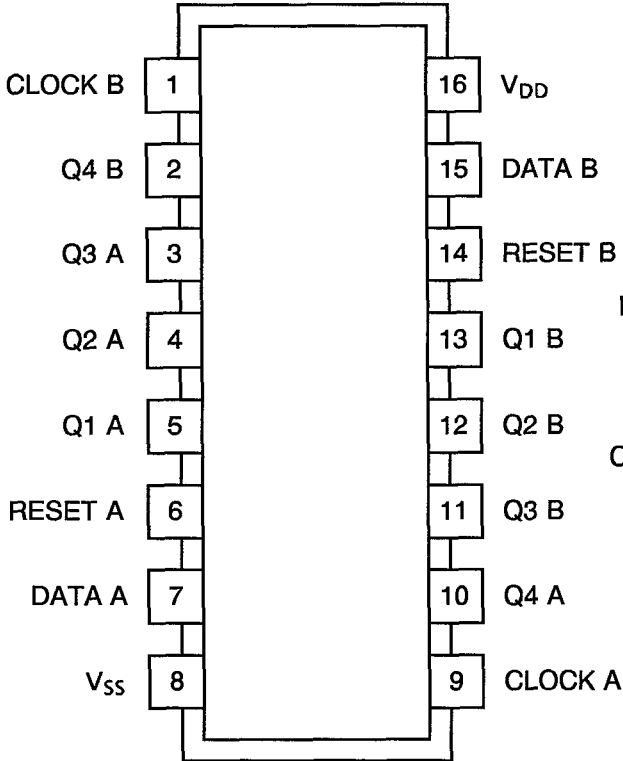
**NOTES TO FIGURES 2(a) TO 2(e) INCLUSIVE**

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(c).
2. The dimension shall be measured from the seating plane to the base plane.
3. All leads or terminals.
4. 16 pin packages : 14 spaces  
20 terminal packages : 12 spaces
5. Index corner only.
6. Three non-index corners.
7. For all pins, either pin shape may be supplied.

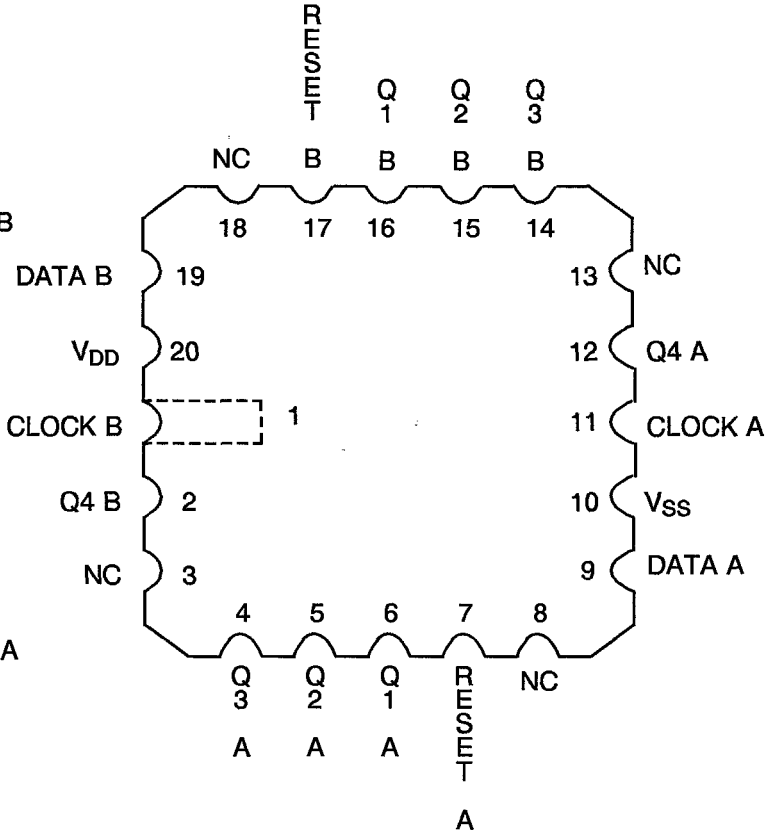
**FIGURE 3(a) - PIN ASSIGNMENT**

DUAL-IN-LINE, SO AND FLAT PACKAGES

CHIP CARRIER PACKAGE



TOP VIEW



TOP VIEW

FLAT PACKAGE, SO AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE, SO AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CHIP CARRIER PIN OUTS	1	2	4	5	6	7	9	10	11	12	14	15	16	17	19	20

**FIGURE 3(b) - TRUTH TABLE**

CL	D	R	Q <sub>1</sub>	Q <sub>n</sub>
┌	0	0	0	Q <sub>n-1</sub>
┐	1	0	1	Q <sub>n-1</sub>
└	X	0	Q <sub>1</sub>	Q <sub>n</sub> - (No. Change)
X	X	1	0	0

- NOTES**
1. Logic Level Definition: 0 = Low Level, 1 = High Level, X = Don't Care,
  2. ┌ = Positive-going transition, └ = Negative-going transition



**FIGURE 3(c) - CIRCUIT SCHEMATIC (ONE REGISTER)**

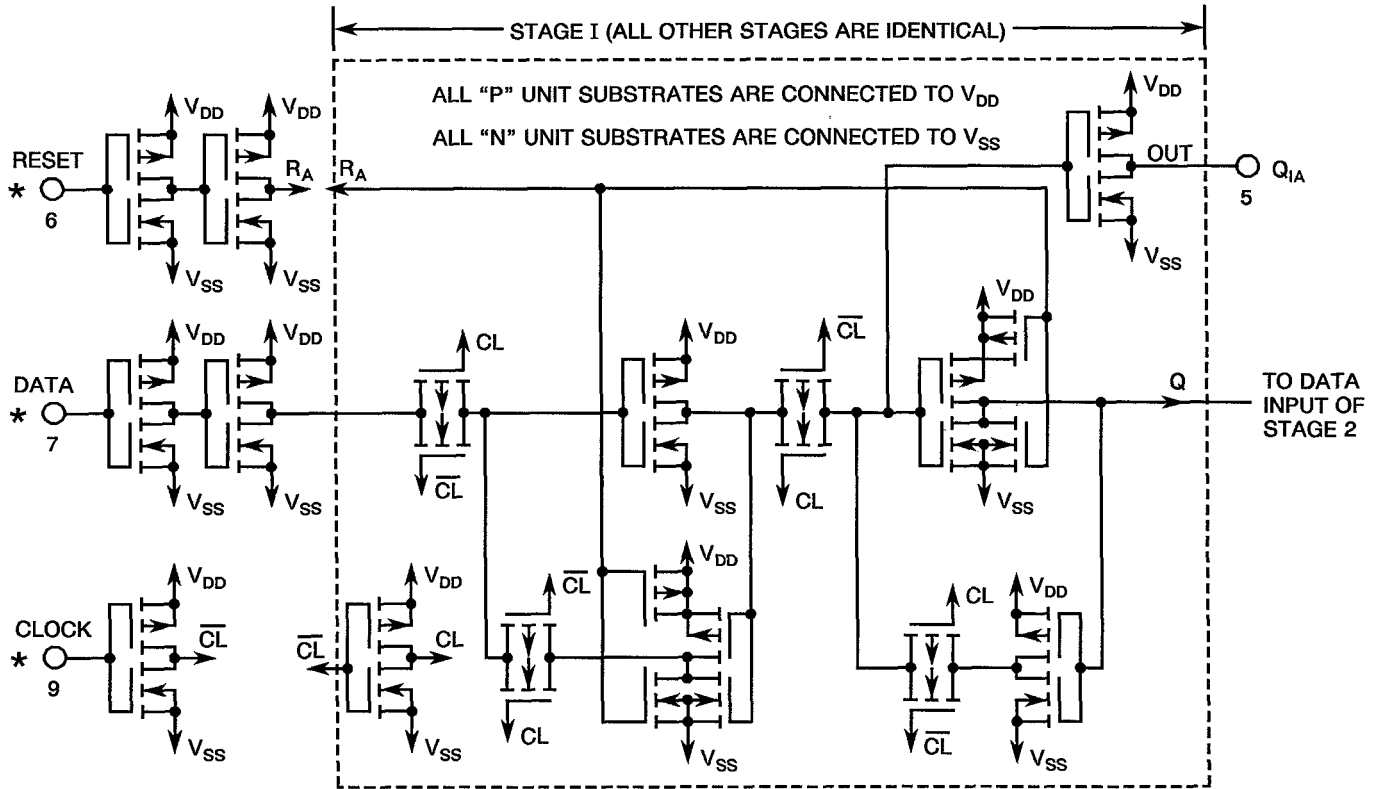
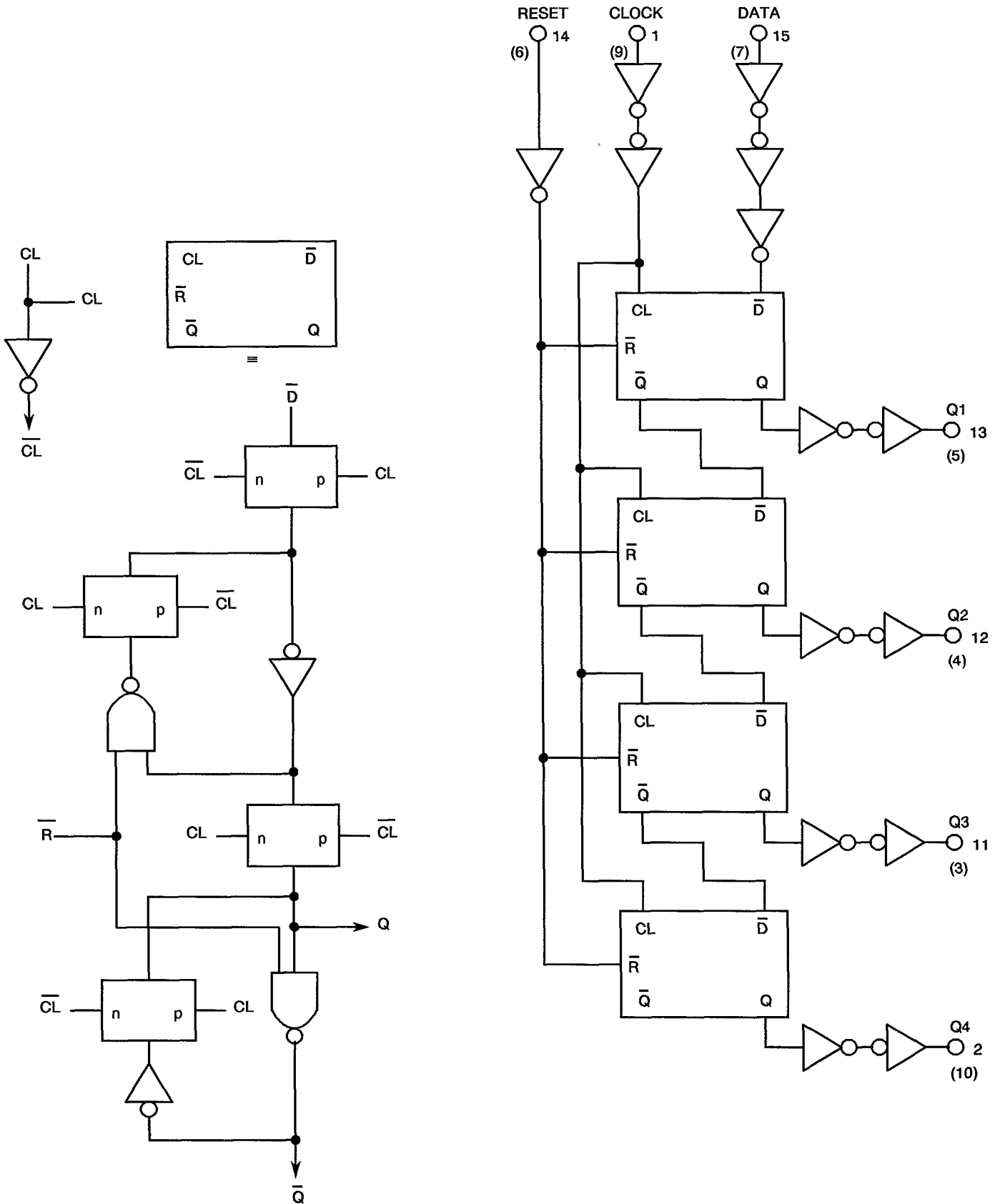


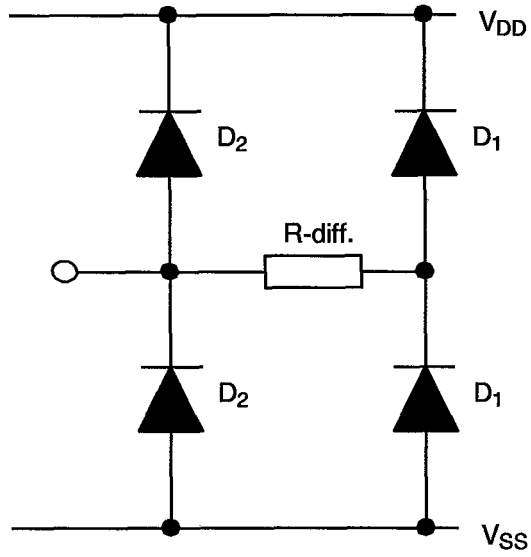


FIGURE 3(d) - FUNCTIONAL DIAGRAM (ONE REGISTER)





**FIGURE 3(e) - INPUT PROTECTION NETWORK**





**2. APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:-

- (a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

**3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

$V_{IC}$  = Input Clamp Voltage  
 $P_{DSO}$  = Single Output Power Dissipation  
CKT = Circuit

**4. REQUIREMENTS****4.1 GENERAL**

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirement and do not affect the components' reliability, are listed in the appendices attached to this specification.

**4.2 DEVIATIONS FROM GENERIC SPECIFICATION****4.2.1 Deviations from Special In-process Controls**

None.

**4.2.2 Deviations from Final Production Tests (Chart II)**

None.

**4.2.3 Deviations from Burn-in Tests (Chart III)****4.2.3.1 Deviations from High Temperature Reverse Bias (H.T.R.B.)**

Prior to operating power burn-in, a high temperature reverse bias (H.T.R.B.) screen at +125 °C shall be added for the N-Channel and then for the P-Channel in accordance with Tables 5(a) and 5(b) of this specification. Each exposure to H.T.R.B. shall be 72 hours and Table 4 Parameter Drift Values shall be applied at 0 and 144 hours.

**4.2.4 Deviations from Qualification Tests (Chart IV)**

None.



#### 4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

### 4.3 MECHANICAL REQUIREMENTS

#### 4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

#### 4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 1.5 grammes for the dual-in-line package, 0.6 grammes for the flat and SO packages and 0.52 grammes for the chip carrier package.

### 4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

#### 4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed or preform-soldered.

#### 4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with either Type '4' or Type '2 or 8' finish in accordance with ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with ESA/SCC Basic Specification No. 23500. For SO ceramic packages, the material shall be Type 'G' with either Type '2' or Type '4' finish in accordance with ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

### 4.5 MARKING

#### 4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

- (a) Lead Identification.
- (b) The SCC Component Number.
- (c) Traceability Information.

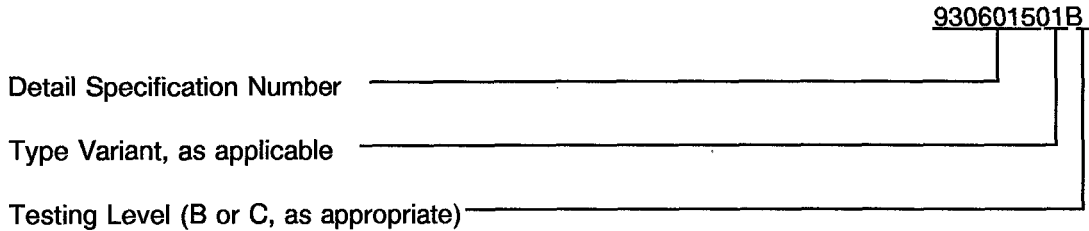
#### 4.5.2 Lead Identification

For dual-in-line, flat and SO packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).



**4.5.3 The SCC Component Number**

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



**4.5.4 Traceability Information**

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

**4.6 ELECTRICAL MEASUREMENTS**

**4.6.1 Electrical Measurements at Room Temperature**

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3 \text{ }^\circ\text{C}$ .

**4.6.2 Electrical Measurements at High and Low Temperatures**

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at  $T_{amb} = +125 (+0-5) \text{ }^\circ\text{C}$  and  $-55 (+5-0) \text{ }^\circ\text{C}$  respectively.

**4.6.3 Circuits for Electrical Measurements**

Circuits and functional test sequence for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

**4.7 BURN-IN TESTS**

**4.7.1 Parameter Drift Values**

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at  $+22 \pm 3 \text{ }^\circ\text{C}$ . The parameter drift values ( $\Delta$ ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

**4.7.2 Conditions for H.T.R.B. and Burn-in**

The requirements for H.T.R.B. and Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and Burn-in shall be as specified in Tables 5(a), 5(b) and 5(c) of this specification.

**4.7.3 Electrical Circuits for H.T.R.B and Burn-in**

Circuits for use in performing the H.T.R.B. and Burn-in tests are shown in Figures 5(a), 5(b) and 5(c) of this specification.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 3V_{dc}$ , $V_{SS} = 0V_{dc}$ Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Notes 1 and 2	-	-	-
3 to 5	Quiescent Current	$I_{DD}$	3005	4(b)	$V_{IL} = 0V_{dc}$ , $V_{IH} = 15V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 3 (Pin D/F 16) (Pin C 20)	-	1.0	$\mu A$
6 to 11	Input Current Low Level	$I_{IL}$	3009	4(c)	$V_{IN}$ (Under Test) = $0V_{dc}$ All Other Inputs: $V_{IN} = 15V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	-50	nA
12 to 17	Input Current High Level	$I_{IH}$	3010	4(d)	$V_{IN}$ (Under Test) = $15V_{dc}$ All Other Inputs: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	50	nA
18 to 25	Output Voltage Low Level	$V_{OL}$	3007	4(e)	Register Under Test: Reset Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = \text{Open}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-	0.05	V

**NOTES:** See Page 25.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
26 to 33	Output Voltage High Level	$V_{OH}$	3006	4(f)	Register Under Test: Clock Input = Pulse Generator Data Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = \text{Open}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	14.95	-	V
34 to 41	Output Drive Current N-Channel	$I_{OL1}$	-	4(g)	Register Under Test: Reset Input: $V_{IN} = 5V_{dc}$ Remaining Inputs: $V_{IN} = 0V_{dc}$ $V_{OUT} = 0.4V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 5V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	0.51	-	mA
42 to 49	Output Drive Current N-Channel	$I_{OL2}$	-	4(g)	Register Under Test: Reset Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IN} = 0V_{dc}$ $V_{OUT} = 1.5V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	3.4	-	mA

**NOTES:** See Page 25.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
50 to 57	Output Drive Current P-Channel	$I_{OH1}$	-	4(h)	Register Under Test: Clock Input = Pulse Generator Data Input: $V_{IH} = 5V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = 4.6V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 5V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-0.51	-	mA
58 to 65	Output Drive Current P-Channel	$I_{OH2}$	-	4(h)	Register Under Test: Clock Input = Pulse Generator Data Input: $V_{IH} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = 13.5V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-3.4	-	mA
66	Input Voltage Low Level (Noise Immunity) (Functional Test)	$V_{IL1}$	-	4 (a)	$V_{IL} = 1.5V_{dc}$ $V_{IH} = 3.5V_{dc}$ $V_{DD} = 5V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 5 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	$V_{IH1}$	-			-	0.5	
67	Input Voltage Low Level (Noise Immunity) (Functional Test)	$V_{IL2}$	-	4 (a)	$V_{IL} = 4V_{dc}$ $V_{IH} = 11V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 5 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	$V_{IH2}$	-			-	1.5	

**NOTES:** See Page 25.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
68	Threshold Voltage N-Channel	$V_{THN}$	-	4(i)	Reset A Input at Ground All Other Inputs: $V_{IN} = 5V_{dc}$ $V_{DD} = 5V_{dc}$ , $I_{SS} = -10\mu A$ (Pin D/F 8) (Pin C 10)	-0.7	-3.0	V
69	Threshold Voltage P-Channel	$V_{THP}$	-	4(j)	Reset A Input at Ground All Other Inputs: $V_{IN} = -5V_{dc}$ $V_{SS} = -5V_{dc}$ , $I_{DD} = 10\mu A$ (Pin D/F 16) (Pin C 20)	0.7	3.0	V
70 to 75	Input Clamp Voltage (to $V_{SS}$ )	$V_{IC1}$	-	4(k)	$I_{IN}$ (Under Test) = $-100\mu A$ $V_{DD} = \text{Open}$ , $V_{SS} = 0V_{dc}$ All Other Pins Open (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	-2.0	V
76 to 81	Input Clamp Voltage (to $V_{DD}$ )	$V_{IC2}$	-	4(l)	$V_{IN}$ (Under Test) = $6V_{dc}$ $V_{SS} = \text{Open}$ , $R = 30K\Omega$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	3.0	-	V

**NOTES:** See Page 25.




**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
82 to 87	Input Capacitance	$C_{IN}$	3012	4(m)	$V_{IN}$ (Not Under Test) = 0Vdc $V_{DD} = V_{SS} = 0Vdc$ Note 6 (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	7.5	pF
88	Propagation Delay Low to High	$t_{PLH}$	3003	4(n)	$V_{IN}$ (Under Test) = Pulse Generator Reset Input: $V_{IN} = 0Vdc$ $V_{IN}$ (All Other Inputs) = 5Vdc $V_{DD} = 5Vdc, V_{SS} = 0Vdc$ Notes 7 and 8 <u>Pins D/F</u> <u>Pins C</u> 9 to 4        11 to 5	-	270	ns
89	Propagation Delay High to Low	$t_{PHL}$	3003	4(n)	$V_{IN}$ (Under Test) = Pulse Generator Reset Input: $V_{IN} = 0Vdc$ $V_{IN}$ (All Other Inputs) = 5Vdc $V_{DD} = 5Vdc, V_{SS} = 0Vdc$ Notes 7 and 8 <u>Pins D/F</u> <u>Pins C</u> 9 to 4        11 to 5	-	270	ns
90	Transition Time Low to High	$t_{TLH}$	3004	4(n)	$V_{IN}$ (Reset) = Pulse Generator $V_{IN}$ (All Other Inputs) = 5Vdc $V_{DD} = 5Vdc, V_{SS} = 0Vdc$ Note 7 (Pin D/F 4) (Pin C 5)	-	150	ns
91	Transition Time High to Low	$t_{THL}$	3004	4(n)	$V_{IN}$ (Reset) = Pulse Generator $V_{IN}$ (All Other Inputs) = 5Vdc $V_{DD} = 5Vdc, V_{SS} = 0Vdc$ Note 7 (Pin D/F 4) (Pin C 5)	-	150	ns
92	Maximum Clock Frequency	$f_{(CL)}$	-	-	Clock = Pulse Generator $V_{DD} = 5Vdc, V_{SS} = 0Vdc$ Notes 7 and 9 (Pin D/F 9) (Pin C 11)	3.0	-	MHz

**NOTES:** See Page 25.



	<p style="text-align: center;">ESA/SCC Detail Specification No. 9306/015</p>		<p>PAGE 25 ISSUE 3</p>
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**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONTINUED)**

**NOTES**

1. GO-NO-GO Test, each pattern of Test Table 4 (a).  
 $V_{OH} \geq V_{DD} - 0.5V_{dc}$      $V_{OL} \leq 0.5V_{dc}$ .
2. Maximum time to output comparator strobe 300 $\mu$ sec.
3. Test each pattern of Table 4(b).
4. Interchange of forcing and measuring function is permitted.
5. This is performed as a Functional Test in which extreme  $V_{IN}$  conditions are applied and output voltage is measured.
6. Measurement performed on a sample basis, LTPD7 or less, with a Capacitance Bridge connected between each input under test and  $V_{SS}$ , only for Lots where LAT Level 2 is to be performed. (For LTPD sampling plan, see Annexe I of ESA/SCC 9000).
7. Measurement performed on a sample basis, LTPD7 or less (see Annexe I of ESA/SCC 9000).
8. Before commencement of test, load all stages with low or high in accordance with Figure 4(a) and measure propagation time at change.
9. A pulse, having the following conditions, shall be applied to the Clock Input:  $V_P = 0V_{dc}$  to  $V_{DD}$  Vdc. Maximum clock frequency  $f_{(CL)}$  requirement is considered met if proper output state changes occur with the pulse repetition rate set to that given in the "Limits" column.

**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 3V_{dc}$ , $V_{SS} = 0V_{dc}$ Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Notes 1 and 2	-	-	-
3 to 5	Quiescent Current	$I_{DD}$	3005	4(b)	$V_{IL} = 0V_{dc}$ , $V_{IH} = 15V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 3 (Pin D/F 16) (Pin C 20)	-	30	$\mu A$
6 to 11	Input Current Low Level	$I_{IL}$	3009	4(c)	$V_{IN}$ (Under Test) = $0V_{dc}$ All Other Inputs: $V_{IN} = 15V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	-100	nA
12 to 17	Input Current High Level	$I_{IH}$	3010	4(d)	$V_{IN}$ (Under Test) = $15V_{dc}$ All Other Inputs: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	100	nA
18 to 25	Output Voltage Low Level	$V_{OL}$	3007	4(e)	Register Under Test: Reset Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = \text{Open}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-	0.05	V

**NOTES:** See Page 25.

**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
26 to 33	Output Voltage High Level	$V_{OH}$	3006	4(f)	Register Under Test: Clock Input = Pulse Generator Data Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = \text{Open}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	14.95	-	V
34 to 41	Output Drive Current N-Channel	$I_{OL1}$	-	4(g)	Register Under Test: Reset Input: $V_{IN} = 5V_{dc}$ Remaining Inputs: $V_{IN} = 0V_{dc}$ $V_{OUT} = 0.4V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 5V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	0.36	-	mA
42 to 49	Output Drive Current N-Channel	$I_{OL2}$	-	4(g)	Register Under Test: Reset Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IN} = 0V_{dc}$ $V_{OUT} = 1.5V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	2.4	-	mA

**NOTES:** See Page 25.



**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
50 to 57	Output Drive Current P-Channel	I <sub>OH1</sub>	-	4(h)	Register Under Test: Clock Input = Pulse Generator Data Input: V <sub>IH</sub> = 5Vdc Remaining Inputs: V <sub>IL</sub> = 0Vdc V <sub>OUT</sub> = 4.6Vdc Other Register: V <sub>IN</sub> = 0Vdc V <sub>DD</sub> = 5Vdc, V <sub>SS</sub> = 0Vdc Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-0.36	-	mA
58 to 65	Output Drive Current P-Channel	I <sub>OH2</sub>	-	4(h)	Register Under Test: Clock Input = Pulse Generator Data Input: V <sub>IH</sub> = 15Vdc Remaining Inputs: V <sub>IL</sub> = 0Vdc V <sub>OUT</sub> = 13.5Vdc Other Register: V <sub>IN</sub> = 0Vdc V <sub>DD</sub> = 5Vdc, V <sub>SS</sub> = 0Vdc Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-2.4	-	mA
66	Input Voltage Low Level (Noise Immunity) (Functional Test)	V <sub>IL1</sub>	-	4(a)	V <sub>IL</sub> = 1.5Vdc V <sub>IH</sub> = 3.5Vdc V <sub>DD</sub> = 15Vdc, V <sub>SS</sub> = 0Vdc Note 5 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V <sub>IH1</sub>	-			-	0.5	
67	Input Voltage Low Level (Noise Immunity) (Functional Test)	V <sub>IL2</sub>	-	4(a)	V <sub>IL</sub> = 4Vdc V <sub>IH</sub> = 11Vdc V <sub>DD</sub> = 15Vdc, V <sub>SS</sub> = 0Vdc Note 5 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V <sub>IH2</sub>	-			-	1.5	

**NOTES:** See Page 25.

**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0-5) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
68	Threshold Voltage N-Channel	$V_{THN}$	-	4(i)	Reset A Input at Ground All Other Inputs: $V_{IN} = 5V_{dc}$ $V_{DD} = 5V_{dc}$ , $I_{SS} = -10\mu A$ (Pin D/F 8) (Pin C 10)	-0.3	-3.5	V
69	Threshold Voltage P-Channel	$V_{THP}$	-	4(j)	Reset A Input at Ground All Other Inputs: $V_{IN} = -5V_{dc}$ $V_{SS} = -5V_{dc}$ , $I_{DD} = 10\mu A$ (Pin D/F 16) (Pin C 20)	0.3	3.5	V

**NOTES:** See Page 25.

**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 3V_{dc}$ , $V_{SS} = 0V_{dc}$ Notes 1 and 2	-	-	-
2	Functional Test	-	-	4(a)	Verify Truth Table without Load. $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Notes 1 and 2	-	-	-
3 to 5	Quiescent Current	$I_{DD}$	3005	4(b)	$V_{IL} = 0V_{dc}$ , $V_{IH} = 15V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 3 (Pin D/F 16) (Pin C 20)	-	1.0	$\mu A$
6 to 11	Input Current Low Level	$I_{IL}$	3009	4(c)	$V_{IN}$ (Under Test) = $0V_{dc}$ All Other Inputs: $V_{IN} = 15V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	-50	nA
12 to 17	Input Current High Level	$I_{IH}$	3010	4(d)	$V_{IN}$ (Under Test) = $15V_{dc}$ All Other Inputs: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	-	50	nA
18 to 25	Output Voltage Low Level	$V_{OL}$	3007	4(e)	Register Under Test: Reset Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = \text{Open}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-	0.05	V

**NOTES:** See Page 25.



**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
26 to 33	Output Voltage High Level	$V_{OH}$	3006	4(f)	Register Under Test: Clock Input = Pulse Generator Data Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IL} = 0V_{dc}$ $V_{OUT} = \text{Open}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	14.95	-	V
34 to 41	Output Drive Current N-Channel	$I_{OL1}$	-	4(g)	Register Under Test: Reset Input: $V_{IN} = 5V_{dc}$ Remaining Inputs: $V_{IN} = 0V_{dc}$ $V_{OUT} = 0.4V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 5V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	0.64	-	mA
42 to 49	Output Drive Current N-Channel	$I_{OL2}$	-	4(g)	Register Under Test: Reset Input: $V_{IN} = 15V_{dc}$ Remaining Inputs: $V_{IN} = 0V_{dc}$ $V_{OUT} = 1.5V_{dc}$ Other Register: $V_{IN} = 0V_{dc}$ $V_{DD} = 15V_{dc}$ , $V_{SS} = 0V_{dc}$ Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	4.2	-	mA

**NOTES:** See Page 25.



**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
50 to 57	Output Drive Current P-Channel	I <sub>OH1</sub>	-	4(h)	Register Under Test: Clock Input = Pulse Generator Data Input: V <sub>IH</sub> = 5Vdc Remaining Inputs: V <sub>IL</sub> = 0Vdc V <sub>OUT</sub> = 4.6Vdc Other Register: V <sub>IN</sub> = 0Vdc V <sub>DD</sub> = 5Vdc, V <sub>SS</sub> = 0Vdc Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-0.64	-	mA
58 to 65	Output Drive Current P-Channel	I <sub>OH2</sub>	-	4(h)	Register Under Test: Clock Input = Pulse Generator Data Input: V <sub>IH</sub> = 15Vdc Remaining Inputs: V <sub>IL</sub> = 0Vdc V <sub>OUT</sub> = 13.5Vdc Other Register: V <sub>IN</sub> = 0Vdc V <sub>DD</sub> = 15Vdc, V <sub>SS</sub> = 0Vdc Note 4 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	-4.2	-	mA
66	Input Voltage Low Level (Noise Immunity) (Functional Test)	V <sub>IL1</sub>	-	4 (a)	V <sub>IL</sub> = 1.5Vdc V <sub>IH</sub> = 3.5Vdc V <sub>DD</sub> = 5Vdc, V <sub>SS</sub> = 0Vdc Note 5 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V <sub>IH1</sub>	-			-	0.5	
67	Input Voltage Low Level (Noise Immunity) (Functional Test)	V <sub>IL2</sub>	-	4 (a)	V <sub>IL</sub> = 4Vdc V <sub>IH</sub> = 11Vdc V <sub>DD</sub> = 15Vdc, V <sub>SS</sub> = 0Vdc Note 5 (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	13.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	V <sub>IH2</sub>	-			-	1.5	

**NOTES:** See Page 25.





**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, -55(+5-0) °C (CONT'D)**

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
68	Threshold Voltage N-Channel	$V_{THN}$	-	4(i)	Reset A Input at Ground All Other Inputs: $V_{IN} = 5V_{dc}$ $V_{DD} = 5V_{dc}$ , $I_{SS} = -10\mu A$ (Pin D/F 8) (Pin C 10)	-0.7	-3.5	V
69	Threshold Voltage P-Channel	$V_{THP}$	-	4(j)	Reset A Input at Ground All Other Inputs: $V_{IN} = -5V_{dc}$ $V_{SS} = -5V_{dc}$ , $I_{DD} = 10\mu A$ (Pin D/F 16) (Pin C 20)	0.7	3.5	V

**NOTES:** See Page 25.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS**

**FIGURE 4(a) - FUNCTIONAL TEST TABLE**

PATTERN NO.	PIN NUMBERS														D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11	12	13	14	15	8	16
1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	V <sub>DD</sub>
2	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	↓
3	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	↓
4	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	↓
5	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	↓
6	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	↓
7	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	↓
8	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	↓
9	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	↓
10	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	↓
11	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	↓
12	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	↓
13	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	↓
14	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	↓
15	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	↓
16	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	↓
17	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	↓
18	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	↓
19	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	↓
20	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	↓
21	1	0	0	0	0	0	0	1	0	0	0	1	0	1	↓	
22	1	0	0	0	0	0	0	1	0	0	0	1	0	0	↓	
23	0	0	0	0	0	0	0	1	0	0	0	1	0	0	↓	
24	1	0	0	0	0	0	0	1	0	0	1	0	0	0	↓	
25	0	0	0	0	0	0	0	1	0	0	1	0	0	0	↓	
26	1	0	0	0	0	0	0	1	0	1	0	0	0	0	↓	
27	0	0	0	0	0	0	0	1	0	1	0	0	0	0	↓	
28	1	1	0	0	0	0	0	1	0	0	0	0	0	0	↓	
29	0	1	0	0	0	0	0	1	0	0	0	0	0	0	↓	
30	1	0	0	0	0	0	0	1	0	0	0	0	0	0	↓	
31	1	0	0	0	0	0	0	1	0	0	0	0	0	1	↓	
32	0	0	0	0	0	0	0	1	0	0	0	0	0	1	↓	
33	1	0	0	0	0	0	0	1	0	0	0	1	0	1	↓	
34	0	0	0	0	0	0	0	1	0	0	0	1	0	1	↓	
35	1	0	0	0	0	0	0	1	0	0	1	1	0	1	↓	
36	0	0	0	0	0	0	0	1	0	0	1	1	0	1	↓	
37	1	0	0	0	0	0	0	1	0	1	1	1	0	1	↓	
38	0	0	0	0	0	0	0	1	0	1	1	1	0	1	↓	
39	1	1	0	0	0	0	0	1	0	1	1	1	0	1	↓	
40	1	1	0	0	0	0	0	1	0	1	1	1	0	1	↓	
41	1	1	0	0	0	0	1	1	0	1	1	1	0	1	↓	
42	1	1	0	0	0	0	1	0	0	1	1	1	0	1	↓	
43	1	1	0	0	1	0	1	1	0	1	1	1	0	1	↓	
44	1	1	0	0	1	0	1	0	0	1	1	1	0	1	↓	
45	1	1	0	1	1	0	1	1	0	1	1	1	0	1	↓	

**NOTES:** See Page 36.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

FIGURE 4(a) - FUNCTIONAL TEST TABLE (CONTINUED)

PATTERN NO.	PIN NUMBERS														D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11	12	13	14	15	8	16
46	1	1	0	1	1	0	1	0	0	1	1	1	0	1	0	V <sub>DD</sub>
47	1	1	1	1	1	0	1	1	0	1	1	1	0	1		
48	1	1	1	1	1	0	1	0	0	1	1	1	0	1		
49	1	1	1	1	1	0	1	1	1	1	1	1	0	1		
50	1	1	1	1	1	0	0	1	1	1	1	1	0	1		
51	1	1	1	1	1	0	0	0	1	1	1	1	0	1		
52	1	1	1	1	0	0	0	1	1	1	1	1	0	1		
53	1	1	1	1	0	0	1	1	1	1	1	1	0	1		
54	1	1	1	1	0	0	1	0	1	1	1	1	0	1		
55	1	1	1	0	1	0	1	1	1	1	1	1	0	1		
56	1	1	1	0	1	0	1	0	1	1	1	1	0	1		
57	1	1	0	1	1	0	1	1	1	1	1	1	0	1		
58	1	1	0	1	1	0	1	0	1	1	1	1	0	1		
59	1	1	1	1	1	0	1	1	0	1	1	1	0	1		
60	1	1	1	1	1	0	1	0	0	1	1	1	0	1		
61	1	1	1	1	1	0	1	1	1	1	1	1	0	1		
62	1	1	1	1	1	0	1	1	1	1	1	1	0	0		
63	0	1	1	1	1	0	1	1	1	1	1	1	0	0		
64	1	1	1	1	1	0	1	1	1	1	1	0	0	0		
65	1	1	1	1	1	0	1	1	1	1	1	0	0	1		
66	0	1	1	1	1	0	1	1	1	1	1	0	0	1		
67	1	1	1	1	1	0	1	1	1	1	0	1	0	1		
68	0	1	1	1	1	0	1	1	1	1	0	1	0	1		
69	1	1	1	1	1	0	1	1	1	0	1	1	0	1		
70	0	1	1	1	1	0	1	1	1	0	1	1	0	1		
71	1	0	1	1	1	0	1	1	1	1	1	1	0	1		
72	0	0	1	1	1	0	1	1	1	1	1	1	0	1		
73	1	1	1	1	1	0	1	1	1	1	1	1	0	1		
74	1	1	0	0	0	1	1	1	0	1	1	1	0	1		
75	1	1	0	0	0	0	1	1	0	1	1	1	0	1		
76	1	0	0	0	0	0	1	1	0	0	0	0	1	1		
77	1	0	0	0	0	0	1	1	0	0	0	0	0	1		
78	0	0	0	0	0	0	1	1	0	0	0	0	0	1		
79	1	0	0	0	0	0	1	1	0	0	0	1	0	1		
80	0	0	0	0	0	0	1	1	0	0	0	1	0	1		
81	1	0	0	0	0	0	1	1	0	0	1	1	0	1		
82	0	0	0	0	0	0	1	1	0	0	1	1	0	1		
83	1	0	0	0	0	0	1	1	0	1	1	1	0	1		
84	0	0	0	0	0	0	1	1	0	1	1	1	0	1		
85	1	1	0	0	0	0	1	1	0	1	1	1	0	1		
86	0	1	0	0	0	0	1	1	0	1	1	1	0	1		
87	0	0	0	0	0	0	1	0	0	0	0	0	1	1		
88	0	0	0	0	0	0	1	0	0	0	0	0	0	1		
89	0	0	0	0	0	0	1	0	0	0	0	0	0	1		
90	0	0	0	0	1	0	1	1	0	0	0	0	0	1		

**NOTES:** See Page 36.

**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

FIGURE 4(a) - FUNCTIONAL TEST TABLE (CONTINUED)

PATTERN NO.	PIN NUMBERS														D.C. SUPPLY	
	1	2	3	4	5	6	7	9	10	11	12	13	14	15	8	16
91	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	V <sub>DD</sub>
92	0	0	0	1	1	0	1	1	0	0	0	0	0	1	↓	↓
93	0	0	0	1	1	0	1	0	0	0	0	0	0	1	↓	↓
94	0	0	1	1	1	0	1	1	0	0	0	0	0	1	↓	↓
95	0	0	1	1	1	0	1	0	0	0	0	0	0	1	↓	↓
96	0	0	1	1	1	0	1	1	1	0	0	0	0	1	↓	↓
97	0	0	1	1	1	0	1	0	1	0	0	0	0	1	↓	↓
98	0	0	0	0	0	1	1	0	0	0	0	0	0	1	↓	↓
99	0	0	0	0	0	0	1	0	0	0	0	0	0	1	↓	↓
100	0	0	0	0	0	1	1	0	0	0	0	0	1	1	↓	↓
101	1	0	0	0	0	1	1	1	0	0	0	0	1	1	↓	↓
102	1	0	0	0	0	0	1	1	0	0	0	0	0	1	↓	↓
103	0	0	0	0	0	0	1	0	0	0	0	0	0	1	↓	↓
104	1	0	0	0	1	0	1	1	0	0	0	1	0	1	↓	↓
105	0	0	0	0	1	0	1	0	0	0	0	1	0	1	↓	↓
106	1	0	0	1	1	0	1	1	0	0	1	1	0	1	↓	↓
107	0	0	0	1	1	0	1	0	0	0	1	1	0	1	↓	↓
108	1	0	1	1	1	0	1	1	0	1	1	1	0	1	↓	↓
109	0	0	1	1	1	0	1	0	0	1	1	1	0	1	↓	↓
110	1	1	1	1	1	0	1	1	1	1	1	1	0	1	↓	↓

- NOTES**
- Figure 4(a) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
  - Logic Level Definitions: 1 = V<sub>IH</sub> = V<sub>DD</sub>, 0 = V<sub>IL</sub> = V<sub>SS</sub>.

FIGURE 4(b) - QUIESCENT CURRENT TEST TABLE

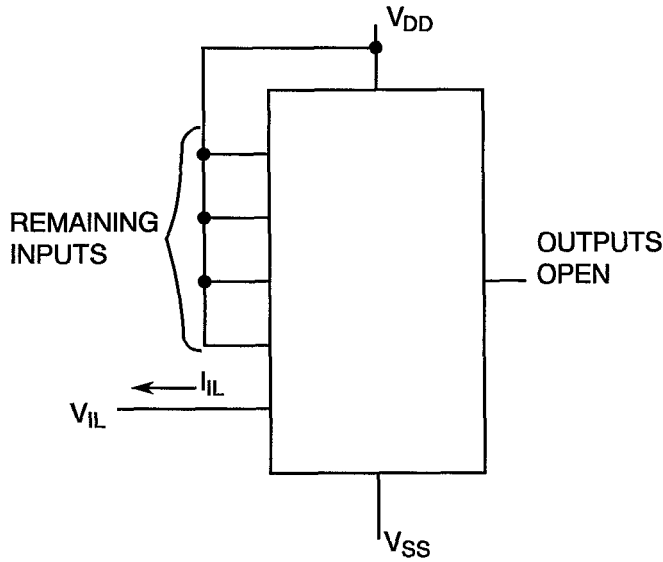
PATTERN NO.	PIN NUMBERS												D.C. SUPPLY			
	INPUTS						OUTPUTS						8	16		
	1	6	7	9	14	15	2	3	4	5	10	11			12	13
1	0	1	0	0	1	0	X	X	X	X	X	X	X	X	V <sub>SS</sub>	V <sub>DD</sub>
2	1	0	1	1	0	1	X	X	X	X	X	X	X	X	↓	↓
3	1	0	0	1	0	0	X	X	X	X	X	X	X	X	↓	↓

- NOTES**
- Figure 4(b) illustrates one series of Test Patterns. Any other pattern series must be agreed with the Qualifying Space Agency and shall be included as an Appendix.
  - Logic Level Definitions: 1 = V<sub>IH</sub> = V<sub>DD</sub>, 0 = V<sub>IL</sub> = V<sub>SS</sub>, X = Don't Care.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

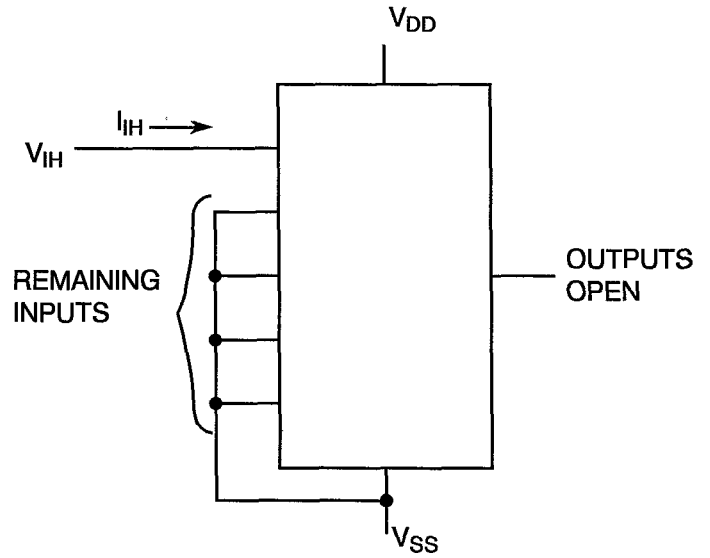
**FIGURE 4(c) - INPUT CURRENT LOW LEVEL**



**NOTES**

1. Each input to be tested separately.

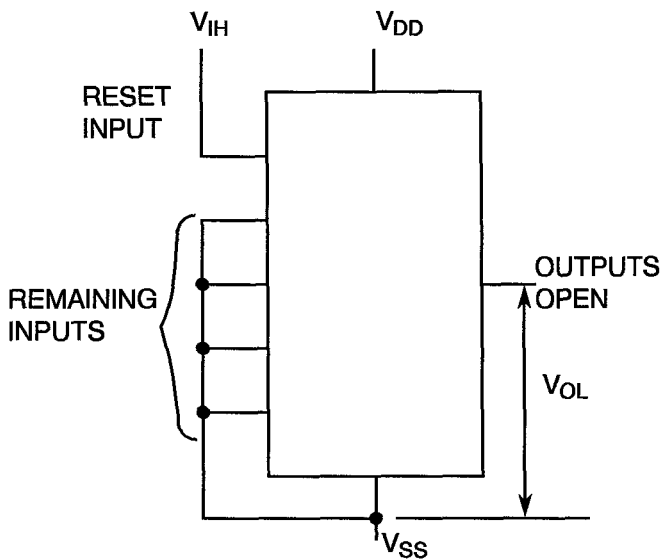
**FIGURE 4(d) - INPUT CURRENT HIGH LEVEL**



**NOTES**

1. Each input to be tested separately.

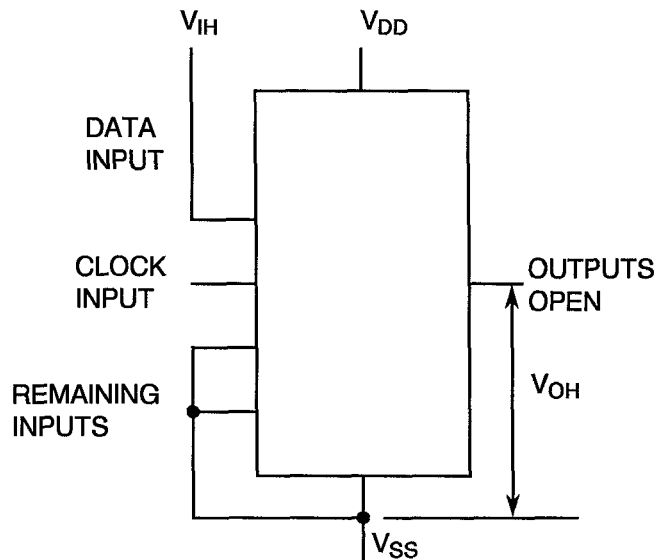
**FIGURE 4(e) - OUTPUT VOLTAGE LOW LEVEL**



**NOTES**

1. Each output to be tested separately.

**FIGURE 4(f) - OUTPUT VOLTAGE HIGH LEVEL**



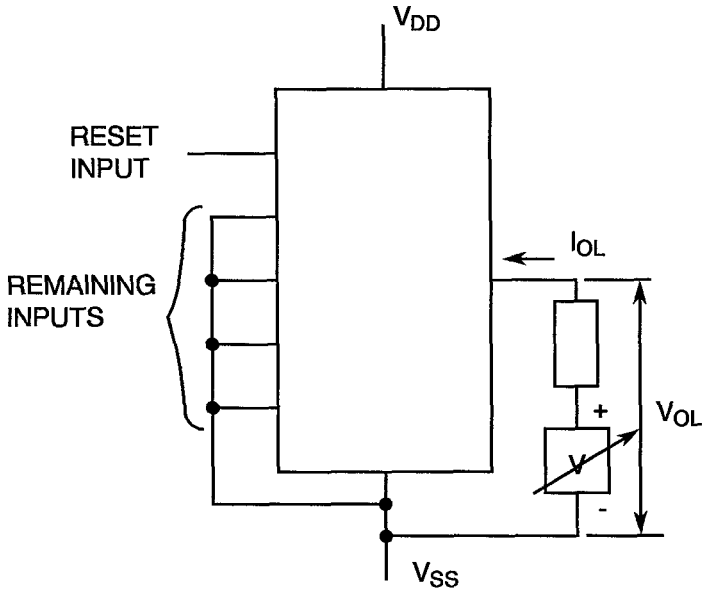
**NOTES**

1. Each output to be tested separately.
2. Apply pulse, 0Vdc to VDD, to clock until proper state is obtained.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

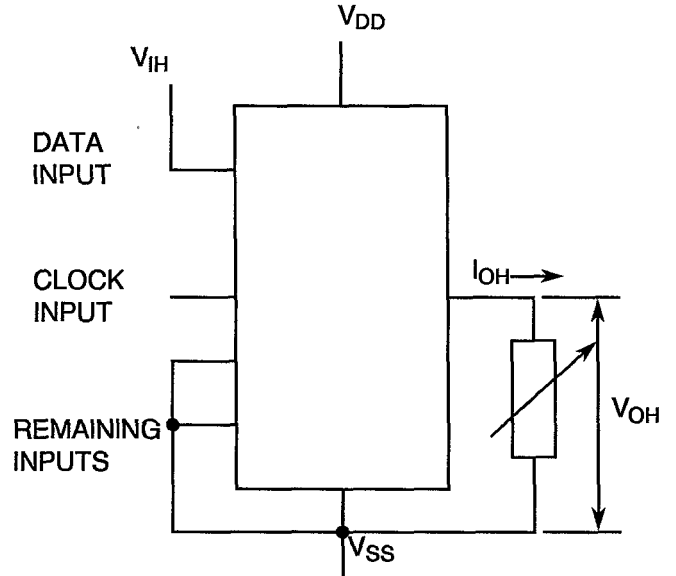
**FIGURE 4(g) - LOW LEVEL OUTPUT CURRENT**



**NOTES**

- 1. Each output to be tested separately.

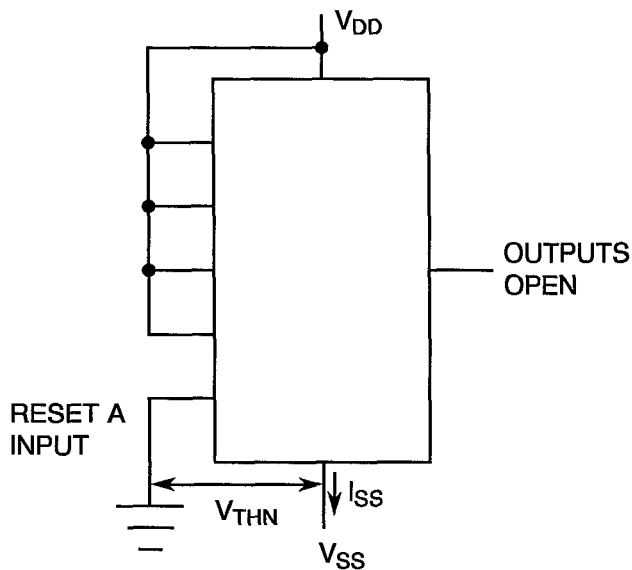
**FIGURE 4(h) - HIGH LEVEL OUTPUT CURRENT**



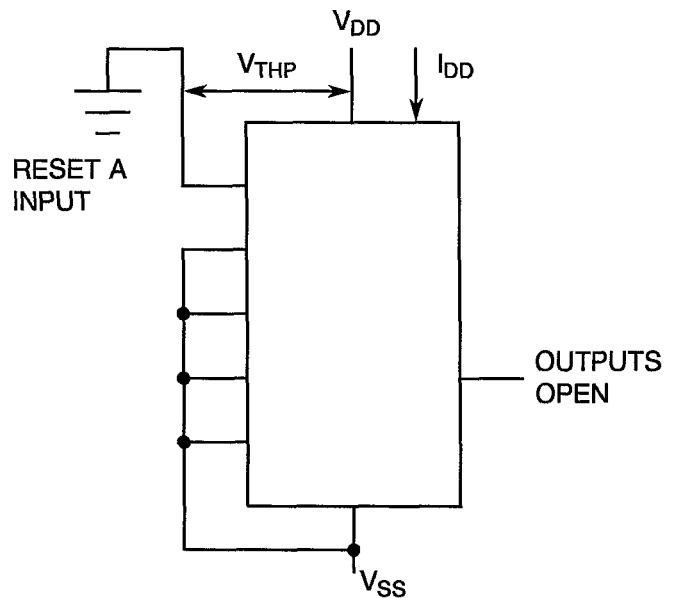
**NOTES**

- 1. Each output to be tested separately.
- 2. Apply pulse, 0Vdc to VDD, to clock until proper state is obtained.

**FIGURE 4(i) - THRESHOLD VOLTAGE N-CHANNEL**



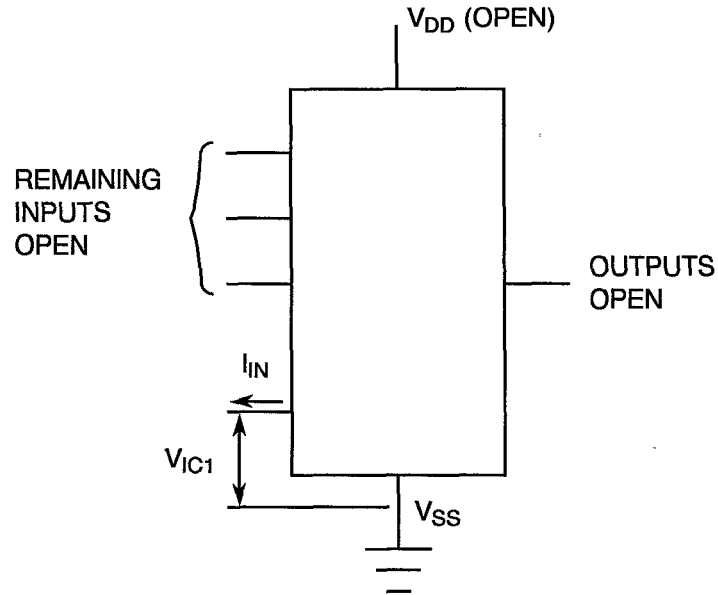
**FIGURE 4(j) - THRESHOLD VOLTAGE P-CHANNEL**





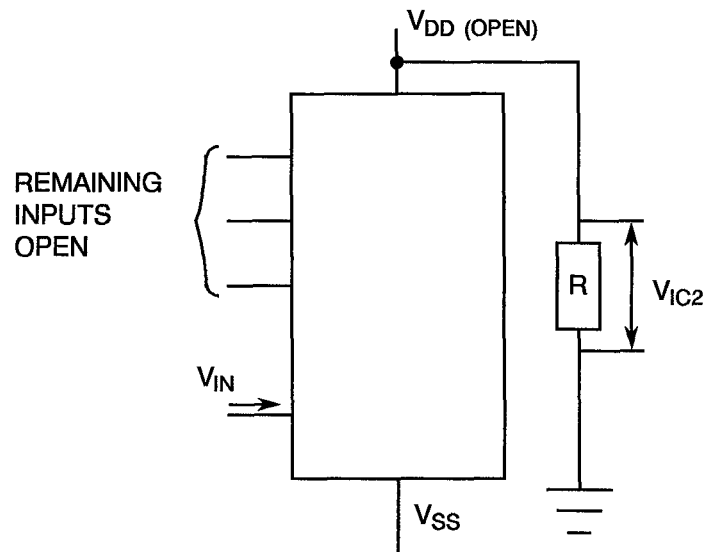
**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(k) - INPUT CLAMP VOLTAGE ( $V_{SS}$ )**



**NOTES** 1. Each input to be tested separately

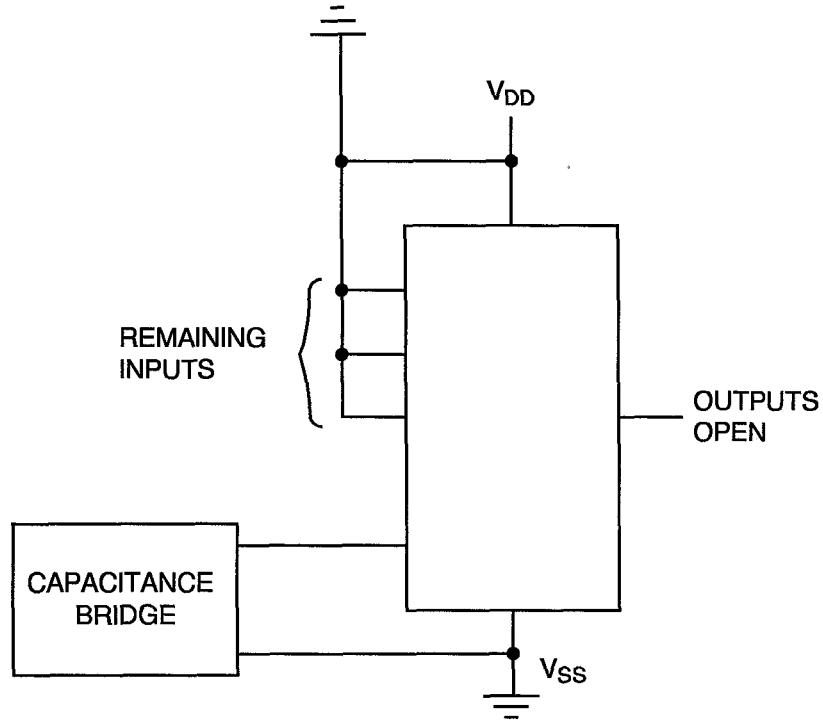
**FIGURE 4(l) - INPUT CLAMP VOLTAGE ( $V_{DD}$ )**



**NOTES** 1. Each input to be tested separately

**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(m) - INPUT CAPACITANCE**



**NOTES**

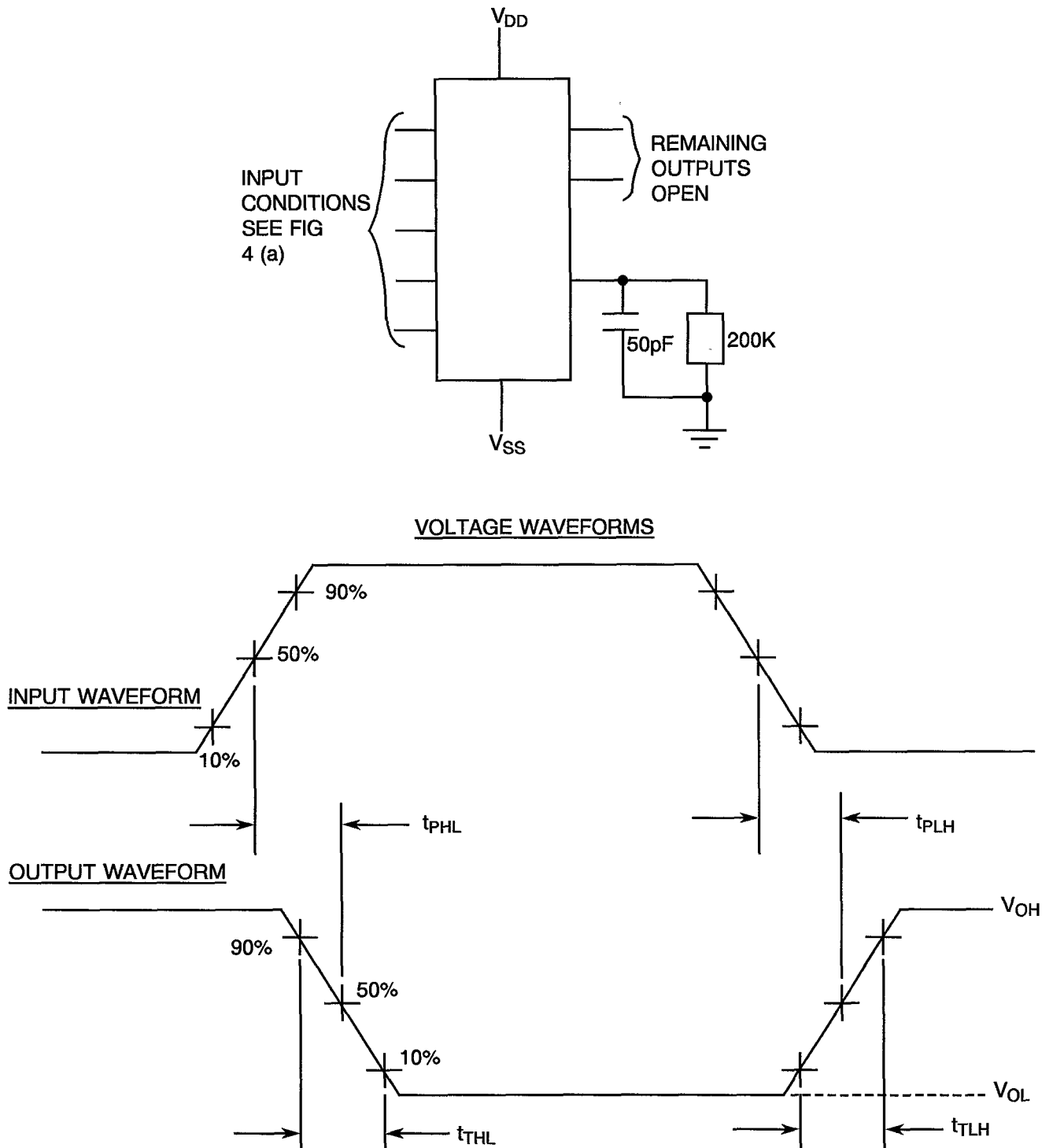
1. Each input to be tested separately.
2.  $f = 100\text{kHz}$  to  $1\text{MHz}$





**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(n) - PROPAGATION DELAY AND TRANSITION TIME**



**NOTES** 1. Pulse Generator -  $V_P = 0$  to  $V_{DD}$ ,  $t_r$  and  $t_f \leq 15ns$ ,  $f = 500KHz$ .

**TABLE 4 - PARAMETER DRIFT VALUES**

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS ( $\Delta$ )	UNIT
3 to 5	Quiescent Current	$I_{DD}$	As per Table 2	As per Table 2	$\pm 150$	nA
34 to 41	Output Drive Current N-Channel	$I_{OL1}$	As per Table 2	As per Table 2	$\pm 15$ (1)	%
50 to 57	Output Drive Current P-Channel	$I_{OH1}$	As per Table 2	As per Table 2	$\pm 15$ (1)	%
68	Threshold Voltage N-Channel	$V_{THN}$	As per Table 2	As per Table 2	$\pm 0.3$	V
69	Threshold Voltage P-Channel	$V_{THP}$	As per Table 2	As per Table 2	$\pm 0.3$	V

**NOTES** 1. Percentage of limit value if voltage is the measurement function.

**TABLE 5(a) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS**

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	$T_{amb}$	+ 125 (+ 0-5)	°C
2	Outputs - (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	$V_{OUT}$	Open	-
3	Inputs - (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	$V_{IN}$	Ground	Vdc
4	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	$V_{DD}$	15	Vdc
5	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	$V_{SS}$	Ground	Vdc

**NOTES** 1. Input Load = Protection Resistor = 2K $\Omega$  minimum to 47K $\Omega$  maximum.

**TABLE 5(b) - CONDITIONS FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS**

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	$T_{amb}$	+ 125 (+ 0-5)	°C
2	Outputs - (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	$V_{OUT}$	Open	-
3	Inputs - (Pins D/F 1-6-7-9-14-15) (Pins C 1-7-9-11-17-19)	$V_{IN}$	$V_{DD}$	Vdc
4	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	$V_{DD}$	15	Vdc
5	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	$V_{SS}$	Ground	Vdc

**NOTES** 1. Input Load = Protection Resistor = 2K $\Omega$  minimum to 47K $\Omega$  maximum.

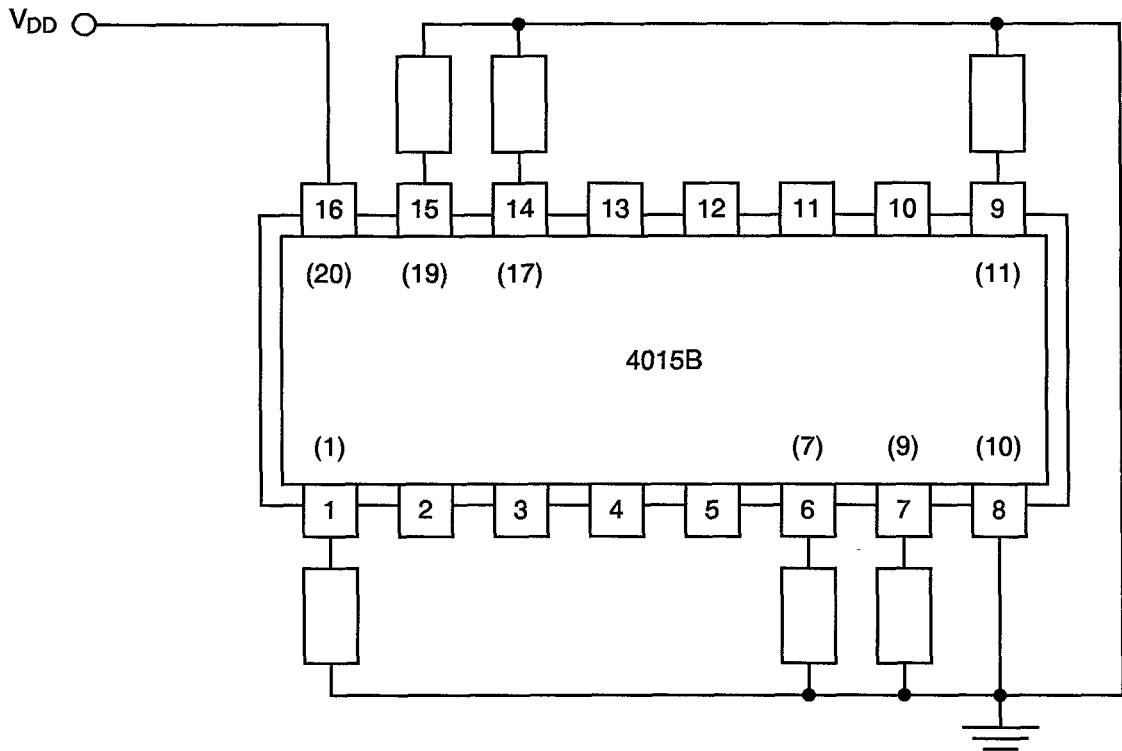
**TABLE 5(c) - CONDITIONS FOR BURN-IN DYNAMIC**

NO.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	$T_{amb}$	+125 (+0-5)	°C
2	Outputs - (Pins D/F 2-3-4-5-10-11-12-13) (Pins C 2-4-5-6-12-14-15-16)	$V_{OUT}$	$V_{DD}/2$	Vdc
3	Inputs - (Pins D/F 1-7-9-15) (Pins C 1-9-11-19)	$V_{IN}$	$V_{GEN}$	Vac
4	Inputs - (Pins D/F 6-14) (Pins C 7-17)	$V_{IN}$	Ground	Vdc
5	Pulse Voltage	$V_{GEN}$	0V to $V_{DD}$	Vac
6	Pulse Frequency Square Wave	f	$50K \leq f < 1M$ 50% Duty Cycle	Hz
7	Positive Supply Voltage (Pin D/F 16) (Pin C 20)	$V_{DD}$	15	Vdc
8	Negative Supply Voltage (Pin D/F 8) (Pin C 10)	$V_{SS}$	Ground	Vdc

**NOTES** 1. Input Load = Output Load = 2K $\Omega$  minimum to 47K $\Omega$  maximum.

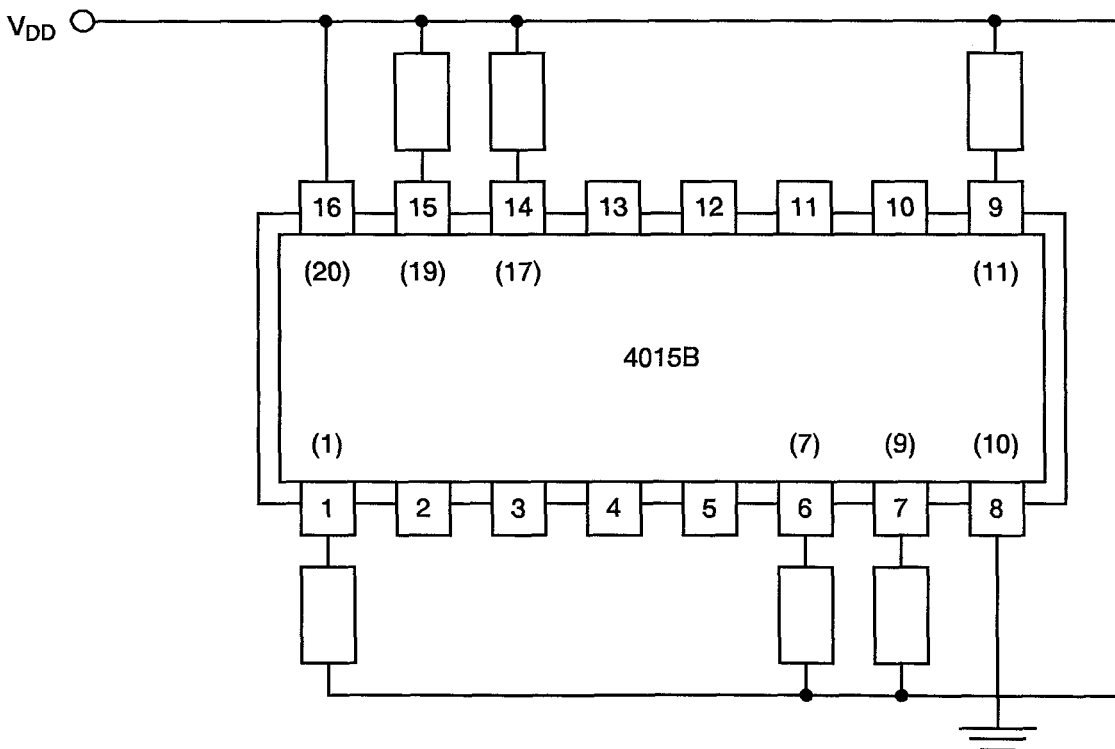


**FIGURE 5(a) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, N-CHANNELS**



**NOTES** 1. Pin numbers in parenthesis are for the chip carrier package.

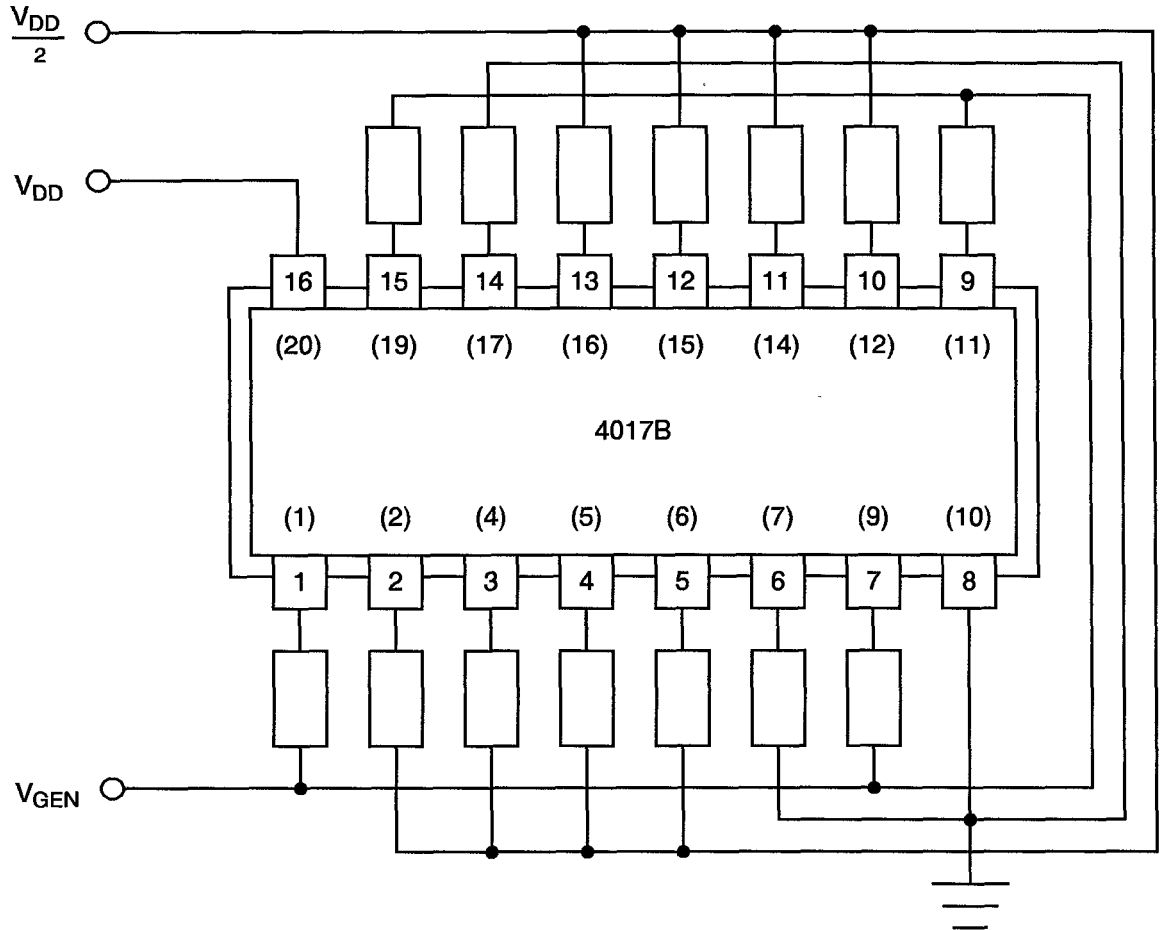
**FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN HIGH TEMPERATURE REVERSE BIAS, P-CHANNELS**





**NOTES** 1. Pin numbers in parenthesis are for the chip carrier package.



**FIGURE 5(c) - ELECTRICAL CIRCUIT FOR BURN-IN DYNAMIC**



**NOTES** 1. Pin numbers in parenthesis are for the chip carrier package.

		<p style="text-align: center;">ESA/SCC Detail Specification No. 9306/015</p>		<p>PAGE 47 ISSUE 3</p>
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4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

4.8.4 Conditions for Operating Life Test

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life test are shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature as specified in Table 1(b) of this specification.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS ( $\Delta$ )			UNIT
						MIN	MAX	
1	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
3 to 5	Quiescent Current	$I_{DD}$	As per Table 2	As per Table 2	$\pm 150$	-	-	nA
6 to 11	Input Current Low Level	$I_{IL}$	As per Table 2	As per Table 2	-	-	-50	nA
12 to 17	Input Current High Level	$I_{IH}$	As per Table 2	As per Table 2	-	-	50	nA
18 to 25	Output Voltage Low Level	$V_{OL}$	As per Table 2	As per Table 2	-	-	0.05	V
26 to 33	Output Voltage High Level	$V_{OH}$	As per Table 2	As per Table 2	-	14.95	-	V
34 to 41	Output Drive Current N-Channel	$I_{OL1}$	As per Table 2	As per Table 2	$\pm 15$ (1)	-	-	%
42 to 49	Output Drive Current N-Channel	$I_{OL2}$	As per Table 2	As per Table 2	$\pm 15$ (1)	-	-	%
50 to 57	Output Drive Current P-Channel	$I_{OH1}$	As per Table 2	As per Table 2	$\pm 15$ (1)	-	-	%
58 to 65	Output Drive Current P-Channel	$I_{OH2}$	As per Table 2	As per Table 2	$\pm 15$ (1)	-	-	%
66	Input Voltage Low Level (Noise Immunity) (Functional Test)	$V_{IL1}$	As per Table 2	As per Table 2	-	4.5	-	V
	Input Voltage High Level (Noise Immunity) (Functional Test)	$V_{IH1}$	As per Table 2	As per Table 2	-	-	0.5	
68	Threshold Voltage N-Channel	$V_{THN}$	As per Table 2	As per Table 2	$\pm 0.3$	-	-	V
69	Threshold Voltage P-Channel	$V_{THP}$	As per Table 2	As per Table 2	$\pm 0.3$	-	-	V

**NOTES** 1. Percentage of limit value if voltage is the measurement function.





APPENDIX 'A'

AGREED DEVIATIONS FOR STMICROELECTRONICS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATION
Para. 4.2.3	Para. 9.23, High Temperature Reverse Bias Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.  Para. 9.24, Power Burn-in: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.4	Para. 9.21.1, Operating Life during Qualification Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.
Para. 4.2.5	Para. 9.21.2, Operating Life during Lot Acceptance Testing: The temperature limits of MIL-STD-883, Para. 4.5.8(c) may be used.