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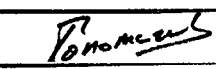
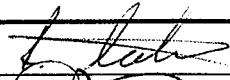
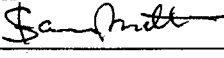
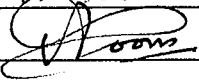
Pages 1 to 31

INTEGRATED CIRCUITS, MONOLITHIC,  
SILICON ON SAPPHIRE,  
CMOS ION COUNTER,  
BASED ON TYPE 11918

ESA/SCC Detail Specification No. 9204/063



space components  
coordination group

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Issue 2	July 1993		
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**SCC**ESA/SCC Detail Specification  
No. 9204/063

Rev. 'A'

PAGE 2



ISSUE 2

**DOCUMENTATION CHANGE NOTICE**

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This issue supersedes Issue 1 and incorporates all modifications defined in the following DCRs:-		
		Cover Page		None
		DCN		None
		Table 1(a)	: Lead Material and Finish amended to "D2"	221016
		Para. 4.2.2	: Paragraph amended	221016
		Para. 4.2.3	: Paragraph amended	221016
		Para. 4.2.4	: Deviation replaced by 'None'	22919
		Para. 4.2.5	: Deviation replaced by 'None'	22919
		Para. 4.4.1	: "Perform" amended to "Preform"	221016
		Para. 4.4.2	: Type "7" amended to Type "2"	221016
		Para. 4.7.1	: H.T.R.B. Burn-in ainea added	23496
		Table 2	: No. 1, amended to "1A"	221016
			: , Test conditions amended	221016
			: , New No. "1B" added	221016
			: Nos 139 to 140, added new "Nos 139 to 140" (Hysteresis)	221016
			: All item numbers incremented by 2	221016
		Table 3(a)	: No. 1, amended to "1A"	221016
			: , Test conditions amended	221016
			: , New No. "1B" added	221016
			: No. 2, maximum limit amended to "300 $\mu$ A"	22950/ 221016
		Table 3(b)	: No. 1, amended to "1A"	221016
			: , Test conditions amended	221016
			: , New No. "1B" added	221016
			: No. 2, Test Condition $V_{DD}$ amended to " $V_{DD} = 5.25V$ "	221016
		Figure 4(i)	: Added " $t_{shold}$ " to Figure	221016
		Figure 4(i) (cont'd)	: Added " $t_{shold}$ " to Table	221016
		Table 5	: Duration added	23496
		Table 6	: No. 1, amended to "1A"	221016
			: , New No. "1B" added	221016
		Table 7	: No. 1, amended to "1A"	221016
			: , New No. "1B" added	221016
			: No. 2, maximum limit amended to "500 $\mu$ A"	221015
'A'	Jan '97	P1. Cover page	: Page count amended	221373
		P2. DCN		None
		P4. T of C	: Appendix 'A' entry added	221373
		P31. Appendix 'A'	: Appendix added as new page	221373

**TABLE OF CONTENTS**

	<u>Page</u>
<b>1. <u>GENERAL</u></b>	<b>5</b>
1.1 Scope	5
1.2 Component Type Variants	5
1.3 Maximum Ratings	5
1.4 Parameter Derating Information	5
1.5 Physical Dimensions	5
1.6 Pin Assignment	5
1.7 Truth Table	5
1.8 Circuit Schematic	5
1.9 Functional Diagram	5
1.10 Handling Precautions	5
1.11 Input and Output Protection Networks	5
<b>2. <u>APPLICABLE DOCUMENTS</u></b>	<b>11</b>
<b>3. <u>TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS</u></b>	<b>11</b>
<b>4. <u>REQUIREMENTS</u></b>	<b>11</b>
4.1 General	11
4.2 Deviations from Generic Specification	11
4.2.1 Deviations from Special In-process Controls	11
4.2.2 Deviations from Final Production Tests	11
4.2.3 Deviations from Burn-in Tests	11
4.2.4 Deviations from Qualification Tests	11
4.2.5 Deviations from Lot Acceptance Tests	11
4.3 Mechanical Requirements	12
4.3.1 Dimension Check	12
4.3.2 Weight	12
4.4 Materials and Finishes	12
4.4.1 Case	12
4.4.2 Lead material and Finish	12
4.5 Marking	12
4.5.1 General	12
4.5.2 Lead Identification	12
4.5.3 The SCC Component Number	12
4.5.4 Traceability Information	13
4.6 Electrical Measurements	13
4.6.1 Electrical Measurements at Room Temperature	13
4.6.2 Electrical Measurements at High and Low Temperatures	13
4.6.3 Circuits for Electrical Measurements	13
4.7 Burn-in Tests	13
4.7.1 Parameter Drift Values	13
4.7.2 Conditions for Power Burn-in	13
4.7.3 Electrical Circuits for Power Burn-in	13
4.8 Environmental and Endurance Tests	27
4.8.1 Electrical Measurements on Completion of Environmental Tests	27
4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests	27
4.8.3 Electrical Measurements on Completion of Endurance Tests	27
4.8.4 Conditions for Operating Life Tests	27
4.8.5 Electrical Circuits for Operating Life Tests	27
4.8.6 Conditions for High Temperature Storage Test	27
4.9 Total Dose Irradiation Testing	27
4.9.1 Application	27
4.9.2 Bias Conditions	27
4.9.3 Electrical Measurements	27

		<p style="text-align: center;">ESA/SCC Detail Specification No. 9204/063</p>	<p style="text-align: center;">Rev. 'A'</p>	<p>PAGE 4 ISSUE 2</p>
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<b><u>TABLES</u></b>	<u>Page</u>
1(a) Type Variants	6
1(b) Maximum Ratings	6
2 Electrical Measurements at Room Temperature - d.c. Parameters	14
Electrical Measurements at Room Temperature - a.c. Parameters	17
3(a) Electrical Measurements at High Temperature	18
3(b) Electrical Measurements at Low Temperature	18
4 Parameter Drift values	24
5 Conditions for Power Burn-in and Operating Life Test	25
6 Electrical Measurements on Completion of Environmental Tests and at Intermediate Points and on Completion of Endurance Testing	28
7 Electrical Measurements During and on Completion of Irradiation Testing	30

<b><u>FIGURES</u></b>	
1 Not applicable	
2 Physical Dimensions	7
3(a) Pin Assignment	8
3(b) Truth Table	8
3(c) Circuit Schematic	9
3(d) Functional Diagram	9
3(e) Input and Output Protection Networks	10
4 Circuits for Electrical Measurements	19
5 Electrical Circuit for Power Burn-in and Operating Life Test	26
6 Bias Conditions for Irradiation Testing	29

<b><u>APPENDICES (Applicable to specific Manufacturers only)</u></b>	
'A' Agreed Deviations for MITEL (S)	31

**1. GENERAL****1.1 SCOPE**

This specification details the ratings, physical and electrical characteristics, test and inspection data for a Monolithic, Silicon on Sapphire, CMOS Ion Counter, based on Type 11918. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

**1.2 COMPONENT TYPE VARIANTS**

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

**1.3 MAXIMUM RATINGS**

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

**1.4 PARAMETER DERATING INFORMATION (Figure 1)**

Not applicable.

**1.5 PHYSICAL DIMENSIONS**

As per Figure 2.

**1.6 PIN ASSIGNMENT**

As per Figure 3(a).

**1.7 TRUTH TABLE**

As per Figure 3(b).

**1.8 CIRCUIT SCHEMATIC**

As per Figure 3(c).

**1.9 FUNCTIONAL DIAGRAM**

As per Figure 3(d).

**1.10 HANDLING PRECAUTIONS**

These circuits are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipping, and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 1500V.

**1.11 INPUT AND OUTPUT PROTECTION NETWORKS**

Protection networks shall be incorporated into each input and output as shown in Figure 3(e).

**TABLE 1(a) - TYPE VARIANTS**

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	Flatpack	2	D2

**TABLE 1(b) - MAXIMUM RATINGS**

NO	CHARACTERISTICS	SYMBOL	MAXIMUM RATING	UNIT	REMARKS
1	Supply Voltage	$V_{DD}$	-0.5 to 7.0	V	
2	Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.5$	V	
3	DC Input Current	$I_{IN}$	$\pm 20$	mA	
4	DC Output Current	$I_{OUT}$	10	mA	Note 1
5	Device Dissipation (Continuous)	$P_D$	200	mWdc	
6	Output Dissipation	$P_{D50}$	50	mWdc	Note 1
7	Operating Temperature Range	$T_{op}$	-55 to +125	$^{\circ}C$	$T_{amb}$
8	Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}C$	
9	Soldering Temperature	$T_{sol}$	+260	$^{\circ}C$	Note 2

**NOTES**

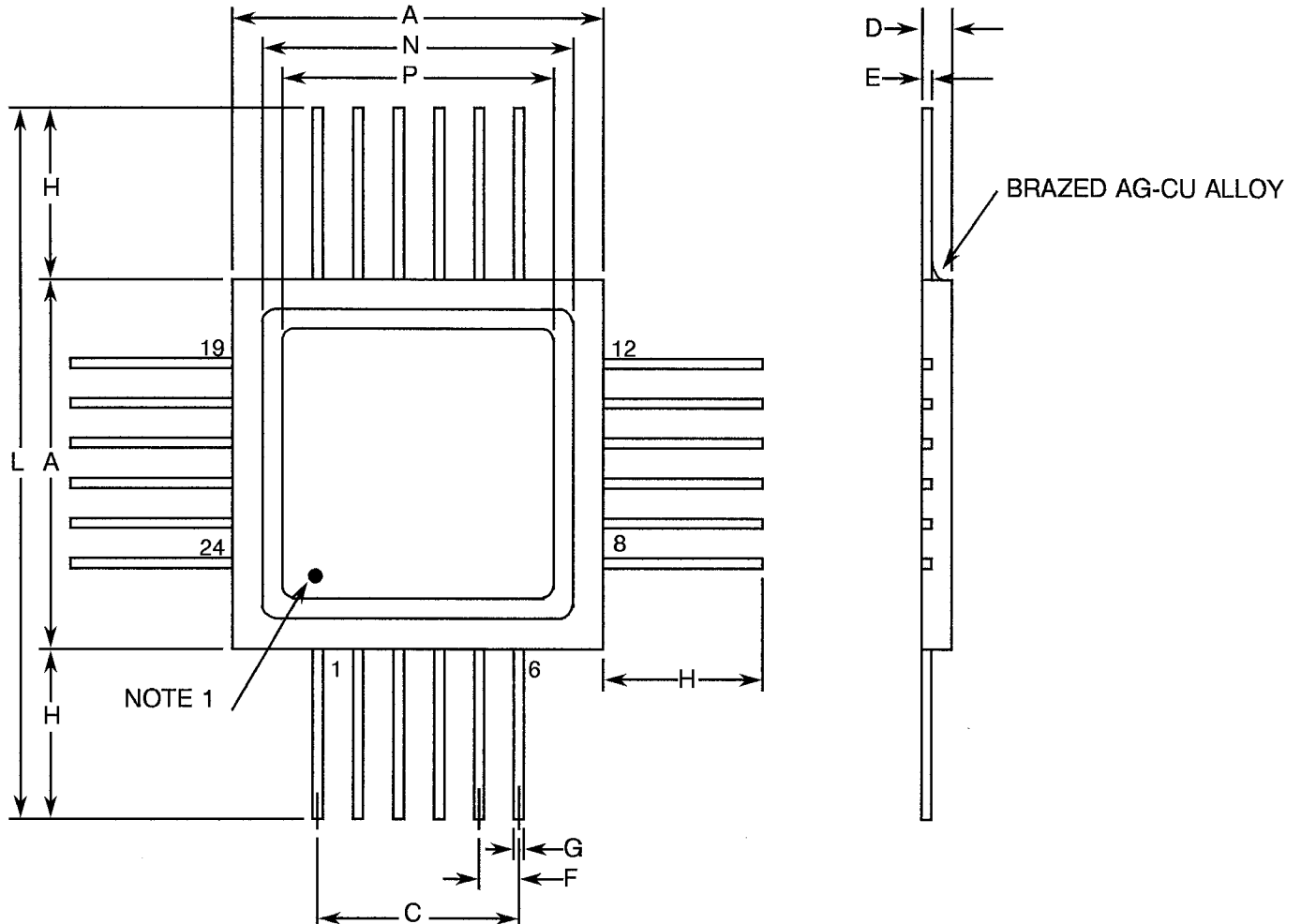
1. Single output.
2. Duration 5 seconds maximum at a distance of not less than 1.0mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

**FIGURE 1 - PARAMETER DERATING INFORMATION**

Not applicable.



**FIGURE 2 - PHYSICAL DIMENSIONS**

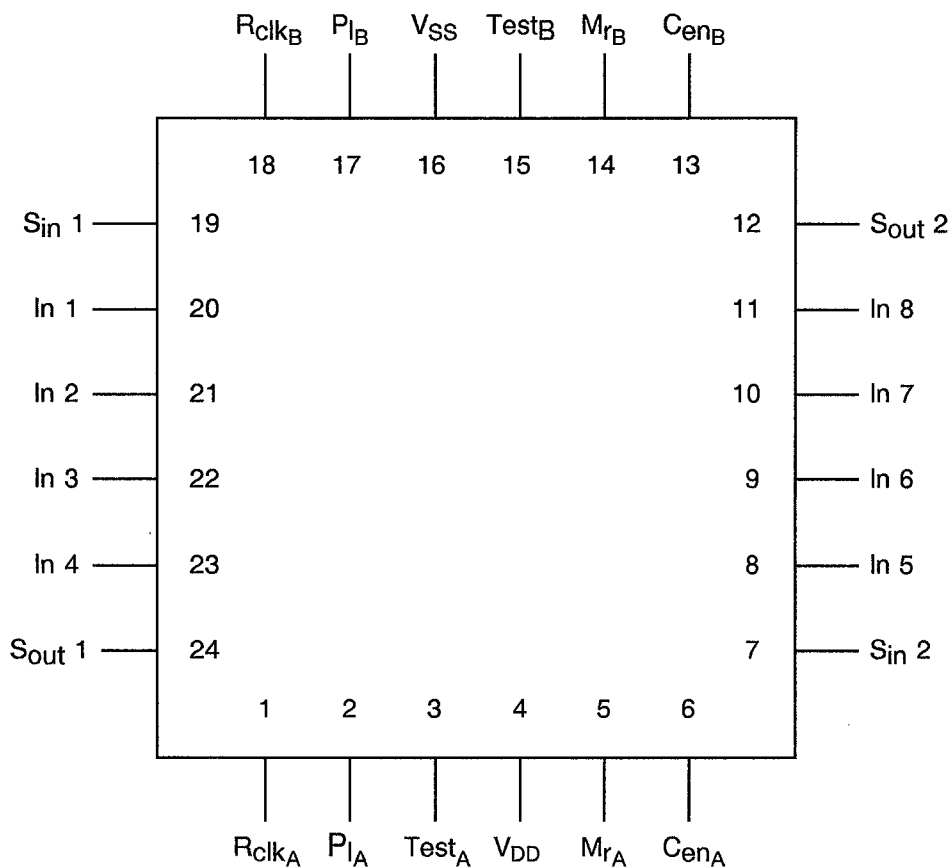


NOTE 1

SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	9.96	10.36	
C	6.22	6.48	
D	1.36	1.73	
E	0.44	0.61	All leads
F	1.19	1.35	
G	0.25	0.51	All leads
H	7.06	-	All leads
L	23.96	-	
M	0.11	0.18	
N	7.98	8.28	
P	6.96	7.26	



**FIGURE 3(a) - PIN ASSIGNMENT**



**FIGURE 3(b) - TRUTH TABLE (EACH COUNTER)**

Sin	In	Rclk	Pl	Mr	Cen	Test	Operation
X	↕	X	L	L	H	L	Count
X	X	X	H	L	L	L	Shift register load
X	X	↕	L	L	X	L	Output next bit
X	X	X	L	H	L	L	Counter reset
X	X	X	H	H	X	L	Master reset
X	X	X	X	X	X	H	Test mode

**NOTES**

1. Logic Level Definitions: L = Low Level, H = High Level, X = Don't Care, ↕ = Transition Low to High.

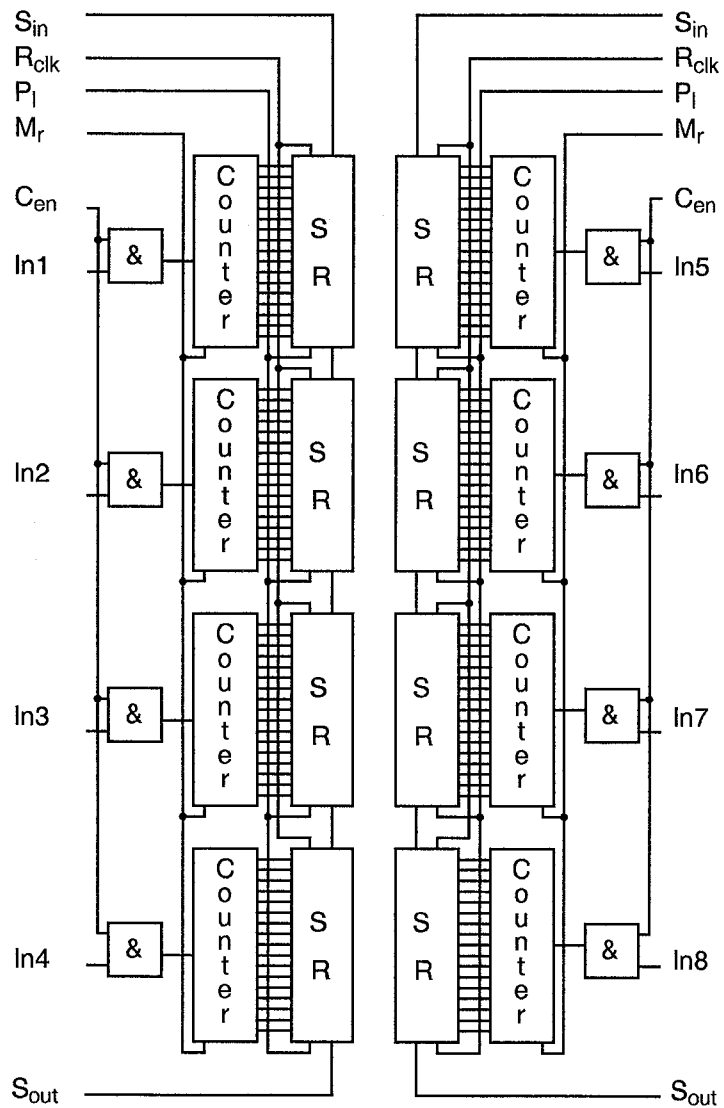




**FIGURE 3(c) - CIRCUIT SCHEMATIC**

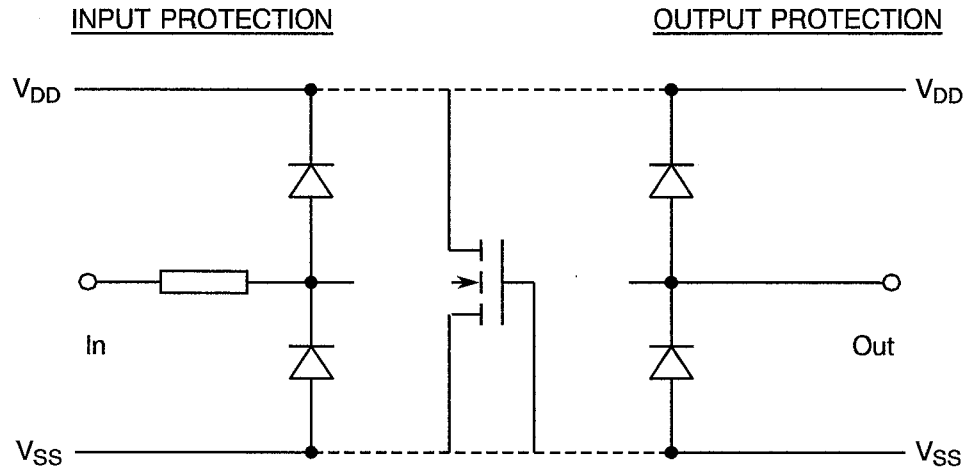
Not applicable

**FIGURE 3(d) - FUNCTIONAL DIAGRAM**





**FIGURE 3(e) - INPUT AND OUTPUT PROTECTION NETWORKS**



**2. APPLICABLE DOCUMENTS**

The following documents form part of this specification and shall be read in conjunction with it:

- (a) ESA/SCC Generic Specification No 9000 for Integrated Circuits Monolithic.
- (b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

**3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS**

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

$V_{HYS}$  = Hysteresis voltage

$C_{IN}$  = Input capacitance

$C_{OUT}$  = Output capacitance

**4. REQUIREMENTS****4.1 GENERAL**

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the component's reliability, are listed in the appendices attached to this specification.

**4.2 DEVIATION FROM GENERIC SPECIFICATION****4.2.1 Deviations from Special In-process Controls**

- (a) Para. 5.2.2, "Total Dose Irradiation Testing": Shall be performed during irradiation qualification and maintenance of qualification.
- (b) Para. 5.2.2, "Total Dose Irradiation Testing": Shall be performed during procurement on an irradiation lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

**4.2.2 Deviations from Final Production Tests (Chart III)**

- (a) Para. 4.4, "Marking": Shall be performed after Para. 9.3, Encapsulation.
- (b) Para. 9.12, "Radiographic Inspection": Shall be performed after Para. 9.8.1/Para. 9.8.2, Seal Test.

**4.2.3 Deviations from Burn-in Tests (Chart III)**

- (a) Para. 9.12, "Radiographic Inspection": Shall not be performed.

**4.2.4 Deviations from Qualification Tests (Chart IV)**

None.

**4.2.5 Deviations from Lot Acceptance Tests (Chart V)**

None.



4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuit specified herein shall be 0.85 grammes.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body, and the lids shall be welded, brazed, or preform soldered.

4.4.2 Lead Material and Finish

The material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

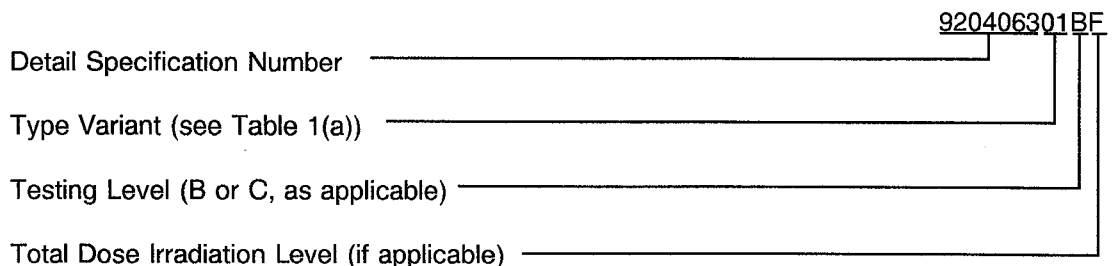
- a) Lead Identification.
- b) The SCC Component Number.
- c) Traceability Information.



4.5.2 Lead Identification

An index will be located at the top of the package in the position defined in note 1 to Figure 2. The pin numbering must be read with the index on the left hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:-



		<p style="text-align: center;">ESA/SCC Detail Specification No. 9204/063</p>	<p>PAGE 13 ISSUE 2</p>
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4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at  $T_{amb} = +125(+0-5)$  °C and  $-55(+5-0)$  °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C. The parameter drift values ( $\Delta$ ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified in Table 2 shall not be exceeded.

For H.T.R.B. Burn-in, the parameter drift values ( $\Delta$ ) shall be applied before the N-Channel (0 hours) and after the P-Channel (144 hours) Burn-in.

4.7.2 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in test are shown in Figure 5 of this specification.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS**

NO	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1A	Functional Test	-	-	4(a) 4(i)	$C_L = 100\text{pF}$ , $R_L = 1.0\text{M}\Omega$ $V_{IL} = 0.8\text{V}$ , $V_{IH} = 4.2\text{V}$ $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ Note 1	-	-	
1B	Functional Test	-	-	4(a) 4(i)	$C_L = 100\text{pF}$ , $R_L = 1.0\text{M}\Omega$ $V_{IL} = 0.8\text{V}$ , $V_{IH} = 4.2\text{V}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ Note 1	-	-	
2	Quiescent Current	$I_{DD}$	-	4(b)	All inputs Grounded $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ (Pin 4)	-	20	$\mu\text{A}$
3 to 22	Input Current Low Level	$I_{IL}$	3009	4(c)	$V_{IN}$ (Input under Test) = 0V $V_{IN}$ (Remaining Inputs) = 5.25V $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ (Pins 1-2-3-5-6-7-8-9-10-11-13-14-15-17-18-19-20-21-22-23)	-	50	nA
23 to 42	Input Current High Level	$I_{IH}$	3010	4(d)	$V_{IN}$ (Input under Test) = 5.25V $V_{IN}$ (Remaining Inputs) = 0V $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ (Pins 1-2-3-5-6-7-8-9-10-11-13-14-15-17-18-19-20-21-22-23)	-	50	nA
43 to 44	Output Voltage Low Level	$V_{OL}$	3007	4(e)	$V_{IN} = 3.15\text{V}$ , $I_{OL} = 4.0\text{mA}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ (Pins 12-24)	-	0.4	V
45 to 46	Output Voltage High Level	$V_{OH}$	3006	4(f)	$V_{IN} = 3.15\text{V}$ , $I_{OH} = -4.0\text{mA}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ (Pins 12-24)	2.8	-	V
47 to 48	Input Voltage Low Level (Noise Immunity) (Functional Test)	$V_{IL}$	-	4(a) 4(i)	$V_{IL} = 0.4\text{V}$ , $V_{IH} = 2.8\text{V}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ Note 2 (Pins 12-24)	-	1.0	V
49 to 50	Input Voltage High Level (Noise Immunity) (Functional Test)	$V_{IH}$	-	4(a) 4(i)	$V_{IL} = 0.4\text{V}$ , $V_{IH} = 2.8\text{V}$ $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ Note 2 (Pins 12-24)	4.0	-	V
51 to 60	Threshold Voltage N-Channel 1	$V_{THN1}$	-	4(g)	$V_{IN} = \text{Ramped}$ Test Points A and B = $V_{DD}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ Note 3 (Pins 12-24)	-	3.6	V

**NOTES:** See Page 17.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

NO	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
61 to 70	Threshold Voltage N-Channel 2	$V_{THN2}$	-	4(g)	$V_{IN}$ = Ramped Test Points A and B = $V_{DD}$ $V_{DD} = 5.25V$ , $V_{SS} = 0V$ Note 3 (Pins 12-24)	-	4.1	V
71 to 80	Threshold Voltage P-Channel 1	$V_{THP1}$	-	4(g)	$V_{IN}$ = Ramped Test Points A and B = $V_{DD}$ $V_{DD} = 4.75$ , $V_{SS} = 0V$ Note 3 (Pins 12-24)	1.0	-	V
81 to 90	Threshold Voltage P-Channel 2	$V_{THP2}$	-	4(g)	$V_{IN}$ = Ramped Test Points A and B = $V_{DD}$ $V_{DD} = 5.25$ , $V_{SS} = 0V$ Note 3 (Pins 12-24)	1.0	-	V
91 to 110	Input Clamp Voltage (to $V_{SS}$ )	$V_{IC1}$	-	4(h)	$I_{IN}$ (Under Test) = -50mA $V_{DD}$ = Open, $V_{SS} = 0V$ All Other Pins Open Note 4 (Pins 1-2-3-5-6-7-8-9-10-11-13-14-15-17-18-19-20-21-22-23)	-	-3.0	V
111 to 130	Input Clamp Voltage (to $V_{DD}$ )	$V_{IC2}$	-	4(h)	$I_{IN}$ (Under Test) = 50mA $V_{DD} = 0V$ , $V_{SS}$ = Open All Other Pins Open Note 4 (Pins 1-2-3-5-6-7-8-9-10-11-13-14-15-17-18-19-20-21-22-23)	-	3.0	V

**NOTES:** See Page 17.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

NO	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
131 to 136	Supply Current	$I_{DDop}$	-	4(a) 4(i)	C = 10MHz SR = 1.0MHz	-	6.0	mA
					C = 10MHz SR = 100kHz	-	2.7	
					C = 10MHz SR = 10kHz	-	2.4	
					C = 1.0MHz SR = 1.0MHz	-	3.8	
					C = 1.0MHz SR = 100kHz	-	0.60	
					C = 1.0MHz SR = 10kHz	-	0.30	
					$V_{DD} = 5.25V, V_{SS} = 0V$ Note 5 (Pin 4)			
137 to 138	Hysteresis	$V_{HYS}$	-	4(a) 4(i)	$V_{DD} = 4.75V, V_{SS} = 0V$ Note 6 (Pins 12-24)	0.5	3.0	V
139 to 140	Hysteresis	$V_{HYS}$	-	4(a) 4(i)	$V_{DD} = 5.25V, V_{SS} = 0V$ Note 6 (Pins 12-24)	0.5	3.0	V

**NOTES:** See Page 17.



**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS**

NO	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
141 to 160	Input Capacitance	$C_{in}$	-	-	$V_{DD} = V_{SS} = 0V$ Note 7 (Pins 1-2-3-5-6-7-8-9-10-11-13-14-15-17-18-19-20-21-22-23)	-	1.0	pF
161 to 162	Output Capacitance	$C_{out}$	-	-	$V_{DD} = V_{SS} = 0V$ Note 7 (Pins 12-24)	-	5.0	pF
163 to 164	Propagation Delay Low to High $R_{clk}$ to $S_{out}$	$t_{PLH1}$	-	4(a) 4(i)	$V_{DD} = 4.75V, V_{SS} = 0V$ Notes 8 and 9 <u>Pins</u> 1 to 24 18 to 12	-	100	ns
165 to 166	Propagation Delay High to Low $R_{clk}$ to $S_{out}$	$t_{PHL1}$	-	4(a) 4(i)	$V_{DD} = 4.75V, V_{SS} = 0V$ Notes 8 and 9 <u>Pins</u> 1 to 24 18 to 12	-	100	ns
167 to 168	Propagation Delay Low to High $P_1$ to $S_{out}$	$t_{PLH2}$	-	4(a) 4(i)	$V_{DD} = 4.75V, V_{SS} = 0V$ Notes 8 and 9 <u>Pins</u> 2 to 24 17 to 12	-	100	ns
169 to 170	Propagation Delay High to Low $P_1$ to $S_{out}$	$t_{PHL2}$	-	4(a) 4(i)	$V_{DD} = 4.75V, V_{SS} = 0V$ Notes 8 and 9 <u>Pins</u> 2 to 24 17 to 12	-	100	ns

**NOTES**

- Includes set up and hold timing tests.
- This is performed as a Functional Test in which extreme  $V_{IN}$  conditions are applied and output voltage is measured.
- Pins 8, 9, 10, 11, 13 measured on Pin 12. Pins 6, 20, 21, 22, 23 measured on Pin 24.  $V_{IN}$  is ramped by steps until a change in output state occurs. This is repeated twice, the second time with finer steps to ensure accuracy.
- Measurements to be performed on 100% basis go-no-go.
- $C$  = Counter frequency,  $SR$  = Read clock frequency.
- Hysteresis shall be performed only during Qualification and Maintenance of Qualification.

**TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE**

NO	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1A	Functional Test	-	-	4(a) 4(i)	$C_L = 100\text{pF}$ , $R_L = 1.0\text{M}\Omega$ $V_{IL} = 0.8\text{V}$ , $V_{IH} = 4.2\text{V}$ $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ Note 1	-	-	
1B	Functional Test	-	-	4(a) 4(i)	$C_L = 100\text{pF}$ , $R_L = 1.0\text{M}\Omega$ $V_{IL} = 0.8\text{V}$ , $V_{IH} = 4.2\text{V}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ Note 1	-	-	
2	Quiescent Current	$I_{DD}$	-	4(b)	All inputs Grounded $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ (Pin 4)	-	300	$\mu\text{A}$
131	Supply Current	$I_{DDop}$	-	4(a) 4(i)	$C = 10\text{MHz}$ , $\text{SR} = 1.0\text{MHz}$ $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ Note 5 (Pin 4)	-	6.5	mA

**NOTES:** See Page 17.**TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE**

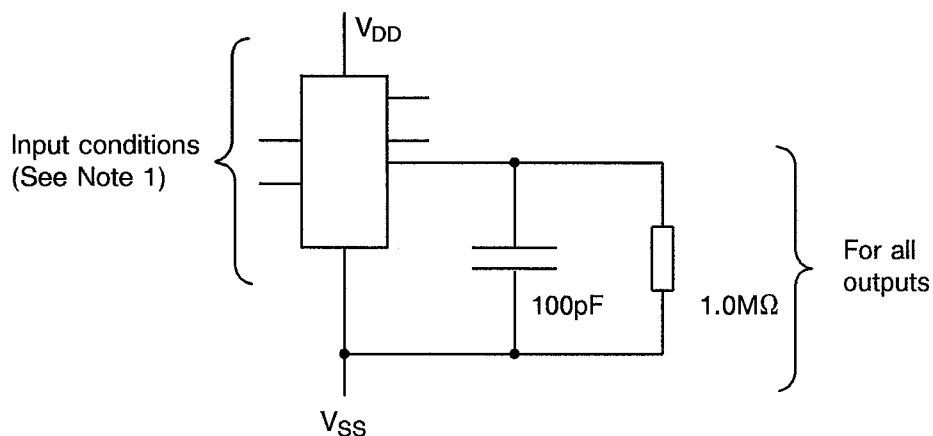
NO	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1A	Functional Test	-	-	4(a) 4(i)	$C_L = 100\text{pF}$ , $R_L = 1.0\text{M}\Omega$ $V_{IL} = 0.8\text{V}$ , $V_{IH} = 4.2\text{V}$ $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ Note 1	-	-	
1B	Functional Test	-	-	4(a) 4(i)	$C_L = 100\text{pF}$ , $R_L = 1.0\text{M}\Omega$ $V_{IL} = 0.8\text{V}$ , $V_{IH} = 4.2\text{V}$ $V_{DD} = 4.75\text{V}$ , $V_{SS} = 0\text{V}$ Note 1	-	-	
2	Quiescent Current	$I_{DD}$	-	4(b)	All inputs Grounded $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ (Pin 4)	-	20	$\mu\text{A}$
131	Supply Current	$I_{DDop}$	-	4(a) 4(i)	$C = 10\text{MHz}$ , $\text{SR} = 1.0\text{MHz}$ $V_{DD} = 5.25\text{V}$ , $V_{SS} = 0\text{V}$ Note 5 (Pin 4)	-	6.5	mA

**NOTES:** See Page 17.



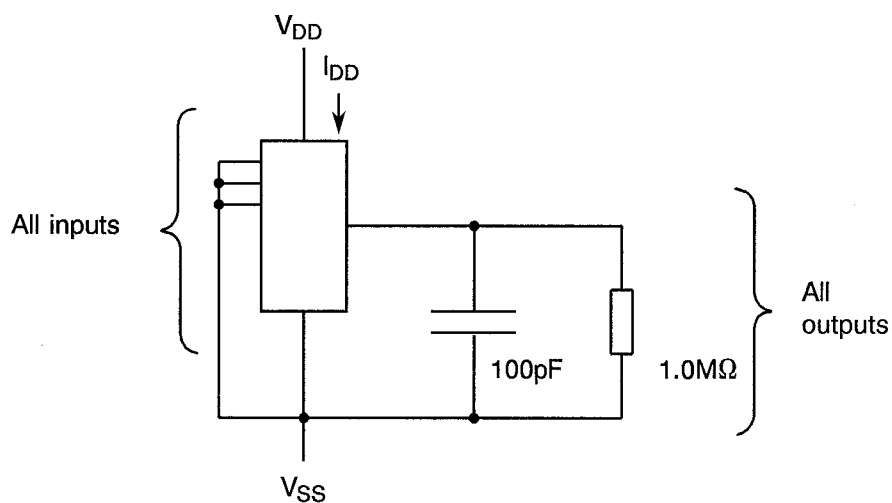
**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS**

**FIGURE 4(a) - FUNCTIONAL TEST**

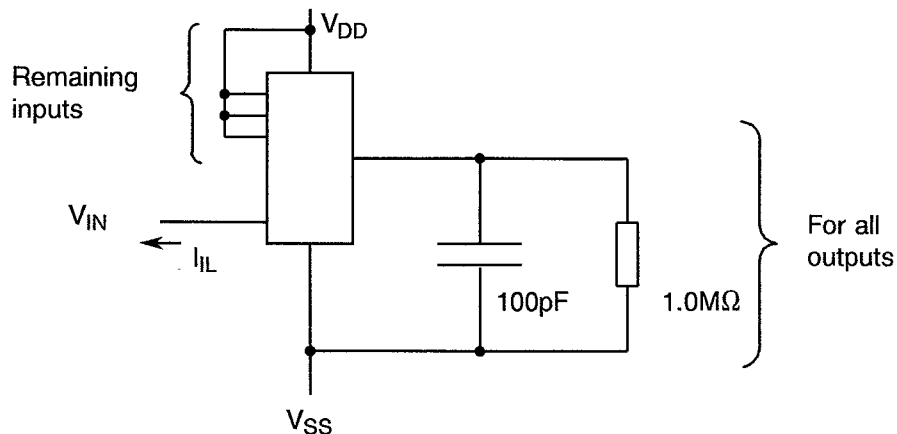


**NOTES** 1.  $V_{IN} = V_{IL(max)}$  and/or  $V_{IH(min)}$  as per Truth Table.

**FIGURE 4(b) - QUIESCENT CURRENT**



**FIGURE 4(c) - INPUT CURRENT LOW LEVEL**

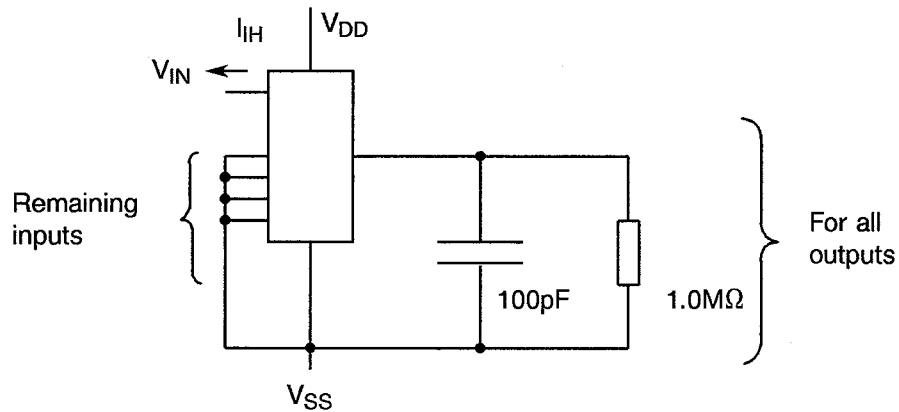


**NOTES** 1. Each input to be tested separately.



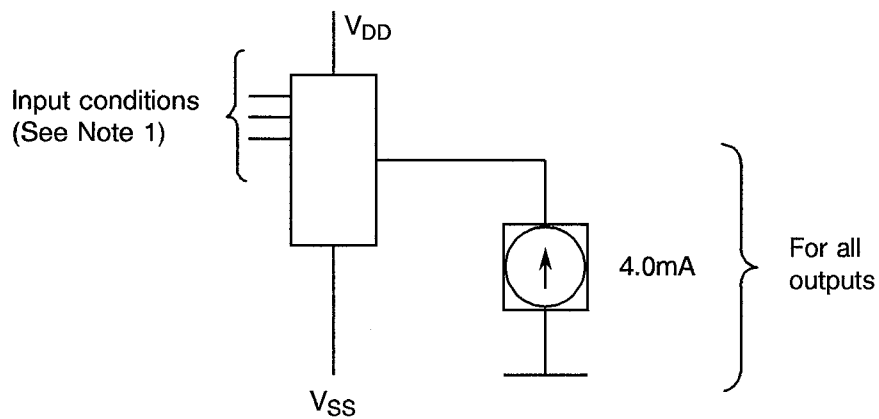
**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(d) - INPUT CURRENT HIGH LEVEL**



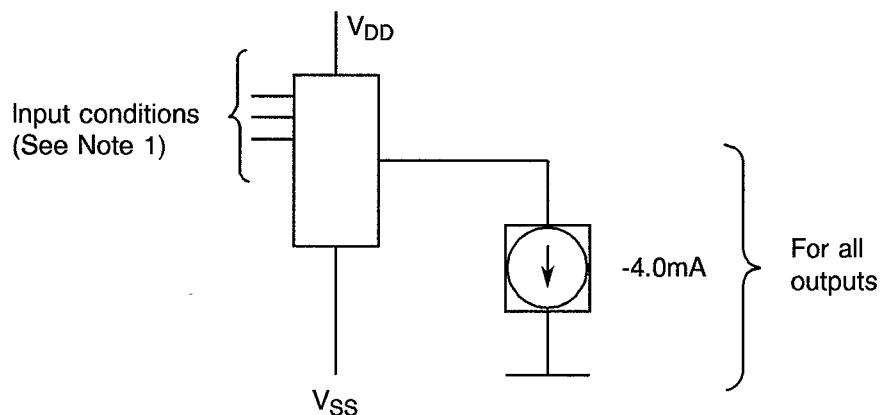
**NOTES** 1. Each input to be tested separately.

**FIGURE 4(e) - OUTPUT VOLTAGE LOW LEVEL**



**NOTES** 1.  $V_{IN} = V_{IL(max)}$  and/or  $V_{IH(min)}$  as per Truth Table to give  $V_{OL}$ .  
2. Each output to be tested separately.

**FIGURE 4(f) - OUTPUT VOLTAGE HIGH LEVEL**

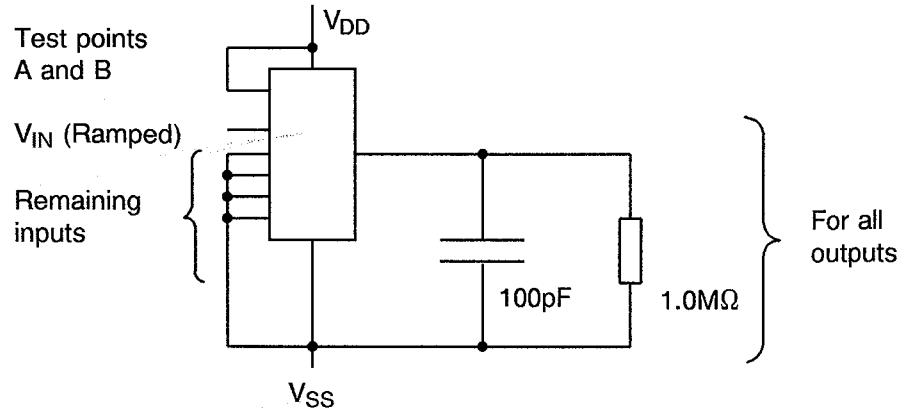


**NOTES** 1.  $V_{IN} = V_{IL(max)}$  and/or  $V_{IH(min)}$  as per Truth Table to give  $V_{OH}$ .  
2. Each output to be tested separately.



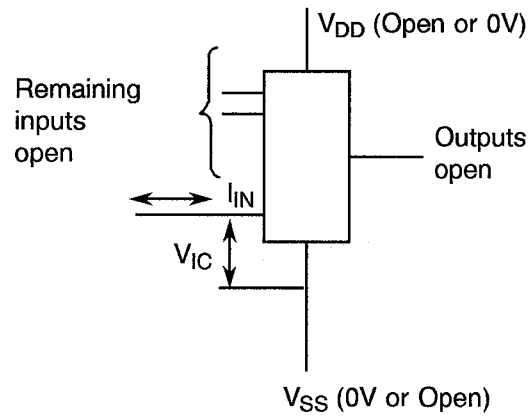
**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(g) - THRESHOLD VOLTAGE**



**NOTES** 1. For test method, see Note 3 to Table 2.

**FIGURE 4(h) - INPUT CLAMP VOLTAGE**

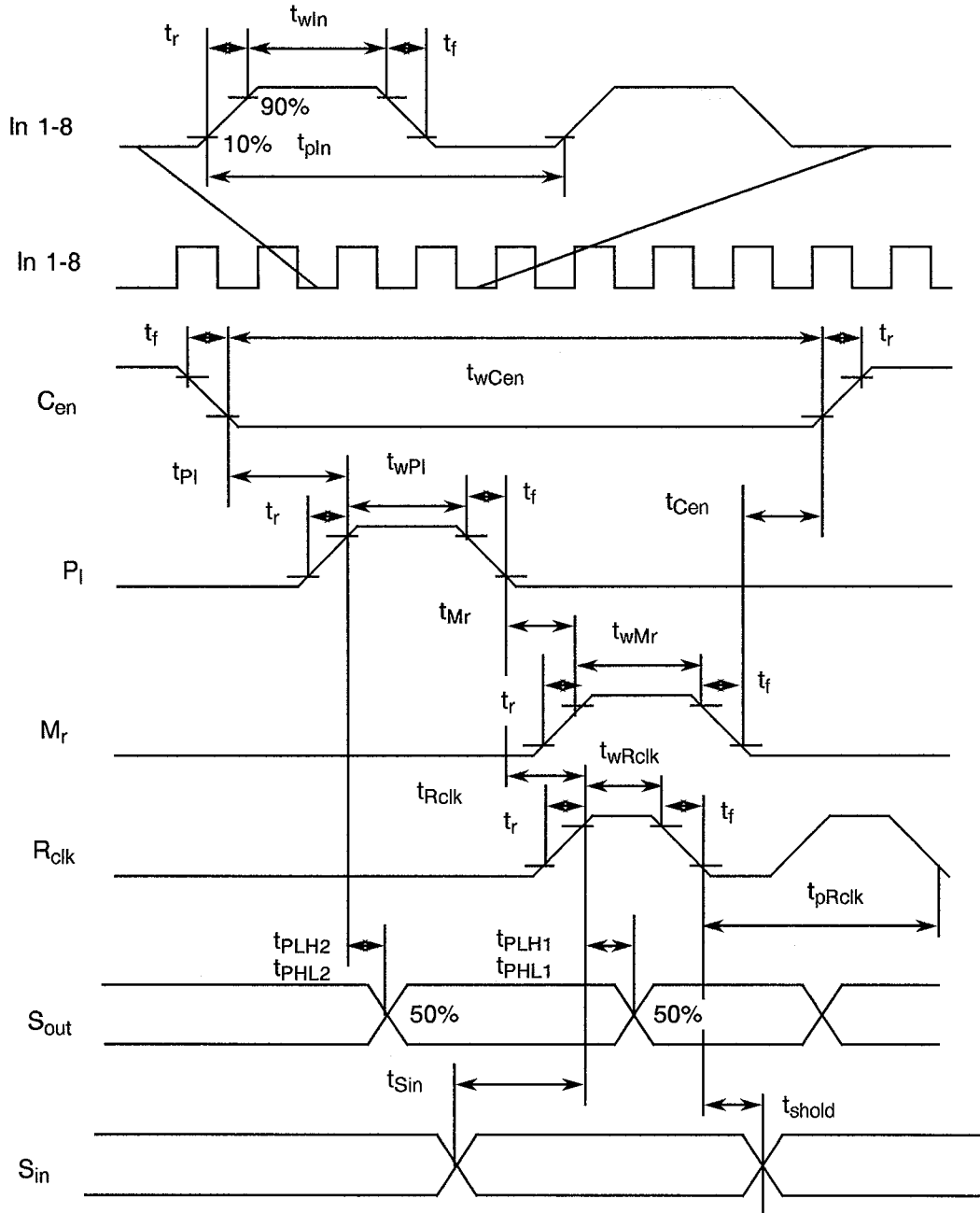


**NOTES** 1. Each input to be tested separately.



**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)**

**FIGURE 4(i) - VOLTAGE WAVEFORMS**



**NOTES**

1. The values for the parameters defined in the figure are given in the table on the next page.

**FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)****FIGURE 4(i) - VOLTAGE WAVEFORMS (CONTINUED)**

TIME	SYMBOL	MIN	MAX	UNIT
Rise Time	$t_r$	-	1.0	$\mu\text{s}$
Fall Time	$t_f$	-	1.0	$\mu\text{s}$
Pulse Width In 1-8	$t_{wIn}$	50	-	ns
Period In 1-8	$t_{pIn}$	100	-	ns
Pulse Width Cen	$t_{wCen}$	4.0	-	$\mu\text{s}$
C <sub>en</sub> low to P <sub>l</sub> high	$t_{pI}$	1.0	-	$\mu\text{s}$
Pulse Width P <sub>l</sub>	$t_{wPI}$	1.0	-	$\mu\text{s}$
P <sub>l</sub> low to M <sub>r</sub> high	$t_{Mr}$	1.0	-	$\mu\text{s}$
Pulse Width M <sub>r</sub>	$t_{wMr}$	1.0	-	$\mu\text{s}$
M <sub>r</sub> low to C <sub>en</sub> high	$t_{Cen}$	0	-	ns
P <sub>l</sub> low to R <sub>clk</sub> high	$t_{Rclk}$	1.0	-	$\mu\text{s}$
Pulse Width R <sub>clk</sub>	$t_{wRclk}$	500	-	ns
Period R <sub>clk</sub>	$t_{pRclk}$	1.0	-	$\mu\text{s}$
Setup S <sub>in</sub> to R <sub>clk</sub>	$t_{Sin}$	100	-	ns
Hold S <sub>in</sub> to R <sub>clk</sub> low	$t_{shold}$	100	-	ns

**TABLE 4 - PARAMETER DRIFT VALUES**

NO	CHARACTERISTICS	SYMBOL	SPEC AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS ( $\Delta$ )	UNIT
2	Quiescent Current	$I_{DD}$	As per Table 2	As per Table 2	$\pm 10$	$\mu A$
3 to 22	Input Current Low Level	$I_{IL}$	As per Table 2	As per Table 2	$\pm 25$	nA
23 to 42	Input Current High Level	$I_{IL}$	As per Table 2	As per Table 2	$\pm 25$	nA
43 to 44	Output Voltage Low Level	$V_{OL}$	As per Table 2	As per Table 2	$\pm 0.2$	V
45 to 46	Output Voltage High Level	$V_{OH}$	As per Table 2	As per Table 2	$\pm 0.9$	V





**TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST**

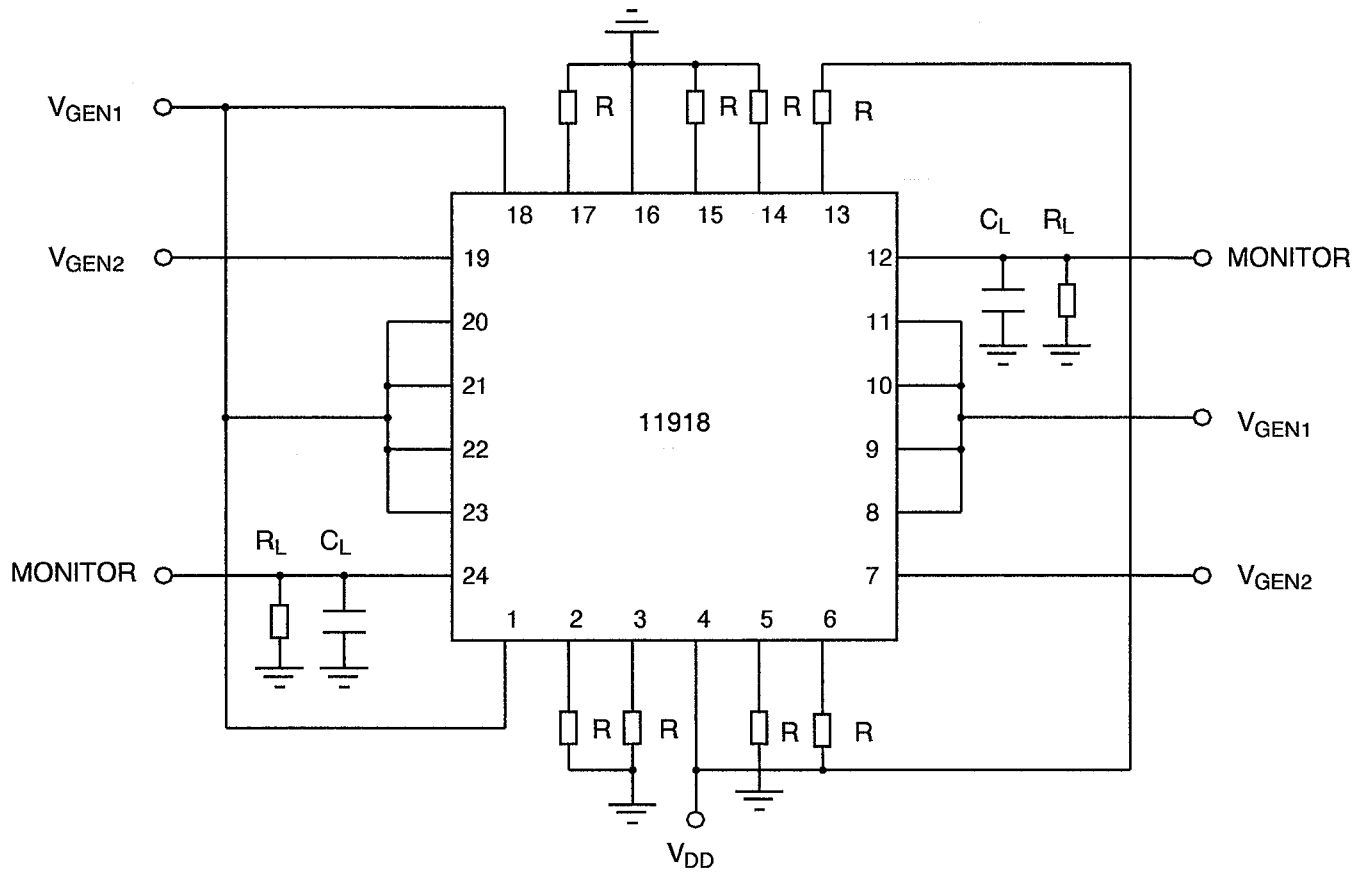
NO	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	$T_{amb}$	+ 125( + 0-5)	°C
2	Outputs - (Pins 12-24)	$V_{OUT}$	Note 2	-
3	Inputs - (Pins 1-8-9-10-11-18-20-21-22-23)	$V_{IN}$	$V_{GEN1}$	Vac
4	Inputs - (Pins 7-19)	$V_{IN}$	$V_{GEN2}$	Vac
5	Inputs - (Pins 6-13)	$V_{IN}$	$V_{DD}$	V
6	Inputs - (Pins 2-3-5-14-15-17)	$V_{IN}$	Ground	V
7	Pulse Voltage	$V_{GEN}$	0 to $V_{DD}$	Vac
8	Pulse Frequency Square Wave	$f_{GEN1}$ $f_{GEN2}$	1.0 0.5 50% Duty Cycle	MHz
9	Positive Supply Voltage (Pin 4)	$V_{DD}$	5.0	V
10	Negative Supply Voltage (Pin 16)	$V_{SS}$	Ground	V
11	Duration	t	72	Hrs

**NOTES**

1. Input Load = Protection Resistor =  $R = 4.7k\Omega$ .
2. Output Load =  $R_L = 1.0M\Omega$  and  $C_L = 100pF$ .



**FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST**





- 4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)
- 4.8.1 Electrical Measurements on Completion of Environmental Tests  
The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.
- 4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests  
The parameters to be measured at intermediate points during endurance testing are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.
- 4.8.3 Electrical Measurements on Completion of Endurance Tests  
The parameters to be measured on completion of endurance testing are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at  $T_{amb} = +22 \pm 3$  °C.
- 4.8.4 Conditions for Operating Life Tests  
The requirements for operating life testing are specified in section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.
- 4.8.5 Electrical Circuits for Operating Life Tests  
Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.
- 4.8.6 Conditions for High Temperature Storage Test  
The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.
- 4.9 TOTAL DOSE IRRADIATION TESTING
- 4.9.1 Application  
If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.
- 4.9.2 Bias Conditions  
Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.
- 4.9.3 Electrical Measurements  
The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.  
  
The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING**

NO	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITION	CHANGE LIMITS ( $\Delta$ )	ABSOLUTE		UNIT
						MIN	MAX	
1A	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
1B	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
2	Quiescent Current	$I_{DD}$	As per Table 2	As per Table 2	$\pm 10$	-	20	$\mu A$
3 to 22	Input Current Low Level	$I_{IL}$	As per Table 2	As per Table 2	$\pm 25$	-	50	nA
23 to 42	Input Current High Level	$I_{IH}$	As per Table 2	As per Table 2	$\pm 25$	-	50	nA
43 to 44	Output Voltage Low Level	$V_{OL}$	As per Table 2	As per Table 2	$\pm 0.2$	-	0.4	V
45 to 46	Output Voltage High Level	$V_{OH}$	As per Table 2	As per Table 2	$\pm 0.9$	2.8	-	V
47 to 48	Input Voltage Low Level (Noise Immunity) (Functional Test)	$V_{IL}$	As per Table 2	As per Table 2	-	-	1.0	V
49 to 50	Input Voltage High Level (Noise Immunity) (Functional Test)	$V_{IH}$	As per Table 2	As per Table 2	-	4.0	-	V
51 to 60	Threshold Voltage N-Channel 1	$V_{THN1}$	As per Table 2	As per Table 2	-	-	3.6	V
61 to 70	Threshold Voltage N-Channel 2	$V_{THN2}$	As per Table 2	As per Table 2	-	-	4.1	V
71 to 80	Threshold Voltage P-Channel 1	$V_{THP1}$	As per Table 2	As per Table 2	-	1.0	-	V
81 to 90	Threshold Voltage P-Channel 2	$V_{THP2}$	As per Table 2	As per Table 2	-	1.0	-	V

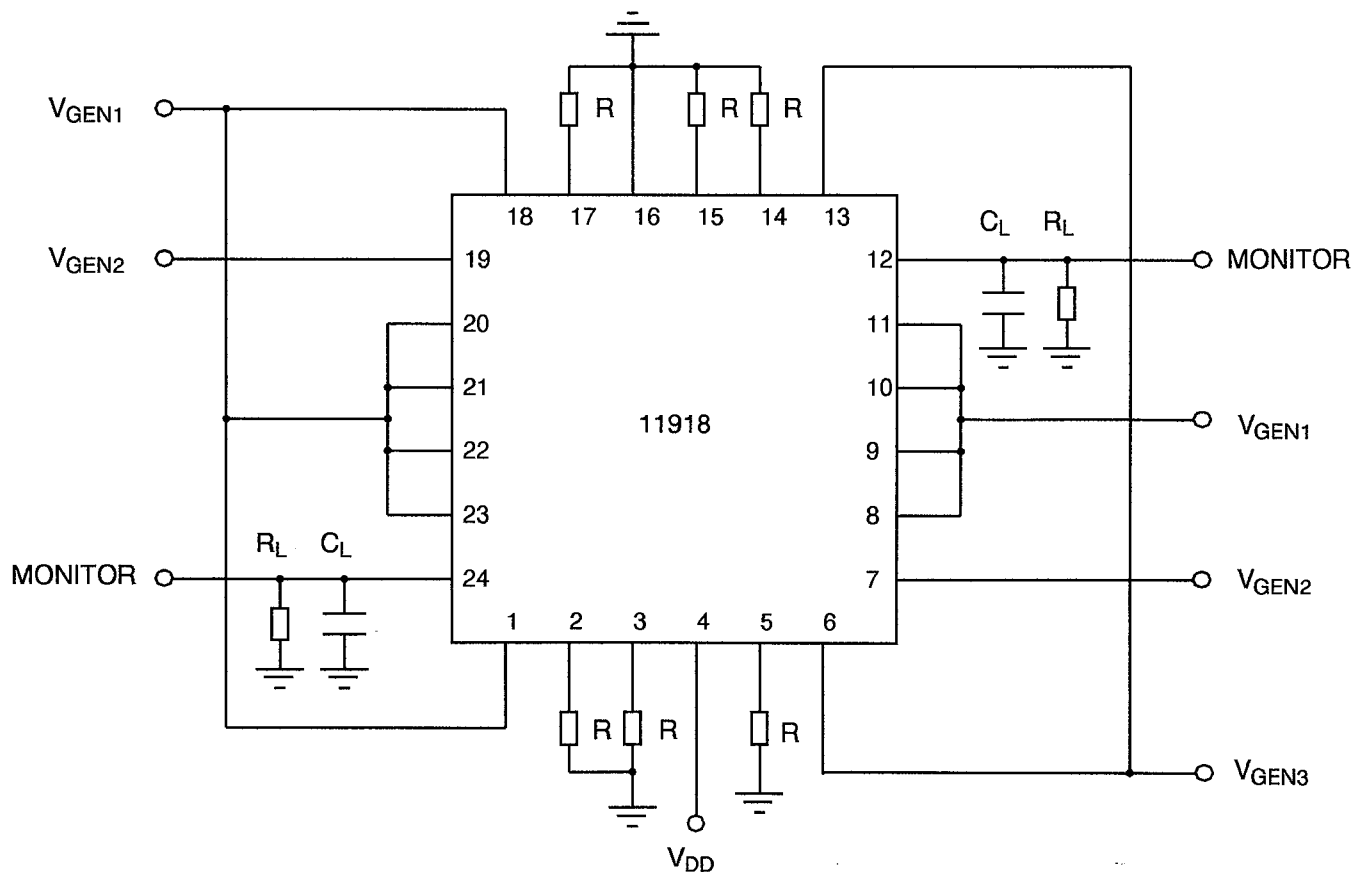


**FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING**

NO	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Outputs - (Pins 12-24)	$V_{OUT}$	Note 2	-
2	Inputs - (Pins 1-8-9-10-11-18-20-21-22-23)	$V_{IN}$	$V_{GEN1}$	Vac
3	Inputs - (Pins 7-19)	$V_{IN}$	$V_{GEN2}$	Vac
4	Inputs - (Pins 6-13)	$V_{IN}$	$V_{GEN3}$	Vac
5	Inputs - (Pins 2-3-5-14-15-17)	$V_{IN}$	Ground	V
6	Pulse Voltage	$V_{GEN}$	0 to $V_{DD}$	Vac
7	Pulse Frequency Square Wave	$f_{GEN1}$ $f_{GEN2}$ $f_{GEN3}$	1.0 0.5 0.05 50% Duty Cycle	MHz
8	Positive Supply Voltage (Pin 4)	$V_{DD}$	5.0 ( $\pm 0.5$ )	V
9	Negative Supply Voltage (Pin 16)	$V_{SS}$	Ground	V

**NOTES**

1. Input Load = Protection Resistor =  $R = 4.7k\Omega$ .
2. Output Load =  $R_L = 1.0M\Omega$  and  $C_L = 100pF$ .



**TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION  
OF IRRADIATION TESTING**

NO	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITION	CHANGE LIMITS ( $\Delta$ )	ABSOLUTE		UNIT
						MIN	MAX	
1A	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
1B	Functional Test	-	As per Table 2	As per Table 2	-	-	-	-
2	Quiescent Current	$I_{DD}$	As per Table 2	As per Table 2	-	-	300	$\mu$ A
3 to 22	Input Current Low Level	$I_{IL}$	As per Table 2	As per Table 2	-	-	450	nA
23 to 42	Input Current High Level	$I_{IH}$	As per Table 2	As per Table 2	-	-	450	nA
43 to 44	Output Voltage Low Level	$V_{OL}$	As per Table 2	As per Table 2	-	-	0.4	V
45 to 46	Output Voltage High Level	$V_{OH}$	As per Table 2	As per Table 2	-	2.8	-	V
51 to 60	Threshold Voltage N-Channel 1	$V_{THN1}$	As per Table 2	As per Table 2	$\pm 0.7$	-	-	V
61 to 70	Threshold Voltage N-Channel 2	$V_{THN2}$	As per Table 2	As per Table 2	$\pm 0.7$	-	-	V
71 to 80	Threshold Voltage P-Channel 1	$V_{THP1}$	As per Table 2	As per Table 2	$\pm 0.7$	-	-	V
81 to 90	Threshold Voltage P-Channel 2	$V_{THP2}$	As per Table 2	As per Table 2	$\pm 0.7$	-	-	V

**SCC**ESA/SCC Detail Specification  
No. 9204/063

Rev. 'A'

PAGE 31

ISSUE 2

**APPENDIX 'A'**Page 1 of 1**AGREED DEVIATIONS FOR MITEL (S)**

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.3	(a) Para. 9.9.2, Electrical Measurements at High and Low Temperatures: May be performed after Paras. 9.8.1 and 9.8.2, Seal Test.