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INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS SILICON GATE, STATIC, 16K (16348 x 1 BIT)

ASYNCHRONOUS RANDOM ACCESS MEMORY

WITH 3-STATE OUTPUTS,

BASED ON TYPES HM65262 AND HM65262B

ESA/SCC Detail Specification No. 9301/018

SCC

space components
coordination group

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		P26	Table 3 : No. 86 and No. 87, minimum limit amended	23576
		P36	Table 6 : Nos. 16 to 32, Nos. 33 to 49, No. 86 and No. 87, minimum limit amended	23576
		P39	Table 7 : Nos. 16 to 32, Nos. 33 to 49, No. 86 and No. 87, minimum limit amended	23576

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1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, CMOS Silicon Gate, Static, 16K (16348 x 1 BIT) Asynchronous Random Access Memory with 3-State Outputs, based on Types HM65262 and HM65262B. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 1 with a Minimum Critical Path Failure Voltage of 500 Volts.

1.11 INPUT PROTECTION NETWORK

Double diode protection shall be incorporated into each input as shown in Figure 3(e).

TABLE 1(a) - TYPE VARIANTS

VARIANT	BASED ON TYPE	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
01	HM65262	DIL	2(a)	D2
02	HM65262	CCP	2(b)	2
03	HM65262B	DIL	2(a)	D2
04	HM65262B	CCP	2(b)	2

TABLE 1(b) - MAXIMUM RATINGS

NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_{DD}	−0.3 to +7.0	V	Note 1
2	Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V	Note 2 Power On
3	D.C. Input Current	$\pm I_{IN}$	1.0	mA	
4	Output Current	$\pm I_{OUT}$	100	mA	Note 3
5	Device Dissipation (Continuous)	P_D	440	mW	Per Package
6	Operating Temperature Range	T_{op}	−55 to +125	°C	T_{amb}
7	Storage Temperature Range	T_{stg}	−65 to +165	°C	
8	Soldering Temperature For DIP For CCP	T_{sol}	 +300 +245	°C	 Note 4 Note 5
9	Thermal Resistance Variants 01 and 03 Variants 02 and 04	$R_{TH(J-A)}$	 65 60	°C/W	
10	Junction Temperature	T_J	165	°C	

NOTES

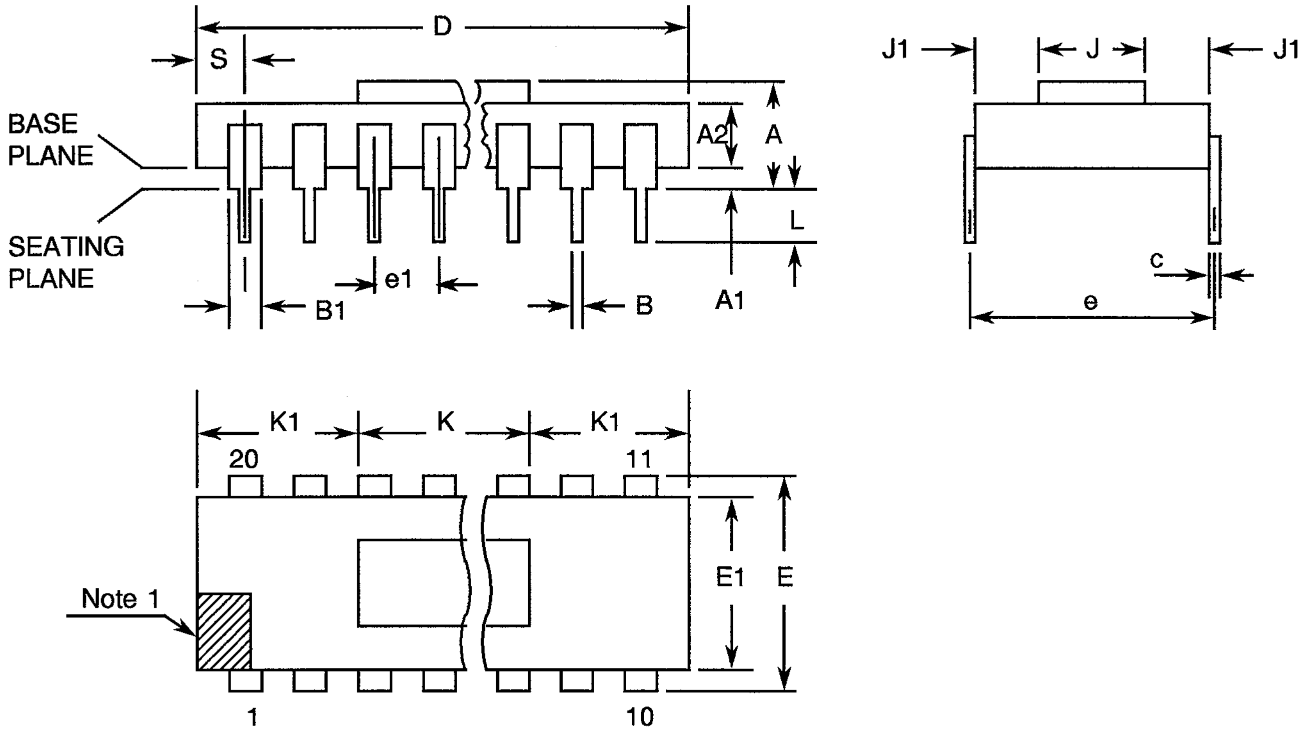
1. Device is functional from +4.5V to +5.5V with reference to Ground.
2. V_{DD} +0.3V should not exceed +7.0V.
3. The maximum output current of any single output.
4. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
5. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION

Not applicable

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - DUAL-IN-LINE PACKAGE, 20 PIN

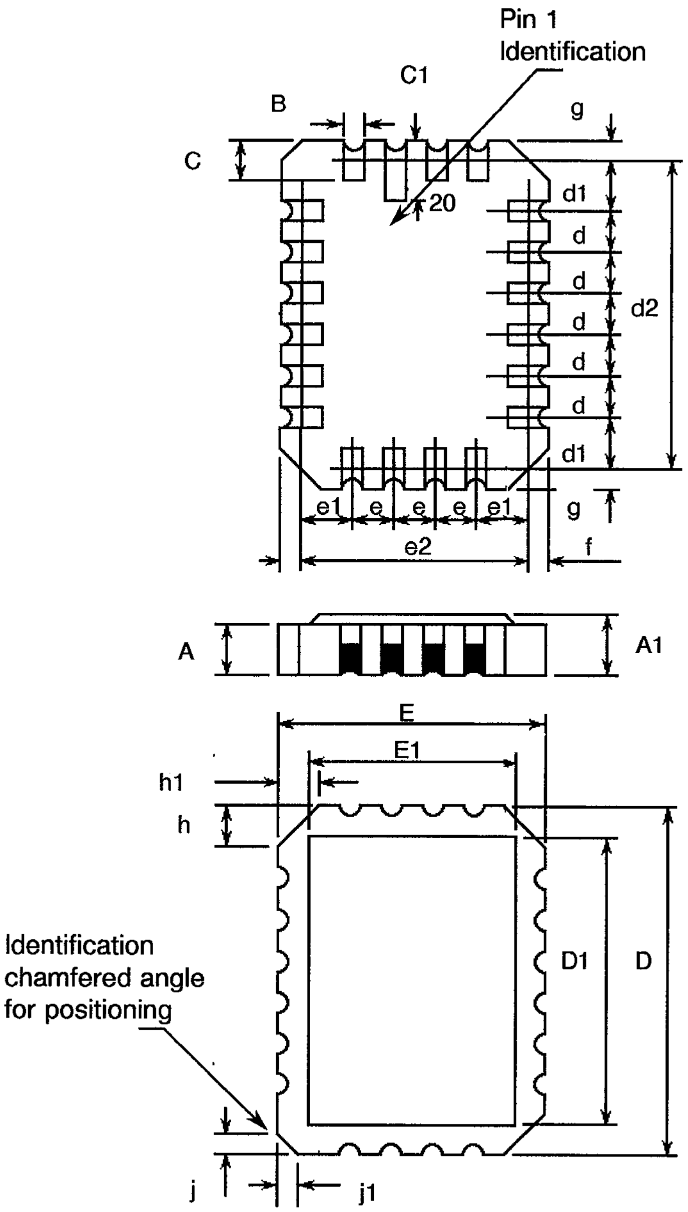


SYMBOL	MILLIMETERS		NOTES
	MIN.	MAX.	
A	2.82	3.94	
A1	0.63	1.14	3
A2	2.06	2.51	
B	0.38	0.53	8
B1	1.22	1.32	8
c	0.20	0.30	8
D	25.14	25.65	
E	7.37	8.25	4
E1	7.49TYPICAL		
e	7.62TYPICAL		
e1	2.54 TYPICAL		6,9
J	5.71 TYPICAL		
J1	0.89 TYPICAL		
K	11.68 TYPICAL		
K1	6.86 TYPICAL		
L	3.18	4.44	8
S	2.41	2.67	7

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - CHIP CARRIER, 20-TERMINAL



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.37	1.68	
A1	1.62	1.98	
B	0.53	0.76	8
C	1.02	1.27	8
C1	2.22 TYPICAL		
D	10.64	10.94	
D1	10.29 TYPICAL		
d, d1	1.27 TYPICAL		5, 9
d2	9.65 TYPICAL		
E	7.21	7.52	
E1	6.73 TYPICAL		
e, e1	1.27 TYPICAL		5, 9
e2	6.22 TYPICAL		
f, g	–	0.76	
h, h1	0.51 TYPICAL		10
j, j1	0.25 TYPICAL		11

NOTES: See Page 9.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

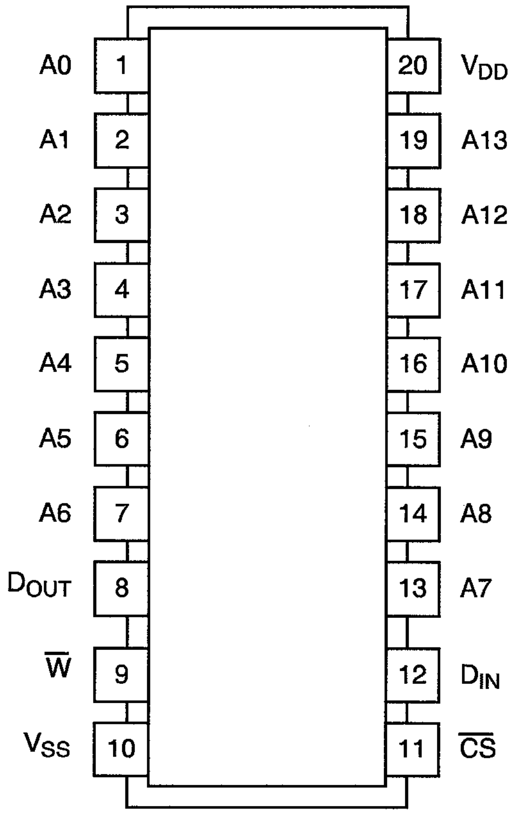
NOTES TO FIGURES 2(a) TO 2(b) INCLUSIVE

1. Index area: a notch, letter or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(b).
2. Not applicable.
3. The dimension shall be measured from the seating plane to the base plane.
4. The dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within 0.13mm of its true longitudinal position relative to Pin 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within 0.25mm of its true longitudinal position relative to Pin 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 18 spaces for dual-in-line packages.

   16 spaces for chip carrier packages.
10. 3 non-index corners - 6 dimensions.
11. Index corner only - 2 dimensions.

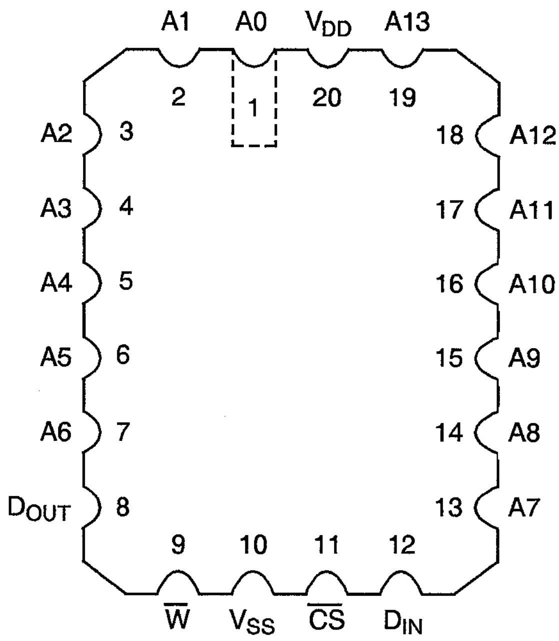
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

NOTES

1. AO to A13 = Address Inputs
2. D_{IN} = Data Inputs
3. $\overline{W}$ = Write Enable
4. $\overline{CS}$ = Chip Select
5. D_{OUT} = Data Output

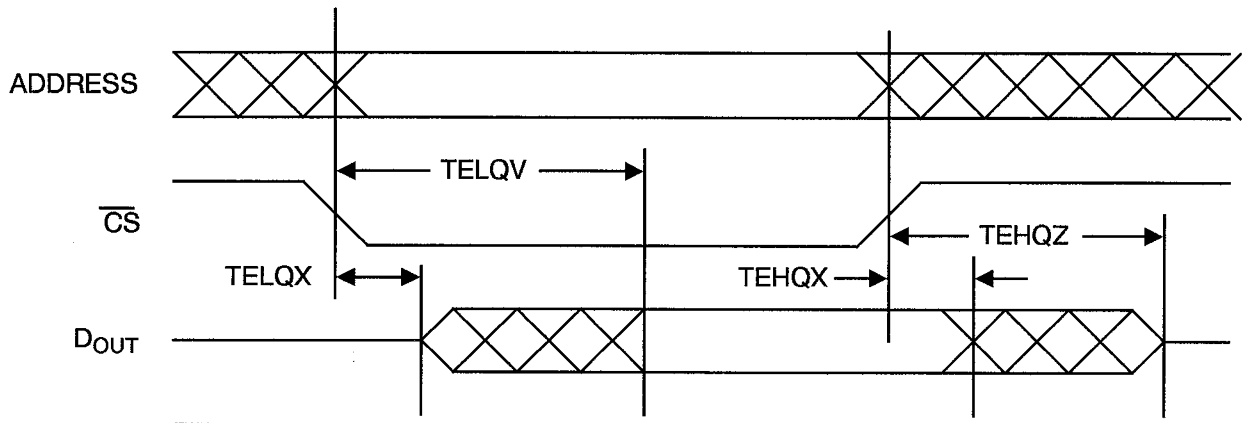
FIGURE 3(b) - TRUTH TABLE

$\overline{CS}$	$\overline{W}$	D_{IN}	D_{OUT}	MODE
H	X	Z	Z	Deselect
L	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

NOTES 1. Logic Level Definitions, L = Low Level, H = High Level, Z = High Impedance, X = Irrelevant.

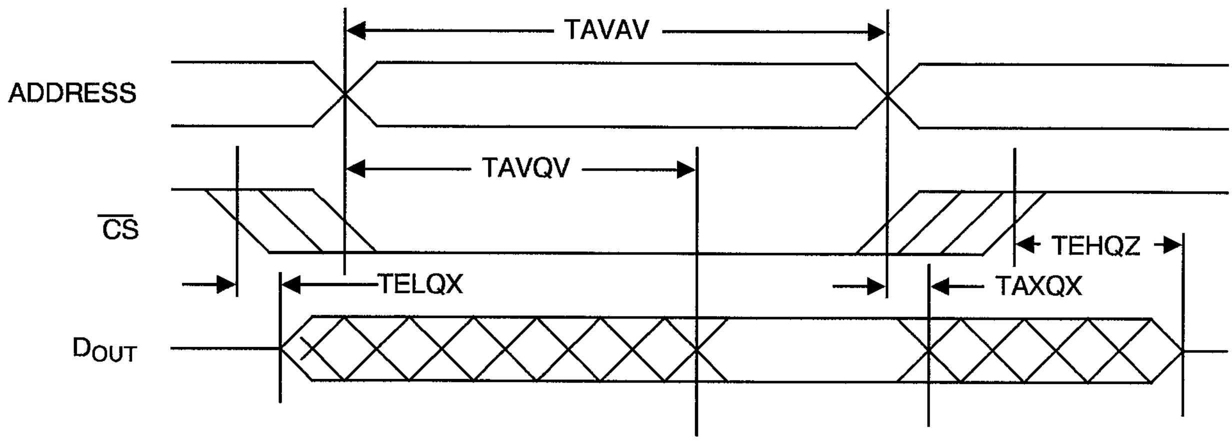
TIMING WAVEFORMS

READ CYCLE 1



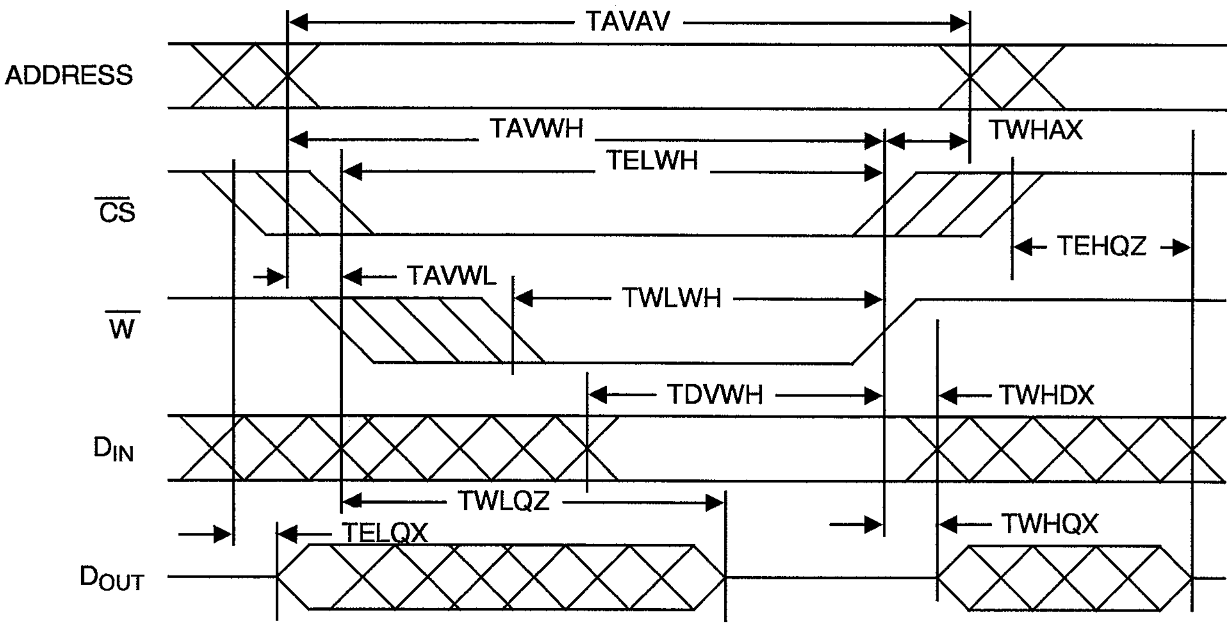
NOTES 1. $\overline{W}$ is High throughout Read Cycle

READ CYCLE 2



NOTES 1. $\overline{W}$ is High throughout Read Cycle

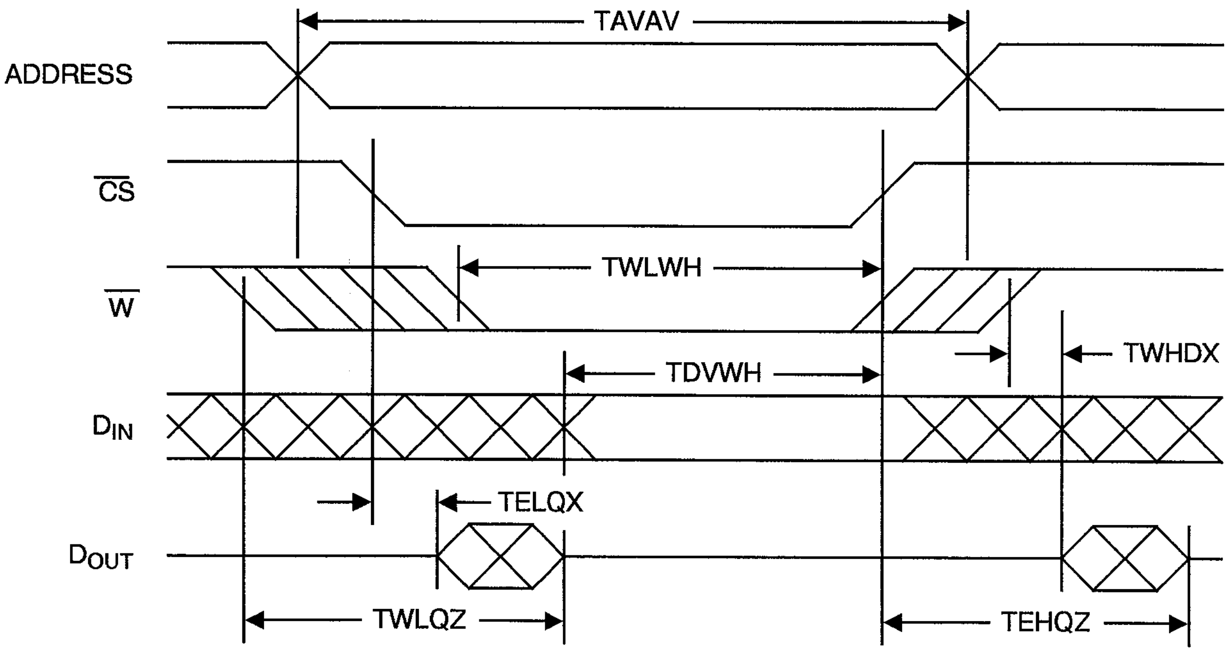
WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



NOTES

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{W}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



NOTES

1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ Low and $\overline{W}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

FIGURE 3(c) - CIRCUIT SCHEMATIC

Not applicable

FIGURE 3(d) - FUNCTIONAL DIAGRAM

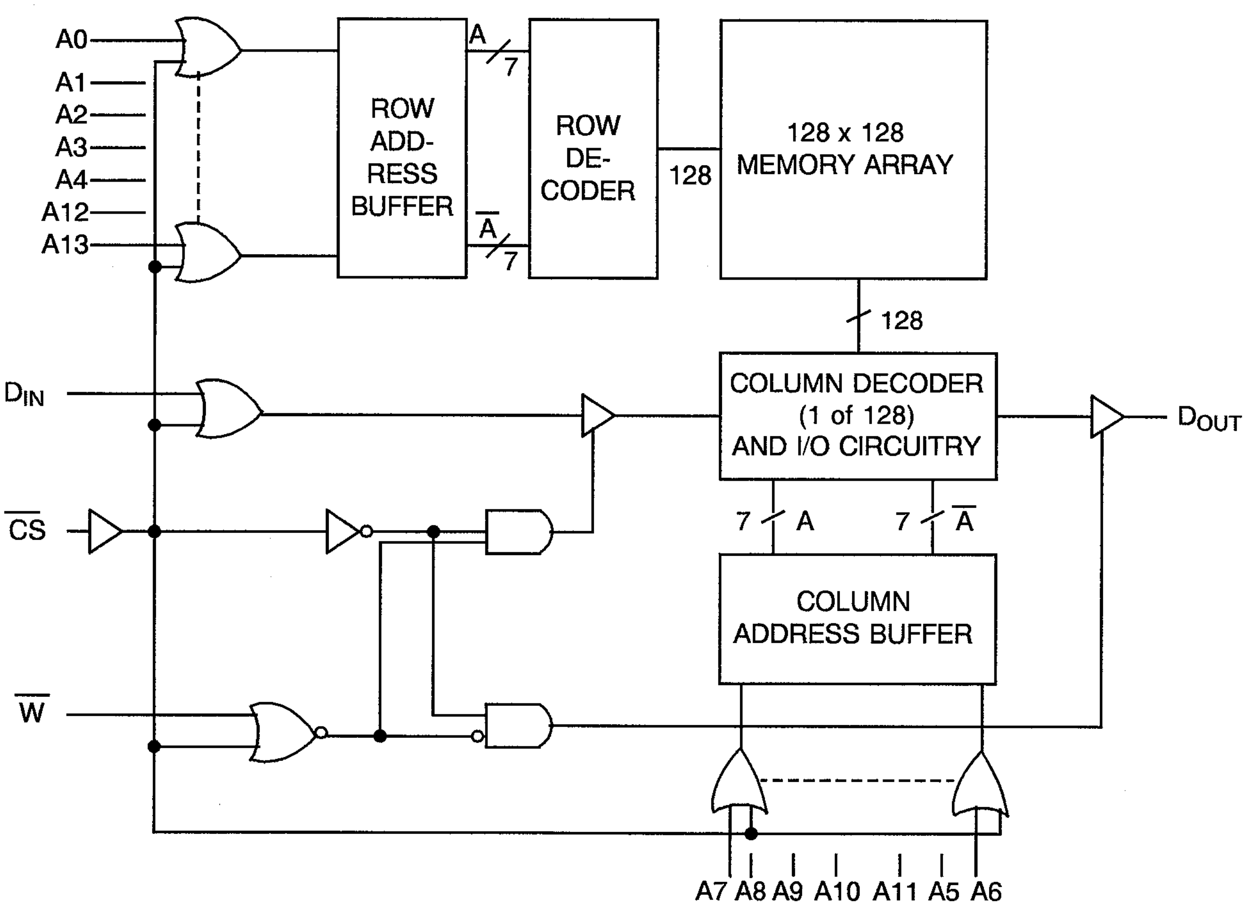
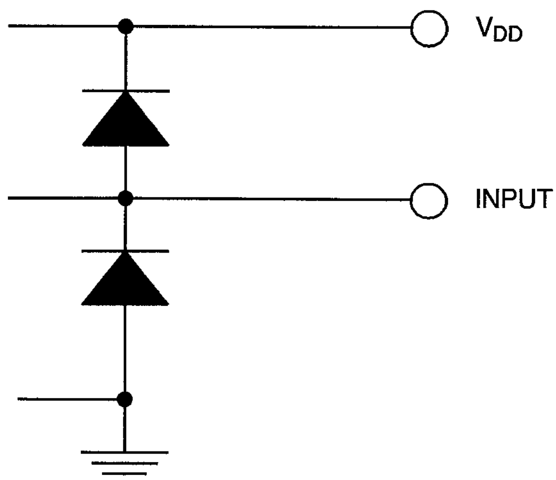


FIGURE 3(e) - INPUT PROTECTION NETWORK



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

V_{IC} = Input Clamp Voltage.

I_{OZL} = Output Leakage Current Third State (Low Level Applied)

I_{OZH} = Output Leakage Current Third State (High Level Applied)

C_{IN} = Input Capacitance.

C_{OUT} = Output Capacitance

TAVAV = Cycle Time.

TAVQV = Address Access Time

TELQV = $\overline{CS}$ Access Time.

TELQX = $\overline{CS}$ Low Output Enable Time.

TGLQV = Output Enable Access Time.

TEHQZ = $\overline{CS}$ High Output Disable Time.

TAVQX = Output Change from Address Change.

TELWH = $\overline{CS}$ Low to End of Write.

TAVWL = Address Set-up Time.

TWLWH = $\overline{W}$ Low Pulse Width.

TWHAX = Address Hold from Write End.

TWLQZ = $\overline{W}$ Low Output Disable Time.

TDVWH = Data Set-up Time.

TWHDX = Data Hold Time.

TWHQX = $\overline{W}$ High Output Enable Time

TAVWH = Address Valid to Write End.

t_r = Recovery Time from Data Retention.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during irradiation qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during procurement on an irradiation lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) The electrical measurements specified at the end of Subgroup I and II tests shall be carried out as stated in Table 2 of this specification.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) The electrical measurements referenced 9.9.4 shall be performed as stated in Table 2 of this specification.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.0 grammes for the dual-in-line package and 0.5 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be brazed or preform-soldered.

4.4.2 Lead Material and Finish

For dual-in-line packages, the material shall be Type 'D' with Type '2' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be Type '2' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(b).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

930101801BF

Detail Specification Number
Type Variant (see Table 1(a))
Testing Level (B or C, as applicable)
Total Dose Irradiation Level (if applicable)

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code letter shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and test sequences for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to Power Burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ), applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1 to 6	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input Conditions and Test Patterns, see Note 1	-	-	-
7	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input Conditions and Test Patterns, see Note 1	-	-	-
8 to 15	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input Conditions and Test Patterns, see Note 1	-	-	-
16 to 32	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	−1.0	+1.0	μA
33 to 49	Input Current High Level	I_{IH}	3010	4(b)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	−1.0	+1.0	μA
50	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0V, V_{IH} = 3.0V I_{OL} = 8.0mA, $V_{IN(\overline{W})}$ = 4.5V $V_{IN(\overline{CS})}$ = 0V, V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pin 8)	-	0.4	V
51	Output Voltage High Level	V_{OH}	3006	4(d)	V_{IL} = 0V, V_{IH} = 3.0V I_{OH} = -4.0mA, $V_{IN(\overline{W})}$ = 4.5V $V_{IN(\overline{CS})}$ = 0V V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 8)	2.4	-	V

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
52 to 68	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(e)	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	−0.2	−2.0	V
69 to 85	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(e)	I_{IN} (Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	0.2	2.0	V
86	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	-	4(f)	$V_{IN(\overline{CS})(\overline{W})}$ = 0V V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pin 8)	−1.0	+1.0	µA
87	Output Leakage Current Third State (High Level Applied)	I_{OZH}	-	4(f)	$V_{IN(\overline{CS})(\overline{W})}$ = 0V V_{OUT} = 5.0V V_{DD} = 5.5V, V_{SS} = 0V (Pin 8)	−1.0	+1.0	µA
88	Supply Current (Operating)	I_{DDop}	3005	4(g)	$V_{IN(\overline{CS})}$ = 0.8V V_{IN} (Remaining Inputs) = 0V to 3.0V f = 2.5MHz Pattern: ICCACT I_{OUT} = 0mA V_{DD} = 5.5V, V_{SS} = 0V (Pin 20)	-	57.5	mA
89	Supply Current (Enabled)	I_{DDE}	3005	4(g)	$V_{IN(\overline{CS})}$ = 0.8V V_{IN} (Remaining Inputs) = 0.8V I_{OUT} = 0mA (Pin 20)	-	50	mA
90	Supply Current (Standby 1)	I_{DDSB1}	3005	4(g)	$V_{IN(\overline{CS})}$ = 2.2V V_{IN} (Remaining Inputs) = 0.8V I_{OUT} = 0mA V_{DD} = 5.5V, V_{SS} = 0V (Pin 20)	-	5.0	mA

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
91 to 94	Supply Current (Standby 2)	I_{DDSB2}	3005	4(g)	$V_{IN(\overline{CS})}$ = V_{DD} − 0.3V V_{IN} (Remaining Inputs) = V_{DD} − 0.3V to − 0.3V I_{OUT} = 0mA V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 20)	-	50	µA
95	Data Retention Current	I_{DDDR}	3005	4(h)	V_{IL} = 0V, V_{IH} = 2.0V $V_{IN(\overline{CS})}$ = 2.0V V_{DD} = 2.0V, V_{SS} = 0V Note 4 (Pin 20)	-	20	µA
96 to 97	Data Retention	DR	-	-	V_{IL} = 0V, V_{IH} = 3.0V $V_{IN(\overline{CS})}$ = 4.5V V_{DD} = 4.5V, V_{SS} = 0V Note 5 (Pin 8)	-	-	-

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS MIN	LIMITS MAX	UNIT
98 to 114	Input Capacitance	C_{IN}	3012	4(i)	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V Note 6 (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	-	5.0	pF
115	Output Capacitance	C_{OUT}	3012	4(j)	V_{IN} (Not Under Test) = 0V V_{DD} = V_{SS} = 0V Note 6 (Pin 8)	-	7.0	pF
116 to 121	Functional Test 4	-	3014	3(b)	Verify Truth Table. For Input and Output Conditions, see Notes 7 and 8 V_{DD} = 4.5V and 5.5V V_{SS} = 0V	-	-	-
122 to 123	Access Time (Address)	TAVQV	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01 and 02 Variants 03 and 04	 - -	 85 70	ns
124 to 125	Access Time (Chip Select)	TELQV	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 9 Variants 01 and 02 Variants 03 and 04	 - -	 85 70	ns
126 to 127	Write Pulse Width ($\overline{W}$ Low)	TWLWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10 Variants 01 and 02 Variants 03 and 04	 65 50	 - -	ns
128 to 129	Data Set-up Time	TDVWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10 Variants 01 and 02 Variants 03 and 04	 45 40	 - -	ns
130 to 131	Data Hold Time	TWHDX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10	0	-	ns

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
132 to 133	Read/Write Cycle Time	TAVAV	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10 Variants 01 and 02 Variants 03 and 04	 85 70	 - -	ns
134 to 135	Output Change from Address Cycle	TAVQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10	5.0	-	ns
136 to 137	$\overline{CS}$ Low to End of Write	TELWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10 Variants 01 and 02 Variants 03 and 04	 65 55	 - -	ns
138 to 139	Address Set-up Time	TAVWL	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10	0	-	ns
140 to 141	Address Valid to End of Write	TAVWH	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10 Variants 01 and 02 Variants 03 and 04	 65 55	 - -	ns
142 to 143	Address Hold from Write End	TWHAX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 7 and 10	0	-	ns
144 to 145	Output Enable Time (CS Low)	TELQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 7	5.0	-	ns
146 to 147	Output Disable Time (CS High)	TEHQZ	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 7	-	40	ns
148 to 149	Output Disable Time (W Low)	TWLQZ	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 7 Variants 01 and 02 Variants 03 and 04	 -	 50 40	ns
150 to 151	Output Enable Time (W High)	TWHQX	-	4(k)	V_{DD} = 4.5V and 5.5V V_{SS} = 0V Notes 6 and 7	0	-	ns

NOTES: See Page 23.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONTINUED)

NOTES

1. Functional test go-no-go with the following test sequences:-

FUNCTIONAL TEST 1

Pattern	Timing	V_{DD}	V_{SS}	V_{IL}	V_{IH}	I_{OL}	I_{OH}	V_{OUT} (COMP)
MARCH, COMARCH	1.0µS	4.5V and 5.5V	0V	0V	3.0V	0.5mA	−0.5mA	1.5V
CHECKERBOARD	1.0µS	4.5V and 5.5V	0V	0V	3.0V	0.5mA	−0.5mA	1.5V

FUNCTIONAL TEST 2

Pattern	Timing	V_{DD}	V_{SS}	V_{IL}	V_{IH}	I_{OL}	I_{OH}	V_{OUT} (COMP)
MARCH	1.0µS	5.0V	0V	−0.3V	5.3V	0.5mA	−0.5mA	1.5V

FUNCTIONAL TEST 3

Pattern	Timing	V_{DD}	V_{SS}	V_{IL}	V_{IH}	I_{OL}	I_{OH}	V_{OUT} (COMP)
MARCH	1.0µS	7.5V	0V	0V	7.5V	0.5mA	−0.5mA	1.5V
MARCH	1.0µS	4.5V	0V	0V	3.0V	0.5mA	−0.5mA	1.5V
MARCH	3.0µS	4.5V and 5.5V	0V	0.8V	2.2V	0.5mA	−0.5mA	1.5V
MARCH	3.0µS	4.5V and 5.5V	0V	0V	3.0V	4.0mA	−1.0mA	1.5V
CHIP DESELECT	1.0µS	4.5V	0V	0V	3.0V	0.5mA	−0.5mA	1.5V
LONG CHIP SELECT	2.5µS	4.5V	0V	0V	3.0V	0.5mA	−0.5mA	1.5V

2. Select Address Inputs to produce low level output at the pin under test in accordance with Figure 3(b).
3. Select Address Inputs to produce high level output at the pin under test in accordance with Figure 3(b).
4. Measurement is performed with the memory loaded with a background of zeros and then with a background of ones, for all inputs high and then low. Only worst case is recorded.
5. Data Retention Procedure:-
   (a) Write memory with Checkerboard pattern with Timing = 1µs at the conditions given.
   (b) Power Down to V_{DD} = 1.6 ± 0V for 250ms. (This is a test condition only. Memory retention cannot be guaranteed if V_{DD} is reduced below 2.0V).
   (c) Restore to original conditions given, read Memory and compare with original pattern.
   (d) Repeat the procedure with $\overline{\text{Checkerboard}}$ pattern with timing = 1µs at the conditions given.
   (e) For Variants 01 and 02: t_r = 85ns, for Variants 03 and 04: t_r = 70ns.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONTINUED)

NOTES

6. Guaranteed but not tested. Characterised at initial design and after major process changes.
7. Test Conditions
   Input Pulse Level = 0 to 3.0V
   Input t_r and t_f = 5.0ns (max.)
   Input/Output Timing Reference Level = 1.5V
   Output Load = 1 TTL Gate equivalent + $C_L \leq$ 100pF.
   f = 2.5MHz
8. Tested go-no-go using March, Comarch and Walkcol patterns.
9. Parameters measured using March pattern during Functional Test 4.
10. Parameters tested go-no-go during Functional Test 4.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
1 to 6	Functional Test 1 (Nominal Inputs)	-	3014	3(b)	Verify Truth Table. For Input Conditions and Test Patterns, see Note 1	-	-	-
7	Functional Test 2 (Worst Case Inputs)	-	3014	3(b)	Verify Truth Table. For Input Conditions and Test Patterns, see Note 1	-	-	-
8 to 15	Functional Test 3 (Worst Case Outputs)	-	3014	3(b)	Verify Truth Table. For Input Conditions and Test Patterns, see Note 1	-	-	-
16 to 32	Input Current Low Level	I_{IL}	3009	4(a)	V_{IN} (Under Test) = 0V V_{IN} (Remaining Inputs) = 5.5V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	−1.0	+1.0	µA
33 to 49	Input Current High Level	I_{IH}	3010	4(b)	V_{IN} (Under Test) = 5.5V V_{IN} (Remaining Inputs) = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	−1.0	+1.0	µA
50	Output Voltage Low Level	V_{OL}	3007	4(c)	V_{IL} = 0V, V_{IH} = 3.0V I_{OL} = 8.0mA, $V_{IN(\overline{W})}$ = 4.5V $V_{IN(\overline{CS})}$ = 0V, V_{DD} = 4.5V, V_{SS} = 0V Note 2 (Pin 8)	-	0.4	V
51	Output Voltage High Level	V_{OH}	3006	4(d)	V_{IL} = 0V, V_{IH} = 3.0V I_{OH} = -4.0mA, $V_{IN(\overline{W})}$ = 4.5V $V_{IN(\overline{CS})}$ = 0V V_{DD} = 4.5V, V_{SS} = 0V Note 3 (Pin 8)	2.4	-	V

NOTES: See Page 23.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
52 to 68	Input Clamp Voltage (to V_{SS})	V_{IC1}	-	4(e)	I_{IN} (Under Test) = -100µA V_{DD} = Open, V_{SS} = 0V All Other Pins Open (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	−0.2	−2.0	V
69 to 85	Input Clamp Voltage (to V_{DD})	V_{IC2}	-	4(e)	I_{IN} (Under Test) = 100µA V_{DD} = 0V, V_{SS} = Open All Other Pins Open (Pins 1-2-3-4-5-6-7-9-11-12-13-14-15-16-17-18-19)	0.2	2.0	V
86	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	-	4(f)	$V_{IN(\overline{CS})(\overline{W})}$ = 0V V_{OUT} = 0V V_{DD} = 5.5V, V_{SS} = 0V (Pin 8)	−1.0	+1.0	µA
87	Output Leakage Current Third State (High Level Applied)	I_{OZH}	-	4(f)	$V_{IN(\overline{CS})(\overline{W})}$ = 0V V_{OUT} = 5.0V V_{DD} = 5.5V, V_{SS} = 0V (Pin 8)	−1.0	+1.0	µA
88	Supply Current (Operating)	I_{DDop}	3005	4(g)	$V_{IN(\overline{CS})}$ = 0.8V V_{IN} (Remaining Inputs) = 0V to 3.0V f = 2.5MHz Pattern: ICCACT I_{OUT} = 0mA V_{DD} = 5.5V, V_{SS} = 0V (Pin 20)	-	57.5	mA
89	Supply Current (Enabled)	I_{DDE}	3005	4(g)	$V_{IN(\overline{CS})}$ = 0.8V V_{IN} (Remaining Inputs) = 0.8V I_{OUT} = 0mA (Pin 20)	-	50	mA
90	Supply Current (Standby 1)	I_{DDSB1}	3005	4(g)	$V_{IN(\overline{CS})}$ = 2.2V V_{IN} (Remaining Inputs) = 0.8V I_{OUT} = 0mA V_{DD} = 5.5V, V_{SS} = 0V (Pin 20)	-	5.0	mA

NOTES: See Page 23.

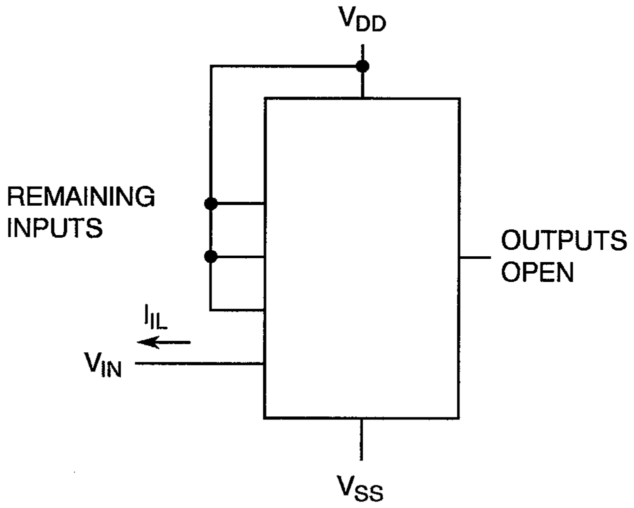
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST)	LIMITS		UNIT
						MIN	MAX	
91 to 94	Supply Current (Standby 2)	I_{DDSB2}	3005	4(g)	$V_{IN(\overline{CS})}$ = V_{DD} −0.3V V_{IN} (Remaining Inputs) = V_{DD} − 0.3V to −0.3V I_{OUT} = 0mA V_{DD} = 5.5V, V_{SS} = 0V Note 4 (Pin 20)	-	50	µA
95	Data Retention Current	I_{DDDR}	3005	4(h)	V_{IL} = 0V, V_{IH} = 2.0V $V_{IN(\overline{CS})}$ = 2.0V V_{DD} = 2.0V, V_{SS} = 0V Note 4 (Pin 20)	-	20	µA
96 to 97	Data Retention	DR	-	-	V_{IL} = 0V, V_{IH} = 3.0V $V_{IN(\overline{CS})}$ = 4.5V V_{DD} = 4.5V, V_{SS} = 0V Note 5 (Pin 8)	-	-	-

NOTES: See Page 23.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

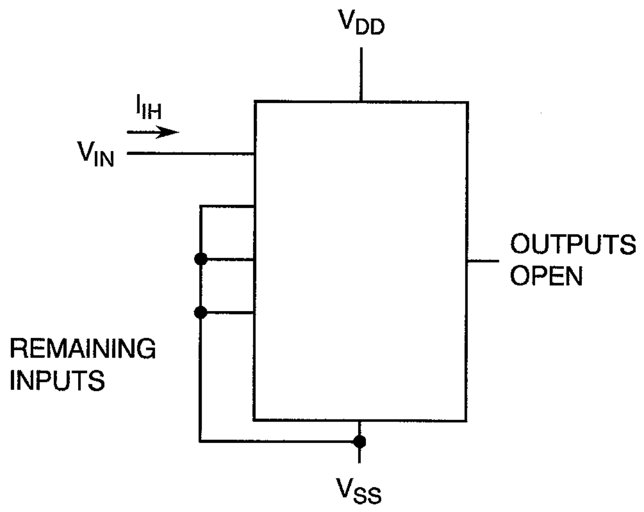
FIGURE 4(a) - INPUT CURRENT LOW LEVEL



NOTES

1. Each input to be tested separately.

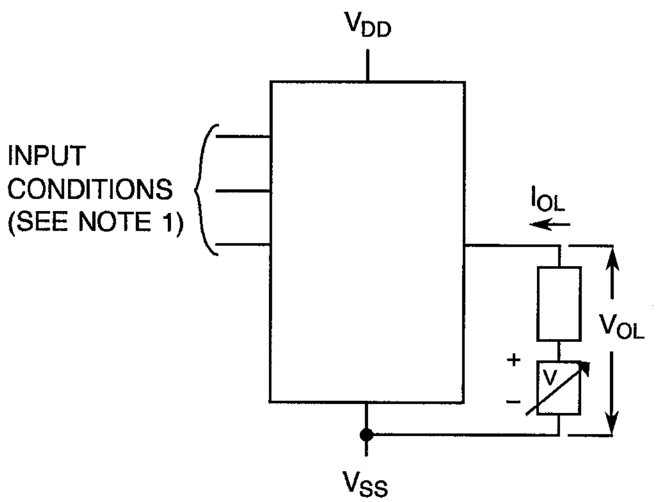
FIGURE 4(b) - INPUT CURRENT HIGH LEVEL



NOTES

1. Each input to be tested separately.

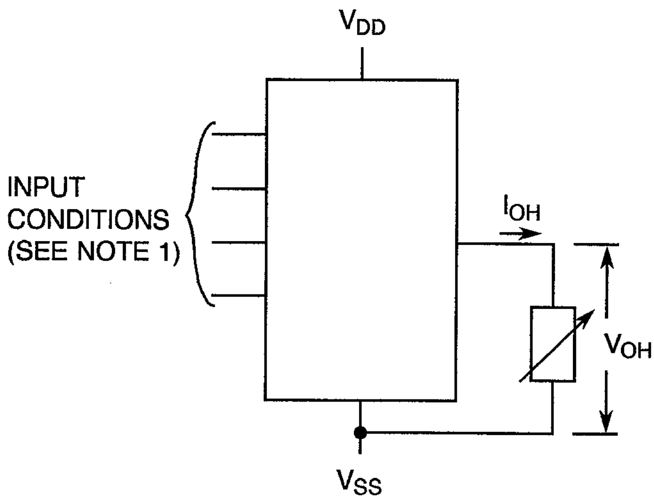
FIGURE 4(c) - OUTPUT VOLTAGE LOW LEVEL



NOTES

1. $V_{IN} = V_{IL}$ (max.) and/or V_{IH} (min.) as per Truth Table to give V_{OL}.
2. Each output to be tested separately.

FIGURE 4(d) - OUTPUT VOLTAGE HIGH LEVEL

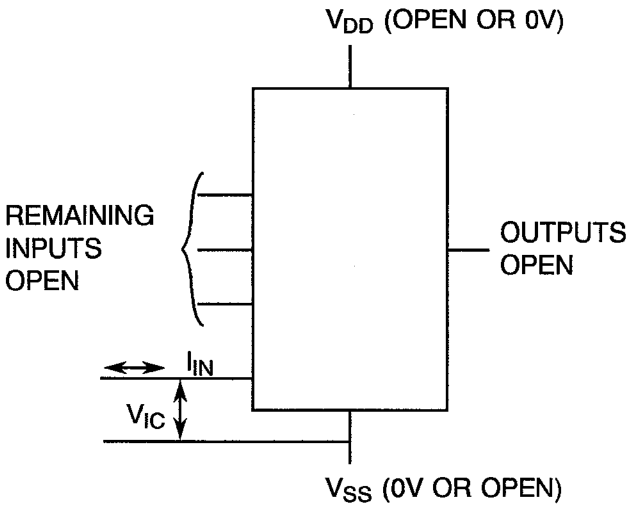


NOTES

1. $V_{IN} = V_{IL}$ (max.) and/or V_{IH} (min.) as per Truth Table to give V_{OH}.
2. Each output to be tested separately.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - INPUT CLAMP VOLTAGE



NOTES
1. Each input to be tested separately.

FIGURE 4(f) - OUTPUT LEAKAGE CURRENT THIRD STATE

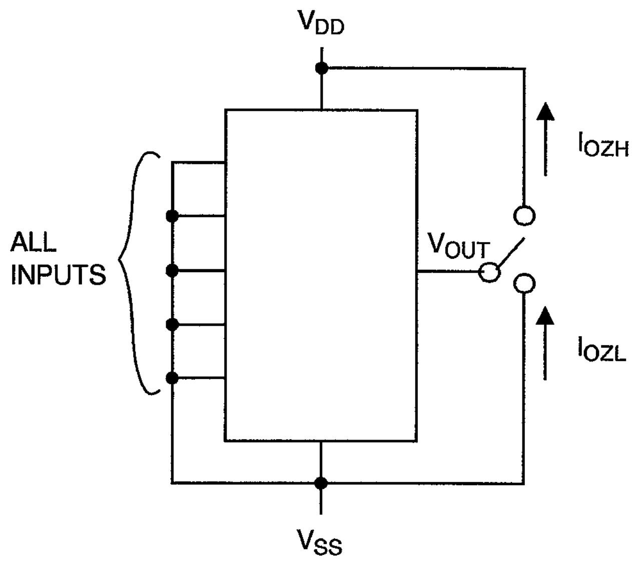
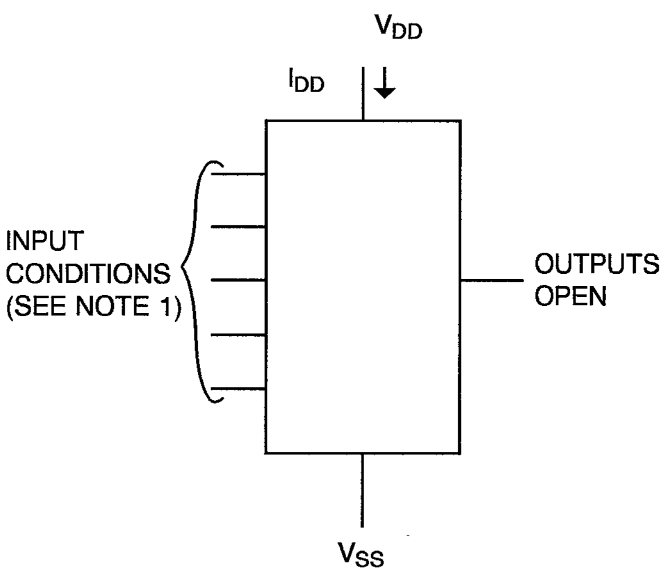
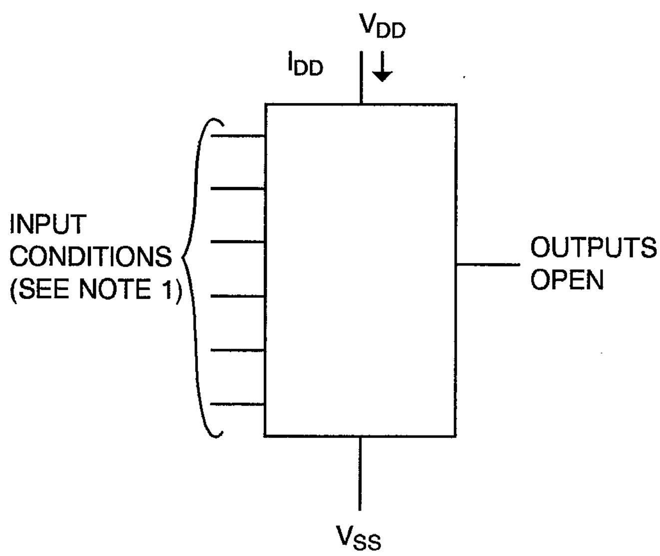


FIGURE 4(g) - SUPPLY CURRENT



NOTES
1. As per Table 2 or 3.

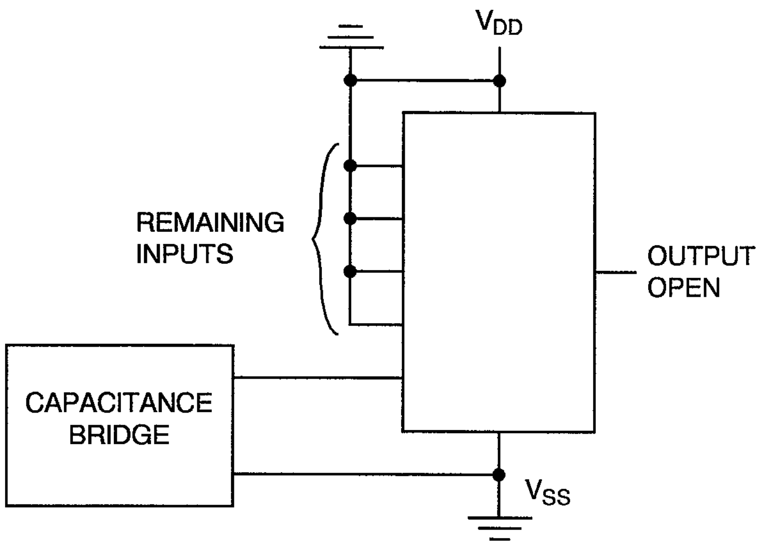
FIGURE 4(h) - DATA RETENTION CURRENT



NOTES
1. Procedure as per Note 4 to Table 2.

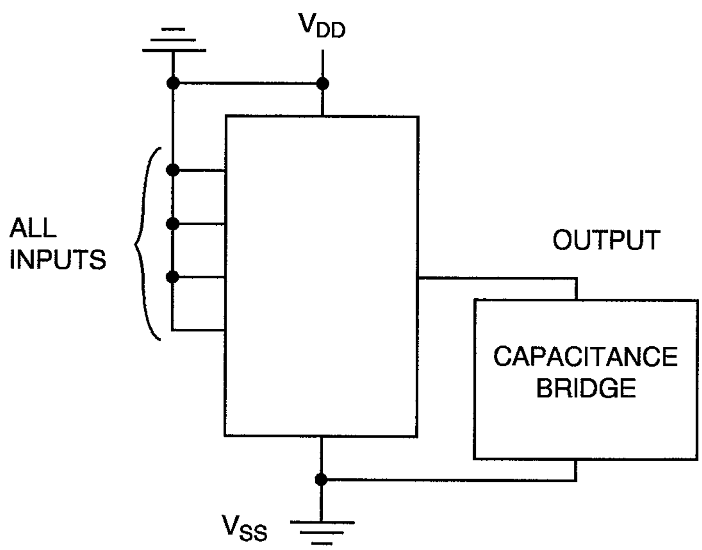
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - INPUT CAPACITANCE



NOTES
1. Each input to be tested separately.
2. f = 100kHz to 1MHz.

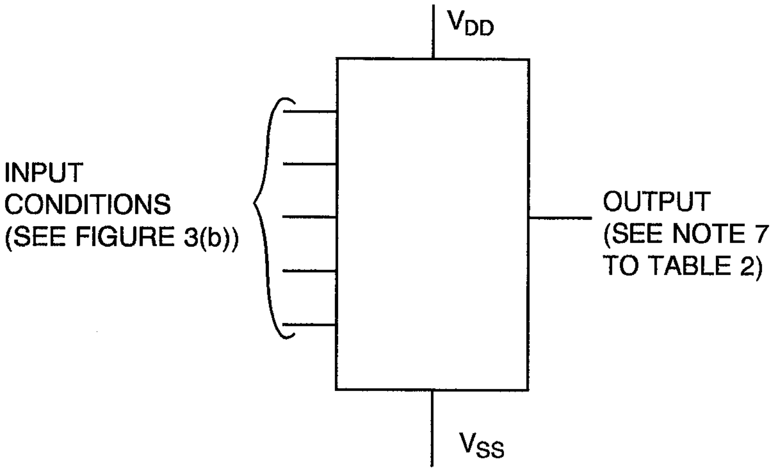
FIGURE 4(j) - OUTPUT CAPACITANCE



NOTES
1. f = 100kHz to 1MHz.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(k) - PROPAGATION DELAY



TIMING WAVEFORMS

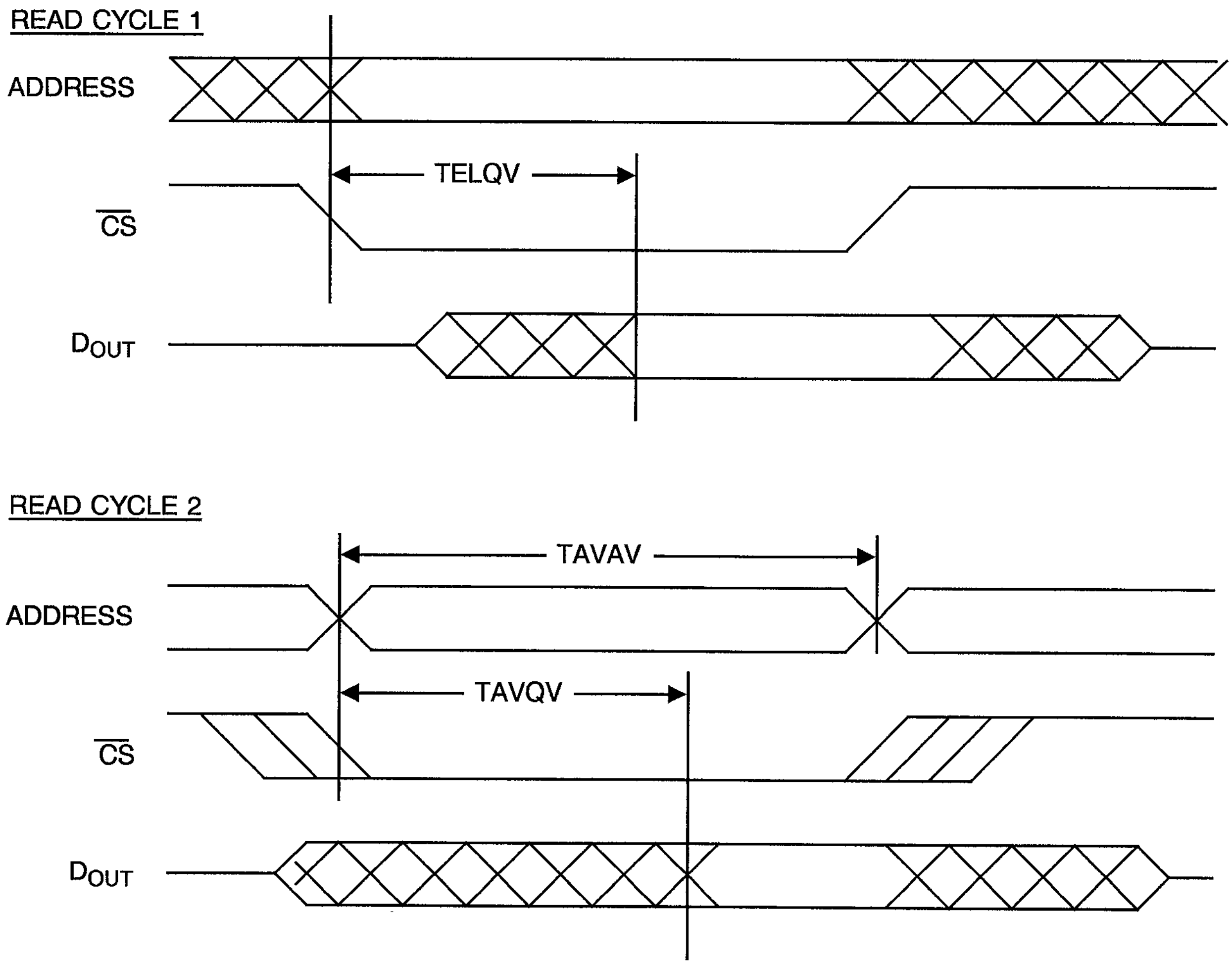


TABLE 4 - PARAMETER DRIFT VALUES

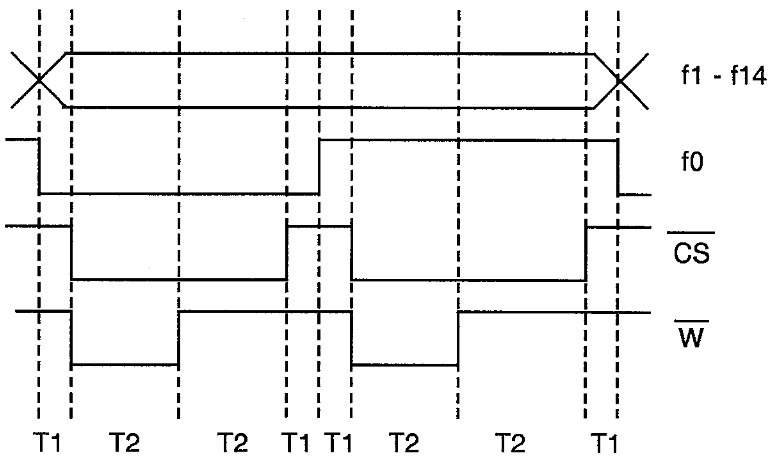
NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
16 to 32	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±100	nA
33 to 49	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	±100	nA
50	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±100	mV
51	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	±100	mV
90	Supply Current (Standby 1)	I_{DDSB1}	As per Table 2	As per Table 2	±0.5	mA
91 to 94	Supply Current (Standby 2)	I_{DDSB2}	As per Table 2	As per Table 2	±5.0	μA
95	Data Retention Current	I_{DDDR}	As per Table 2	As per Table 2	±5.0	μA

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST

NO.	CHARACTERISTICS	SYMBOL	CONDITIONS	UNIT
1	Ambient Temperature	T_{amb}	$+125(+0-5)$	°C
2	Inputs - (Pins 1-2-3-4-5-6-7-12-13-14-15-16-17-18-19)	V_{IN}	f_0 to f_{14}	Vac
3	Inputs - (Pins 9-11)	V_{IN}	$\overline{CS}$, $\overline{W}$ (Note 3)	Vac
4	Output - (Pin 8)	V_{OUT}	V_{SS} or V_{DD}	V
5	Pulse Voltage	V_{GEN}	0 to V_{DD}	Vac
6	Pulse Frequency	f_O	50k ±20% 50±15% Duty Cycle	Hz
7	Positive Supply Voltage (Pin 20)	V_{DD}	$5.0(+0.5-0)$	V
8	Negative Supply Voltage (Pin 10)	V_{SS}	0	V

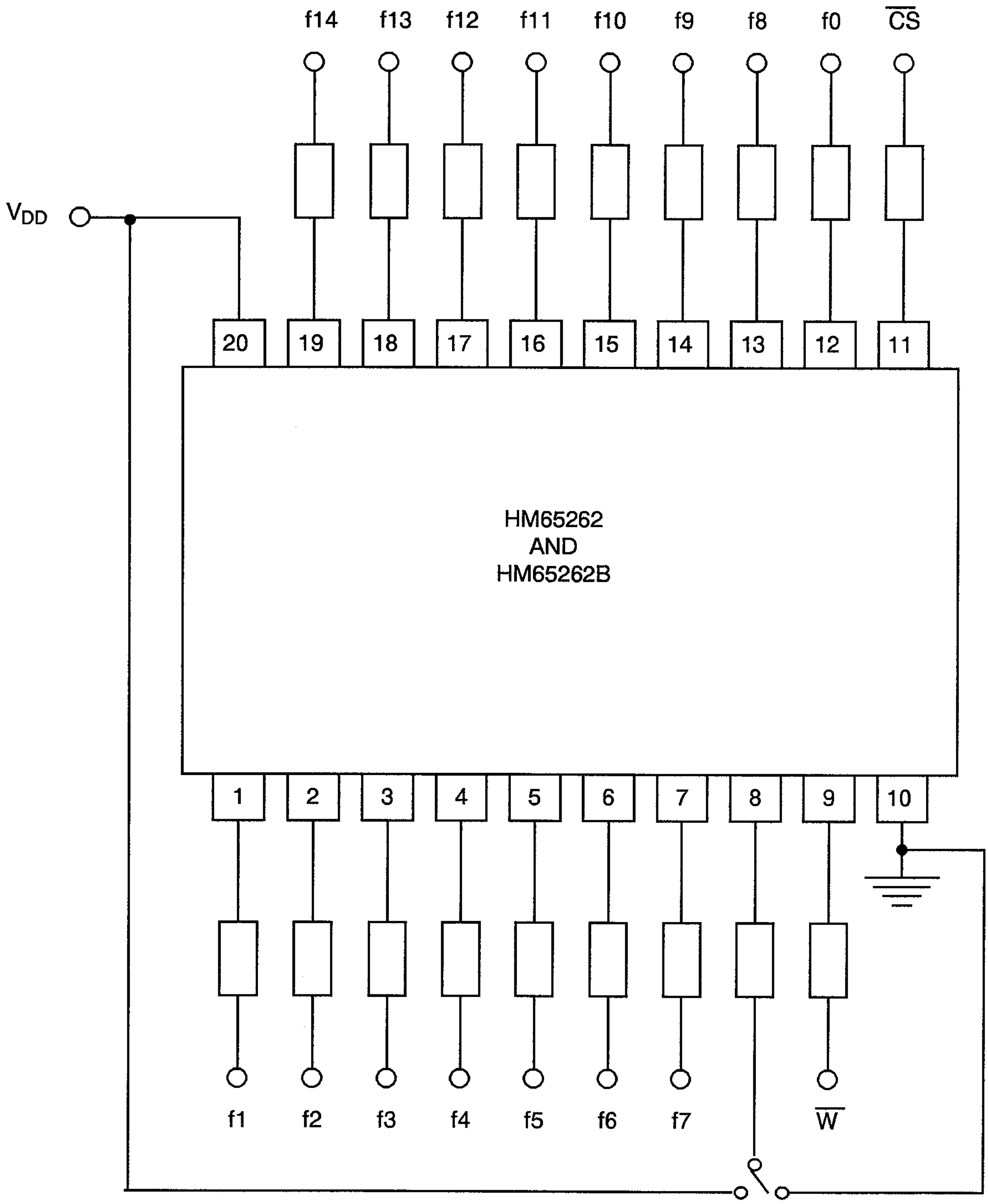
NOTES

1. Input Protection Resistor = 1.0kΩ.
2. Output Load Resistor = 1.0kΩ.
3. $fn = \frac{1}{2}(fn - 1)$.
4. Input Timing:



T1 = 0.61 us
T2 = 4.24 us

FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST



4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION No. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 2. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(c) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(c) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be included in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

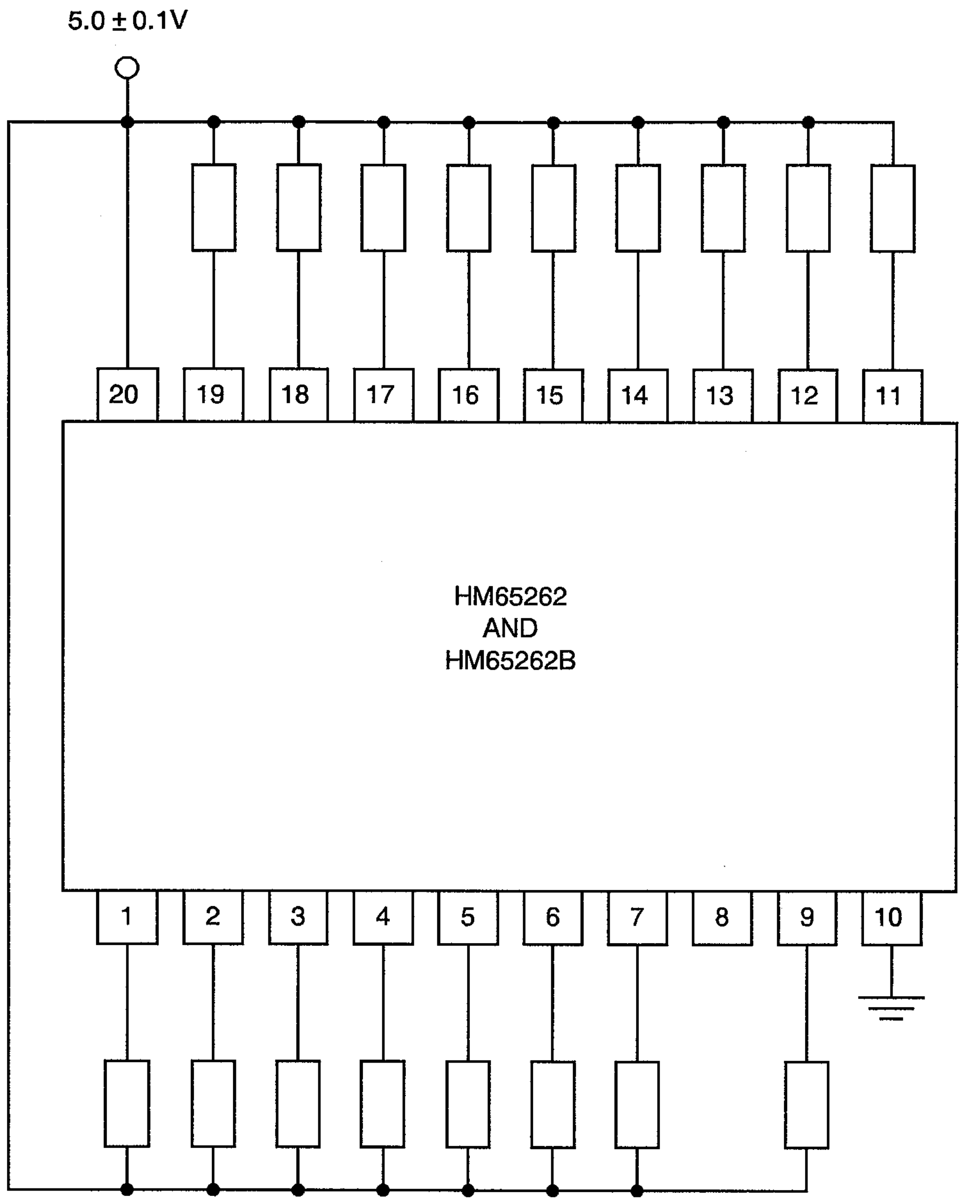
TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1 to 6	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-
7	Functional Test 2 (Worst Case Inputs)	-	As per Table 2	As per Table 2	-	-	-
8 to 15	Functional Test 3 (Worst Case Outputs)	-	As per Table 2	As per Table 2	-	-	-
16 to 32	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	−1.0	+1.0	µA
33 to 49	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	−1.0	+1.0	µA
50	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
51	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
52 to 68	Input Clamp Voltage (to V_{SS})	V_{IC1}	As per Table 2	As per Table 2	−0.2	−2.0	V
69 to 85	Input Clamp Voltage (to V_{DD})	V_{IC2}	As per Table 2	As per Table 2	0.2	2.0	V
86	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	−1.0	+1.0	µA
87	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	−1.0	+1.0	µA
88	Supply Current (Operating)	I_{DDop}	As per Table 2	As per Table 2	-	57.5	mA
89	Supply Current (Enabled)	I_{DDE}	As per Table 2	As per Table 2	-	50	mA

TABLE 6 - ELECTRICAL MEASUREMENTS AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING (CONTINUED)

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
90	Supply Current (Standby 1)	I_{DDSB1}	As per Table 2	As per Table 2	-	5.0	mA
91 to 94	Supply Current (Standby 2)	I_{DDSB2}	As per Table 2	As per Table 2	-	50	µA
95	Data Retention Current	I_{DDDR}	As per Table 2	As per Table 2	-	20	µA
96 to 97	Data Retention	DR	As per Table 2	As per Table 2	-	-	-

FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING



NOTES

1. Input Protection Resistor = 1.0kΩ.

TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1 to 6	Functional Test 1 (Nominal Inputs)	-	As per Table 2	As per Table 2	-	-	-
16 to 32	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	−1.0	+1.0	µA
33 to 49	Input Current High Level	I_{IH}	As per Table 2	As per Table 2	−1.0	+1.0	µA
50	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	-	0.4	V
51	Output Voltage High Level	V_{OH}	As per Table 2	As per Table 2	2.4	-	V
86	Output Leakage Current Third State (Low Level Applied)	I_{OZL}	As per Table 2	As per Table 2	−1.0	+1.0	µA
87	Output Leakage Current Third State (High Level Applied)	I_{OZH}	As per Table 2	As per Table 2	−1.0	+1.0	µA
91 to 94	Supply Current (Standby 2)	I_{DDSB2}	As per Table 2	As per Table 2	-	1.0	mA

APPENDIX 'A'

AGREED DEVIATIONS FOR MATRA-HARRIS (F)

The following test patterns may be used:-

ICCACT Pattern

(a) Write loop pattern between N min. and N max.

WALKOL Pattern

(a) Write a column of ones on a background of zeros.
(b) Read the column and background, step the column and repeat the read.
(c) Continue until all columns have been used.
(d) Repeat with data complement.
(e) 4YN + 2Y + 2 cycles.

CHIP DESELECT Pattern

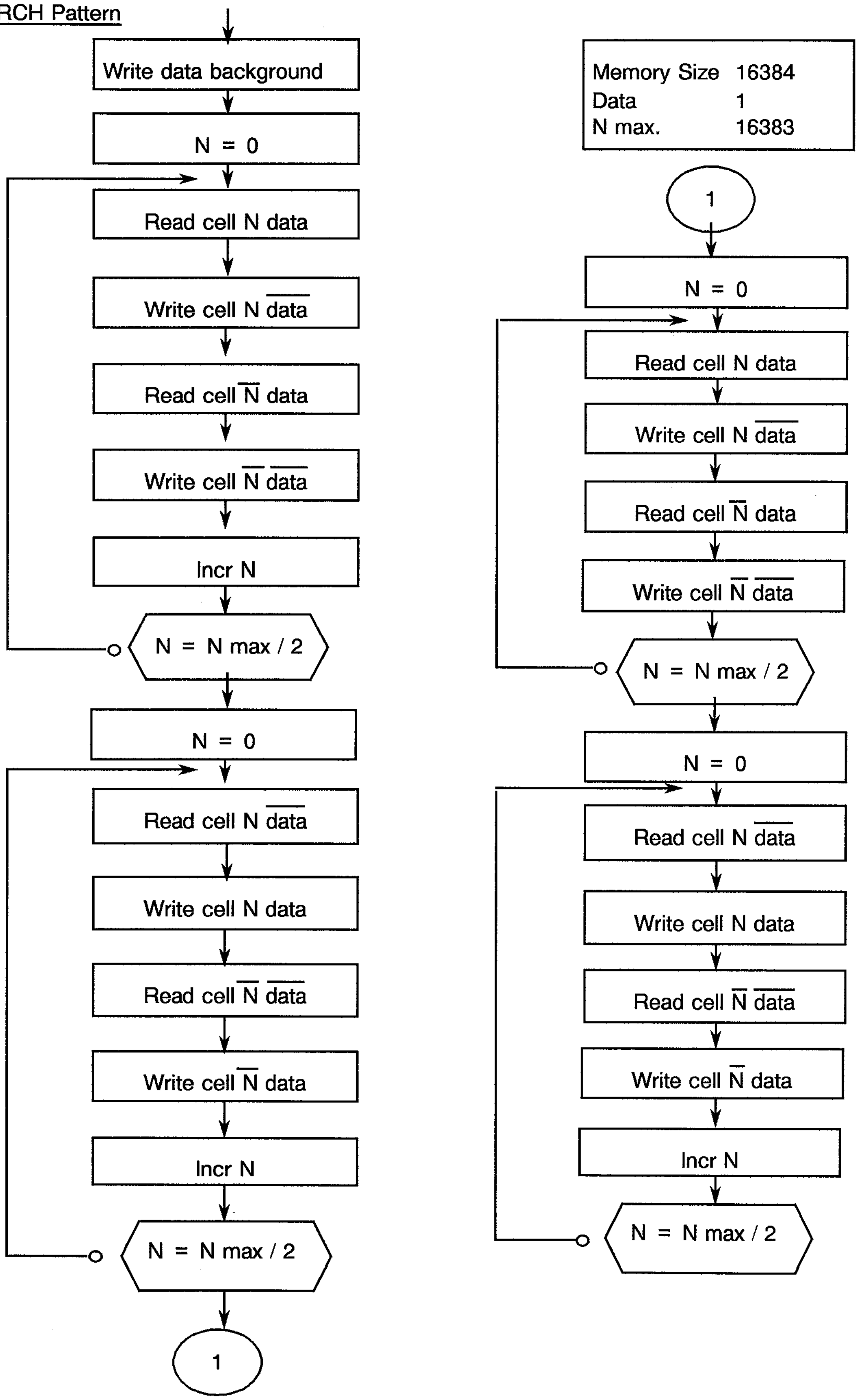
(a) Write 0 background $\overline{CS}$ at VIL.
(b) Write 1 background $\overline{CS}$ at VIL.
(c) Read 1 background $\overline{CS}$ at VIL.
(d) Write 0 background $\overline{CS}$ at VIH.
(e) Read 1 background $\overline{CS}$ at VIL.

LONG CHIP SELECT Pattern

Checkerboard pattern with timing unspecified.

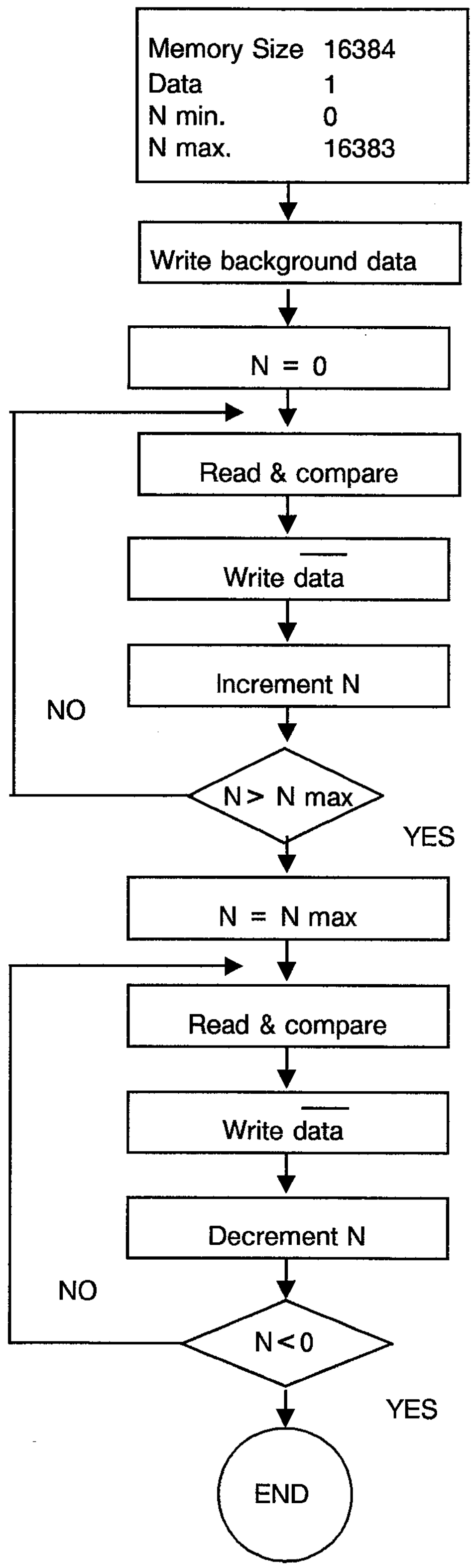
APPENDIX 'A'

COMARCH Pattern



APPENDIX 'A'

MARCH Pattern



APPENDIX 'A'

CHECKERBOARD Pattern