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# INTEGRATED CIRCUITS, SILICON MONOLITHIC, BIPOLAR OCTAL D-TYPE, 3-STATE POSITIVE EDGE-TRIGGERED FLIP-FLOPS, BASED ON TYPE 54S374

## ESA/SCC Detail Specification No. 9203/041

space components
coordination group

| Issue/Rev. | Date | Approved by | |
|---|---|---|---|
| | | SCCG Chairman | ESA Director General or his Deputy |
| Issue 2 | April 1994 | | |
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## DOCUMENTATION CHANGE NOTICE

| Rev. Letter | Rev. Date | Reference | CHANGE Item | Approved DCR No. |
|---|---|---|---|---|
| | | This Issue supersedes Issue 1 and incorporates all modifications defined in Revisions 'A', 'B' and 'C' to Issue 1 and the following DCR's:- | | |
| | | Cover page | | None |
| | | DCN | | None |
| | | Table 1(a) | : Lead Material and/or Finish amended for existing Variants | 22881 |
| | | | : Variant 02 added and existing figure reference amended | 22920 |
| | | | : Variants 11 and 12 added | 22881 |
| | | Table 1(b) | : No. 2, in Remarks, Note No. amended to "1" | 23573 |
| | | | : No. 3, in Remarks, Note No. amended to "2" | 23573 |
| | | | : No. 6, existing temperature specified for DIL/FP and Note No. amended to "3" | 23573 |
| | | | , new temperature and Note reference added for CCP | 23573 |
| | | | : Note 1 renumbered as "2" | 23573 |
| | | | : Note 2 renumbered as "3" and text amended | 23573 |
| | | | : Note 3 renumbered as "1" | 23573 |
| | | | : New Note 4 added | 23573 |
| | | Figure 2(a) | : New figure added | 22920 |
| | | Figure 2(b) | : Drawing and Table amended | 23592 |
| | | Figure 2(c) | : New figure added | 22881 |
| | | Notes to Figures | : Title of the notes amended | 22881 |
| | | | : Existing Notes deleted, new Notes added | 22881 |
| | | | : Note 2, "Not applicable" deleted, new Note added | 22920 |
| | | Figure 3(a) | : Figure for chip carrier package added | 22881 |
| | | | : Subtitles added above both drawings | 22881 |
| | | Figure 3(b) | : Note added | 23644 |
| | | Para. 4.2.2 | : PIND deviation deleted, "None" added | 21048 |
| | | Para. 4.2.4 | : Deviation deleted, "None" added | 22919 |
| | | Para. 4.2.5 | : Deviation deleted, "None" added | 22919 |
| | | Para. 4.3.2 | : Paragraph rewritten | 22920/ 23460 |
| | | | : Maximum weight limits amended | 221047 |
| | | Para. 4.4.2 | : Paragraph rewritten | 22881/ 22920 |
| | | Para. 4.5.2 | : Paragraph rewritten | 22881/ 22920 |
| | | Para. 4.5.3 | : Paragraph standardised | 23644 |
| | | Para. 4.7.1 | : "$T_{amb}$" added before "... +22 ± 3°C" | 23644 |
| | | Paras. 4.7.2 & 4.7.3 | : In title and paragraph, "burn-in" amended to read "power burn-in" | 23644 |
| | | Tables 2 and 3 | : Nos. 12 to 21, in Conditions, "See Note 2" deleted | 23650 |
| | | Table 2 | : Note 1 corrected | 23650 |
| | | Figure 4(i) | : In right-hand waveforms, measurement references corrected | 23650 |
| | | | : In Note 1, "$t_p = 0.5$" added | 23573 |
| | | Para. 4.8 | : Title amended | 23644 |
| | | Para. 4.8.2 | : Second sentence added | 23650 |
| | | Para. 4.8.5 | : Text completed | 23650 |
| | | Table 6 | : Nos. 12 to 21, Characteristics corrected | 23650 |

## TABLE OF CONTENTS

## 1. GENERAL

### 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, bipolar, Schottky Octal D-Type, 3-State, Positive Edge-Triggered Flip-Flop, based on Type 54S374. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

### 1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

### 1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

### 1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

### 1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

### 1.6 PIN ASSIGNMENT

As per Figure 3(a).

### 1.7 TRUTH TABLE

As per Figure 3(b).

### 1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

### 1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

## TABLE 1(a) - TYPE VARIANTS

| VARIANT | CASE | FIGURE | LEAD MATERIAL AND/OR FINISH |
|---|---|---|---|
| 02 | FLAT | 2(a) | G4 |
| 05 | DIL | 2(b) | D7 |
| 06 | DIL | 2(b) | G4 |
| 11 | CCP | 2(c) | 7 |
| 12 | CCP | 2(c) | 4 |

## TABLE 1(b) - MAXIMUM RATINGS

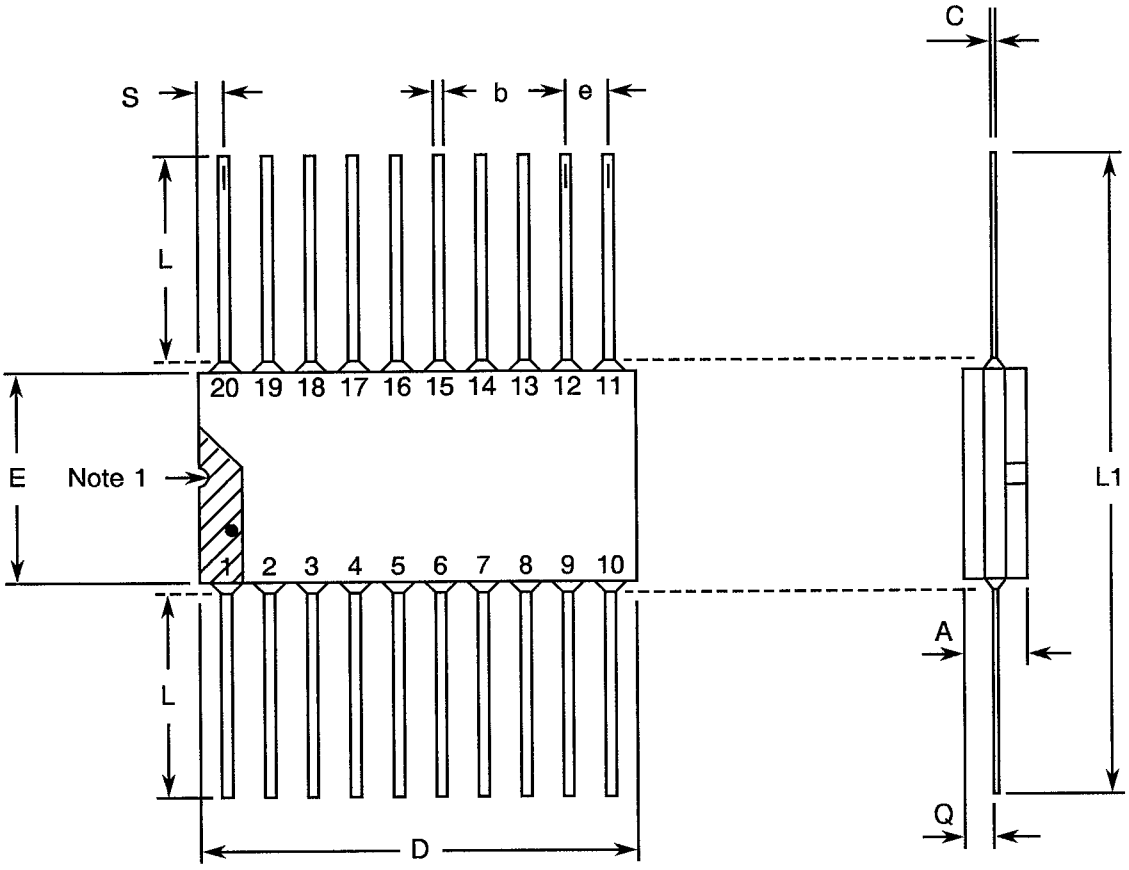
| No. | CHARACTERISTICS | SYMBOL | MAXIMUM RATINGS | UNIT | REMARKS |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $V_{CC}$ | −0.5 to 7.0 | V | - |
| 2 | Input Voltage | $V_{IN}$ | −0.5 to 5.5 | V | Note 1 |
| 3 | Device Dissipation | $P_D$ | 770 | mWdc | Note 2 |
| 4 | Operating Temperature Range | $T_{op}$ | −55 to +125 | °C | - |
| 5 | Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C | - |
| 6 | Soldering Temperature<br>For FP and DIP<br>For CCP | $T_{sol}$ | <br>+265<br>+245 | °C | <br>Note 3<br>Note 4 |

**NOTES**

1. Input current limited to −18mA.
2. Must withstand added $P_D$ due to short circuit conditions (i.e. $I_{OS}$) at one output for 5 seconds.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

## FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE

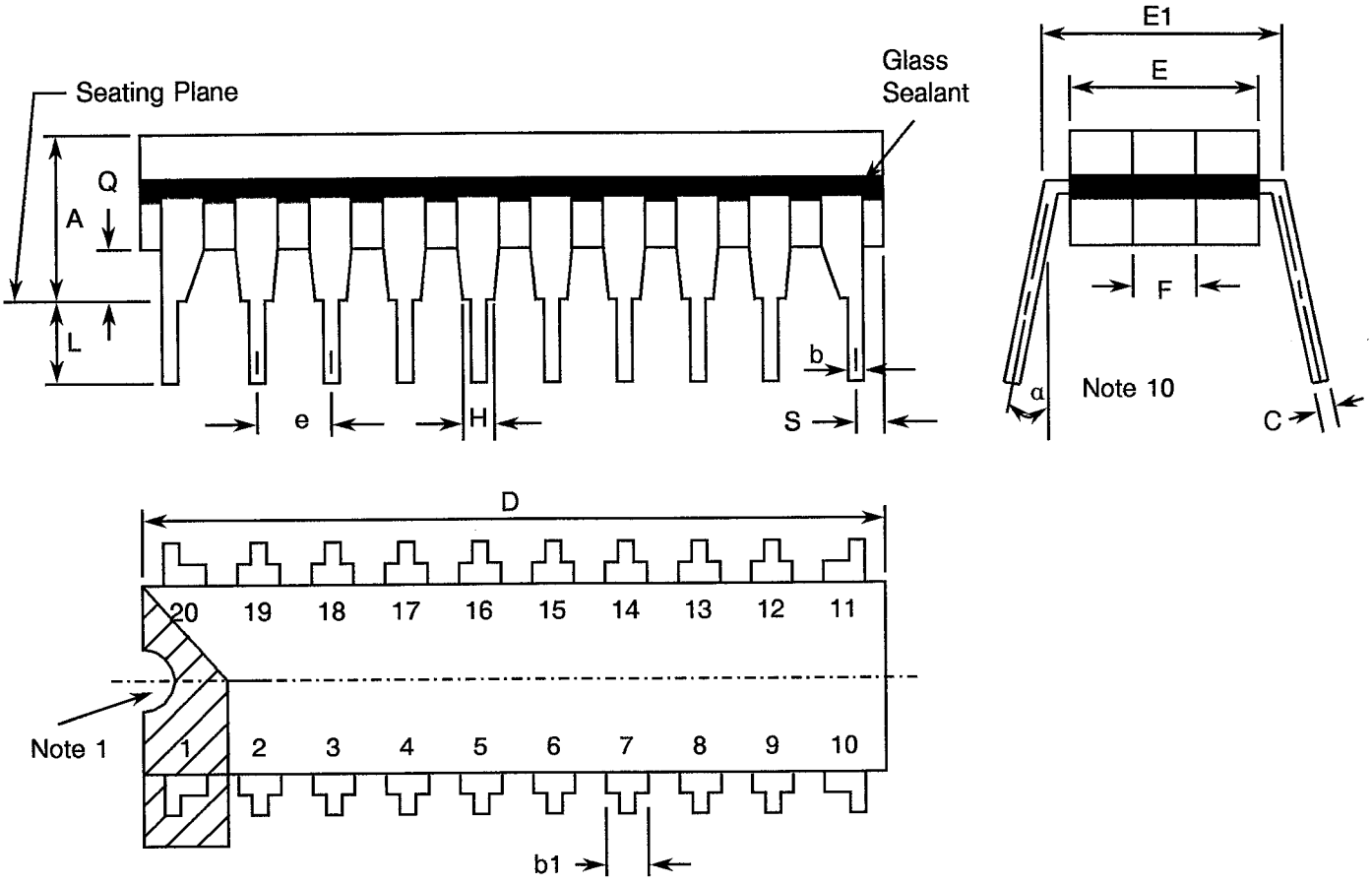



| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A | 1.14 | 2.34 | |
| b | 0.38 | 0.56 | 8 |
| C | 0.08 | 0.23 | 8 |
| D | - | 12.95 | 4 |
| E | 6.60 | 7.65 | |
| E1 | 8.15 | TYPICAL | 4 |
| e | 1.27 | TYPICAL | 5, 9 |
| L | 6.35 | 9.40 | 8 |
| L1 | 18.90 | 25.90 | |
| Q | 0.25 | 1.02 | 2 |
| S | 0.13 | 1.14 | 7 |

**NOTES:** See Page 10.

## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - DUAL-IN-LINE PACKAGE

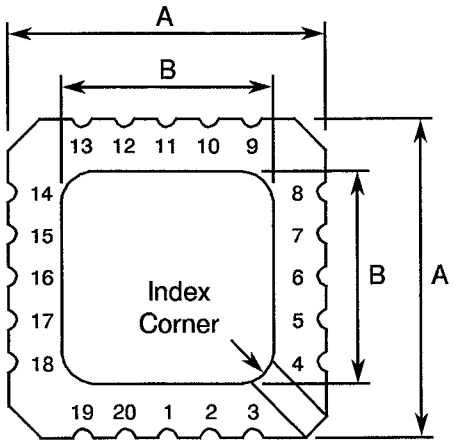



| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A | - | 5.08 | |
| b | 0.38 | 0.66 | 8 |
| b1 | - | 1.78 | 8 |
| C | 0.20 | 0.44 | 8 |
| D | 23.62 | 24.76 | 4 |
| E | 6.22 | 7.62 | 4 |
| E1 | 7.37 | 8.13 | |
| e | 2.54 TYPICAL | | 6, 9 |
| F | 1.27 TYPICAL | | |
| H | 0.76 | - | |
| L | 3.30 | 5.08 | 8 |
| Q | 0.51 | - | 3 |
| S | 0.38 | 1.27 | 7 |
| α | 0° | 15° | 10 |

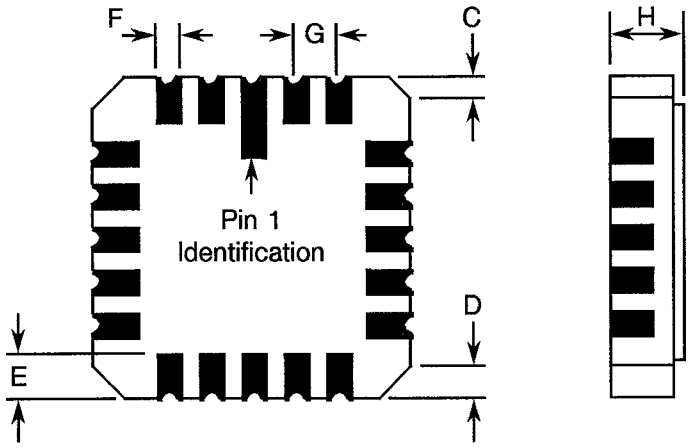
**NOTES:** See Page 10.

## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE)




20 Terminal




| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN. | MAX. | |
| A | 8.687 | 9.093 | - |
| B | 7.798 | 9.093 | - |
| C | 0.250 | 0.510 | 11 |
| D | 0.889 | 1.143 | 12 |
| E | 1.140 | 1.400 | 8 |
| F | 0.559 | 0.712 | 8 |
| G | 1.27 TYPICAL | | 5, 9 |
| H | 1.630 | 2.540 | - |

**NOTES:** See Page 10.

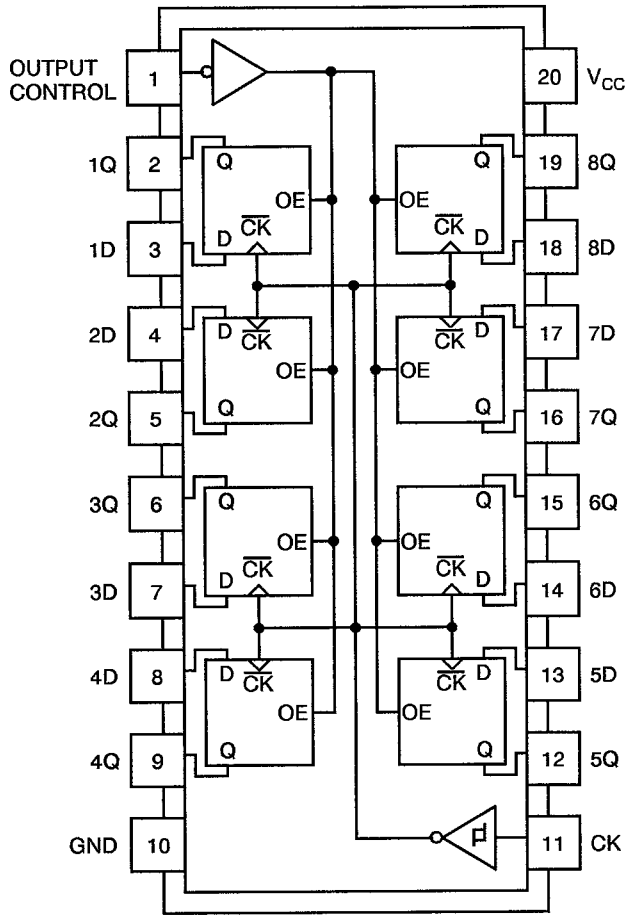
## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

NOTES TO FIGURES 2(a) TO 2(c)

1. Index area: a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages, the index shall be as shown in Figure 2(c).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ±0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 18 spaces for flat and dual-in-line packages.
   16 spaces for chip carrier packages.
10. Lead centre when $\alpha$ is 0°.
11. Index corner only - 2 dimensions.
12. 3 non-index corners - 6 dimensions.

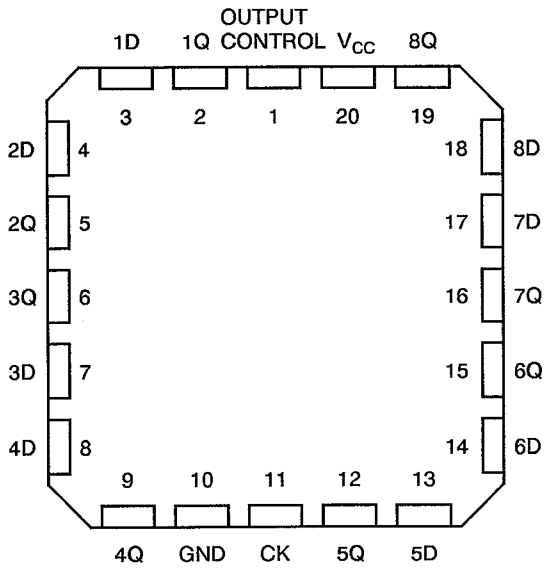
## FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE




(TOP VIEW)

CHIP CARRIER PACKAGE




(TOP VIEW)

## FIGURE 3(b) - TRUTH TABLE (EACH FLIP-FLOP)

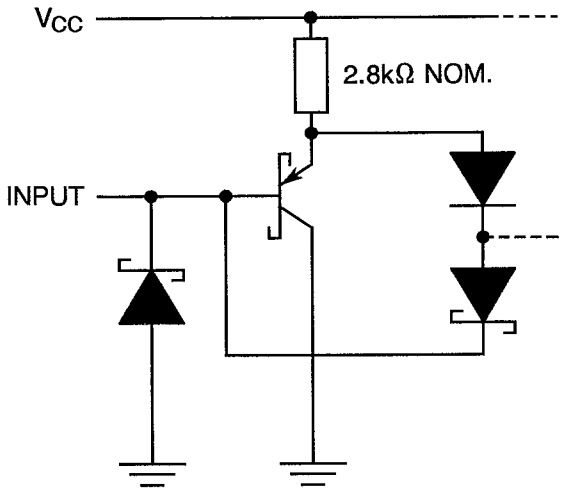
| INPUTS | | | OUTPUT |
|---|---|---|---|
| OUTPUT CONTROL | CLOCK | D | Y |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q0 |
| H | X | X | Z |

**NOTES**

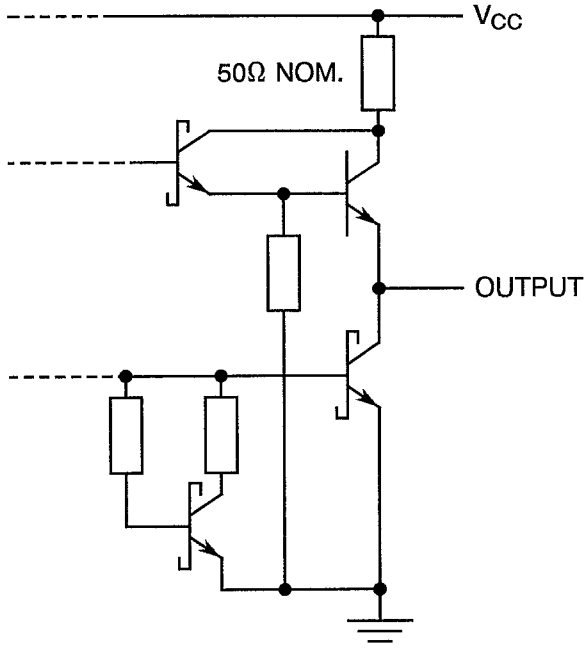
1. Logic Level Definitions: L = Low Level, H = High Level, Z = High Impedance, X = Don't Care.
2. ↑ = Transition from Low to High Level.

## FIGURE 3(c) - CIRCUIT SCHEMATIC

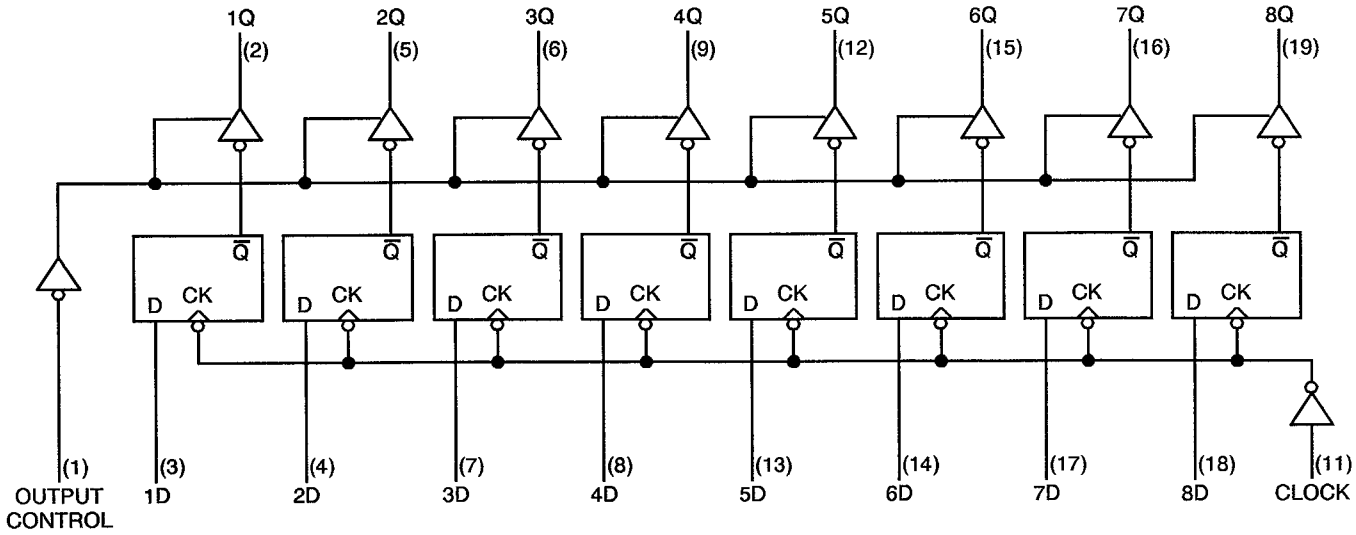
EQUIVALENT OF EACH INPUT




TYPICAL OF ALL OUTPUTS




## FIGURE 3(d) - FUNCTIONAL DIAGRAM



## 2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

## 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

$V_{IC}$ = Input Clamp Voltage.
$V_{CC}$ = Supply Voltage.
$I_{OZH}$ = Off-State Output Current High.
$I_{OZL}$ = Off-State Output Current Low.

## 4. REQUIREMENTS

### 4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

### 4.2 DEVIATIONS FROM GENERIC SPECIFICATION

#### 4.2.1 Deviations from Special In-process Controls

None.

#### 4.2.2 Deviations from Final Production Tests (Chart II)

None.

#### 4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

(b) Para. 9.9.2, "Electrical Measurements at High and Low Temperatures": Only a test result summary, based on go-no-go tests and presented in histogram form is required.

#### 4.2.4 Deviations from Qualification Tests (Chart IV)

None.

#### 4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 0.9 grammes for the flat package, 3.2 grammes for the dual-in-line package and 0.6 grammes for the chip carrier package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be either Type 'D' or Type 'G' with either Type '4' or Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages, the finish shall be either Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

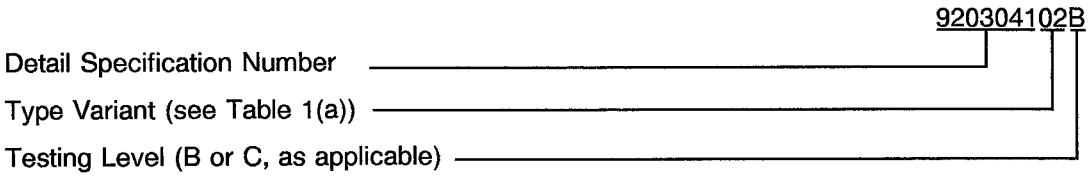
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2(c).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:




4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125$ and $-55$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values ($\Delta$) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5 of this specification.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - D.C. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 1 | Functional Test | - | - | 3(b) | Verify Truth Table with Load. Note 1 | - | - | - |
| 2 to 11 | Input Current High Level 1 | $I_{IH1}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 1-3-4-7-8-11-13-14-17-18) | - | 50 | µA |
| 12 to 21 | Input Current High Level 2 (Max. Input Voltage) | $I_{IH2}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 5.5V (Pins 1-3-4-7-8-11-13-14-17-18) | - | 1.0 | mA |
| 22 to 31 | Input Clamp Voltage | $V_{IC}$ | 3008 | 4(b) | $V_{CC}$ = 4.5V, $I_{IN}$ = −18mA Note 2 (Pins 1-3-4-7-8-11-13-14-17-18) | - | −1.2 | V |
| 32 to 41 | Input Current Low Level | $I_{IL}$ | 3009 | 4(c) | $V_{CC}$ = 5.5V, $V_{IL}$ = 0.5V (Pins 1-3-4-7-8-11-13-14-17-18) | - | −250 | µA |
| 42 to 49 | Output Voltage Low Level | $V_{OL}$ | 3007 | 4(d) | $V_{CC}$ = 4.5V, $V_{IL}$ = 0.8V $V_{IH}$ = 2.0V, $I_{OL}$ = 20mA (Pins 2-5-6-9-12-15-16-19) | - | 0.5 | V |
| 50 to 57 | Output Voltage High Level | $V_{OH}$ | 3006 | 4(e) | $V_{CC}$ = 4.5V, $V_{IL}$ = 0.8V $V_{IH}$ = 2.0V, $I_{OH}$ = −2.0mA (Pins 2-5-6-9-12-15-16-19) | 2.4 | - | V |
| 58 to 65 | Off-State Output Current, High Level Applied | $I_{OZH}$ | - | 4(h) | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.0V $V_{OUT}$ = 2.4V (Pins 2-5-6-9-12-15-16-19) | - | 50 | µA |
| 66 to 73 | Off-State Output Current, Low Level Applied | $I_{OZL}$ | - | 4(h) | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.0V $V_{OUT}$ = 0.5V (Pins 2-5-6-9-12-15-16-19) | - | −50 | µA |
| 74 to 81 | Short Circuit Output Current | $I_{OS}$ | 3011 | 4(f) | $V_{CC}$ = 5.5V Note 3 (Pins 2-5-6-9-12-15-16-19) | −40 | −100 | mA |
| 82 | Supply Current | $I_{CC}$ | 3005 | 4(g) | $V_{CC}$ = 5.5V (Pin 20) | - | 140 | mA |

**NOTES:** See Page 17.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - A.C. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) (NOTE 4) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 83 to 90 | Propagation Delay, Low to High Level, Clock to any Q | $t_{PLH}$ | - | 4(i) | $V_{CC}$ = 5.0V<br>$R_L$ = 280Ω<br>$C_L$ = 15pF<br>(Pins 2-5-6-9-12-15-16-19) | - | 15 | ns |
| 91 to 98 | Propagation Delay, High to Low Level, Clock to any Q | $t_{PHL}$ | - | 4(i) | $V_{CC}$ = 5.0V<br>$R_L$ = 280Ω<br>$C_L$ = 15pF<br>(Pins 2-5-6-9-12-15-16-19) | - | 17 | ns |
| 99 to 106 | Output Enable Time to High Level from Output Control to any Q | $t_{PZH}$ | - | 4(i) | $V_{CC}$ = 5.0V<br>$R_L$ = 280Ω<br>$C_L$ = 15pF<br>(Pins 2-5-6-9-12-15-16-19) | - | 15 | ns |
| 107 to 114 | Output Enable Time to Low Level from Output Control to any Q | $t_{PZL}$ | - | 4(i) | $V_{CC}$ = 5.0V<br>$R_L$ = 280Ω<br>$C_L$ = 15pF<br>(Pins 2-5-6-9-12-15-16-19) | - | 18 | ns |
| 115 to 122 | Output Disable Time to High Level from Output Control to any Q | $t_{PHZ}$ | - | 4(i) | $V_{CC}$ = 5.0V<br>$R_L$ = 280Ω<br>$C_L$ = 5.0pF<br>(Pins 2-5-6-9-12-15-16-19) | - | 9.0 | ns |
| 123 to 130 | Output Disable Time to Low Level from Output Control to any Q | $t_{PLZ}$ | - | 4(i) | $V_{CC}$ = 5.0V<br>$R_L$ = 280Ω<br>$C_L$ = 5.0pF<br>(Pins 2-5-6-9-12-15-16-19) | - | 12 | ns |

**NOTES**

1. Go-no-go test with $V_{IL}$ = 0.3V, $V_{IH}$ = 3.0V, $V_{CC}$ = 5.0V; trip point 1.5V.
2. All inputs and outputs not under test shall be open.
3. No more than 1 output should be shorted at a time, and only for 1 second maximum.
4. Propagation delay measurements shall be performed as a go-no-go test on a 100% basis. Read-and-record measurements shall be performed on an LTPD7 sample basis following the Chart III Burn-in Test.

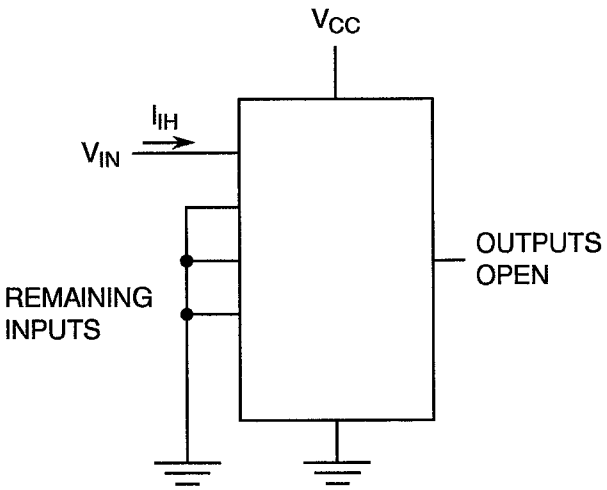
**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0−5) °C AND −55(+5−0) °C**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 1 | Functional Test | - | - | 3(b) | Verify Truth Table with Load. Note 1 | - | - | - |
| 2 to 11 | Input Current High Level 1 | $I_{IH1}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 2.7V (Pins 1-3-4-7-8-11-13-14-17-18) | - | 50 | µA |
| 12 to 21 | Input Current High Level 2 (Max. Input Voltage) | $I_{IH2}$ | 3010 | 4(a) | $V_{CC}$ = 5.5V, $V_{IN}$ = 5.5V (Pins 1-3-4-7-8-11-13-14-17-18) | - | 1.0 | mA |
| 22 to 31 | Input Clamp Voltage | $V_{IC}$ | 3008 | 4(b) | $V_{CC}$ = 4.5V, $I_{IN}$ = −18mA Note 2 (Pins 1-3-4-7-8-11-13-14-17-18) | - | −1.2 | V |
| 32 to 41 | Input Current Low Level | $I_{IL}$ | 3009 | 4(c) | $V_{CC}$ = 5.5V, $V_{IL}$ = 0.5V (Pins 1-3-4-7-8-11-13-14-17-18) | - | −250 | µA |
| 42 to 49 | Output Voltage Low Level | $V_{OL}$ | 3007 | 4(d) | $V_{CC}$ = 4.5V, $V_{IL}$ = 0.8V $V_{IH}$ = 2.0V, $I_{OL}$ = 20mA (Pins 2-5-6-9-12-15-16-19) | - | 0.5 | V |
| 50 to 57 | Output Voltage High Level | $V_{OH}$ | 3006 | 4(e) | $V_{CC}$ = 4.5V, $V_{IL}$ = 0.8V $V_{IH}$ = 2.0V, $I_{OH}$ = −2.0mA (Pins 2-5-6-9-12-15-16-19) | 2.4 | - | V |
| 58 to 65 | Off-State Output Current, High Level Applied | $I_{OZH}$ | - | 4(h) | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.0V $V_{OUT}$ = 2.4V (Pins 2-5-6-9-12-15-16-19) | - | 50 | µA |
| 66 to 73 | Off-State Output Current, Low Level Applied | $I_{OZL}$ | - | 4(h) | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.0V $V_{OUT}$ = 0.5V (Pins 2-5-6-9-12-15-16-19) | - | −50 | µA |
| 74 to 81 | Short Circuit Output Current | $I_{OS}$ | 3011 | 4(f) | $V_{CC}$ = 5.5V Note 3 (Pins 2-5-6-9-12-15-16-19) | −40 | −100 | mA |
| 82 | Supply Current | $I_{CC}$ | 3005 | 4(g) | $V_{CC}$ = 5.5V (Pin 20) | - | 140 | mA |

**NOTES:** See Page 17.

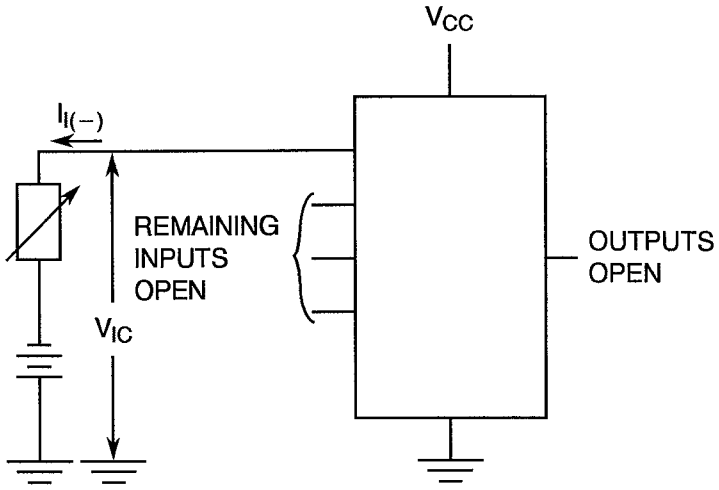
## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

### FIGURE 4(a) - HIGH LEVEL INPUT CURRENT



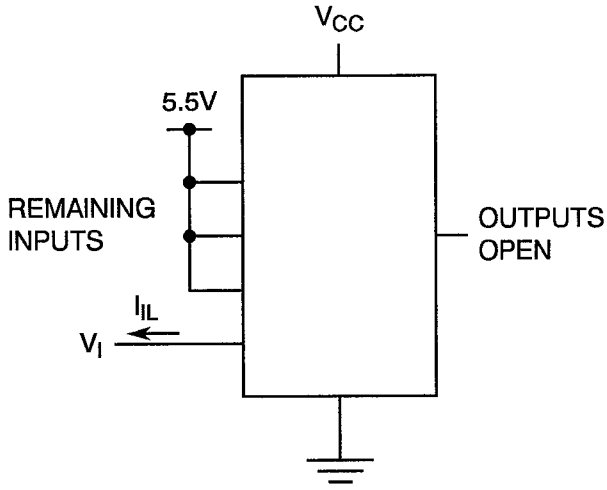

**NOTES**
1. Each input to be tested separately.

### FIGURE 4(b) - INPUT CLAMP VOLTAGE



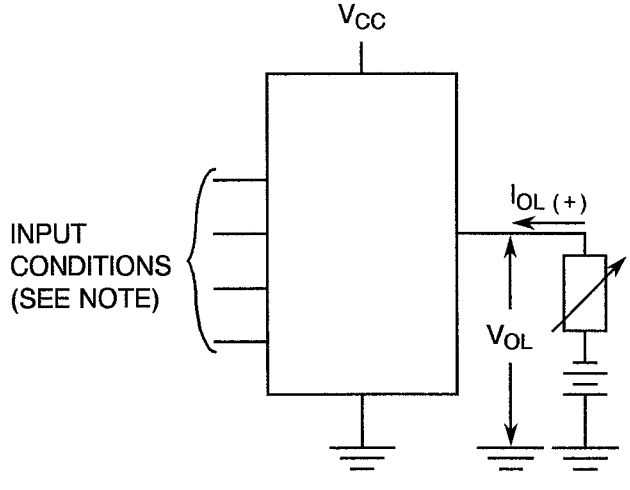

**NOTES**
1. Each input to be tested separately.

### FIGURE 4(c) - LOW LEVEL INPUT CURRENT




**NOTES**
1. Each input to be tested separately.

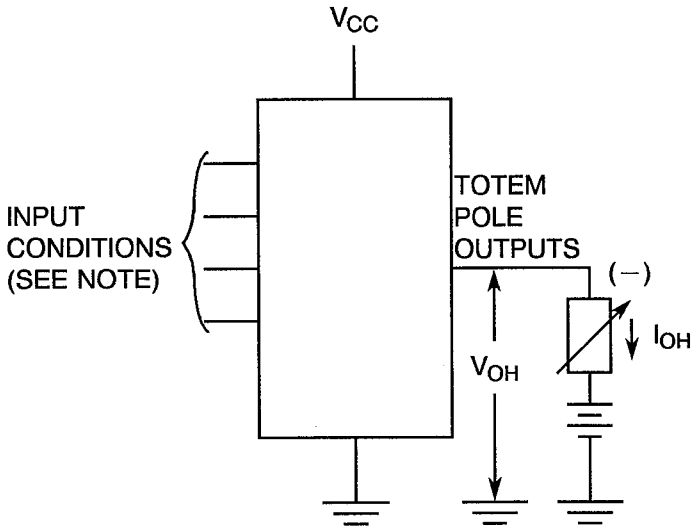
### FIGURE 4(d) - LOW LEVEL OUTPUT VOLTAGE




**NOTES**
1. Output Control and D inputs at $V_{IL}$.
   Clock input at transition from low to high.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

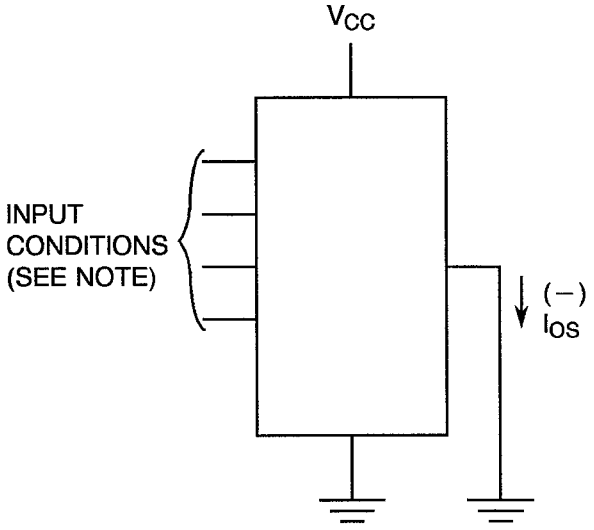
FIGURE 4(e) - HIGH LEVEL OUTPUT VOLTAGE




**NOTES**

1. Output Control at $V_{IL}$, D input at $V_{IH}$.
   Clock input at transition from low to high.

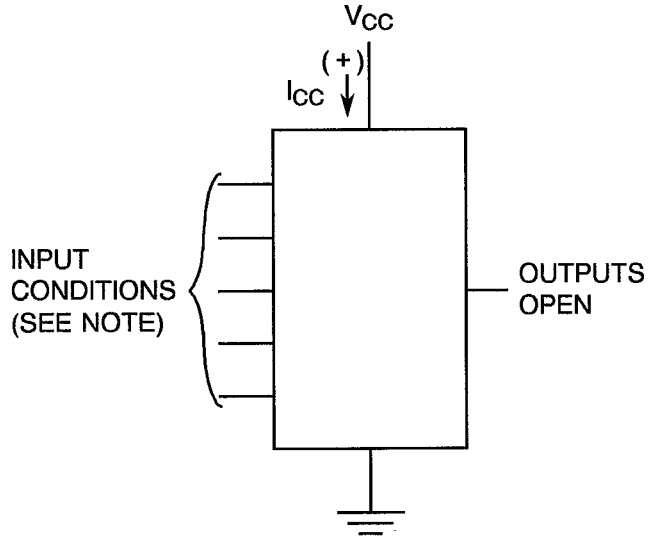
FIGURE 4(f) - SHORT CIRCUIT OUTPUT CURRENT




**NOTES**

1. Output Control at $V_{IL}$, D input at $V_{IH}$.
   Clock input at transition from low to high.
2. No more than one output to be shorted at a time.

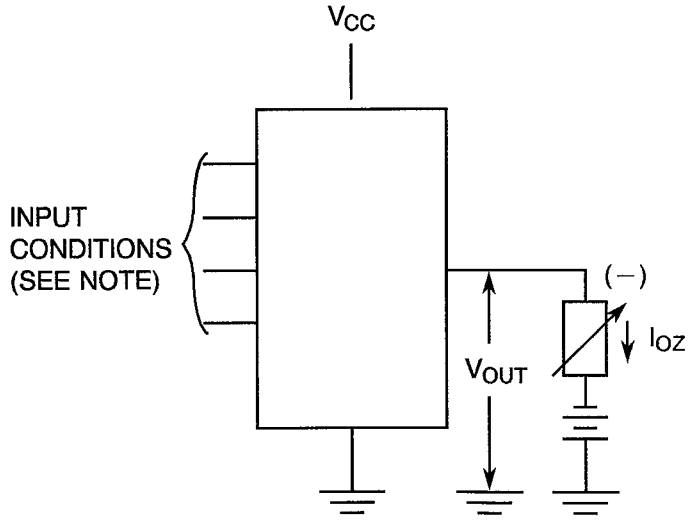
FIGURE 4(g) - SUPPLY CURRENT




**NOTES**

1. Output Control at $V_{IH} = 4.5V$, all other inputs at $V_{IL} = 0V$.

FIGURE 4(h) - OFF-STATE OUTPUT CURRENT

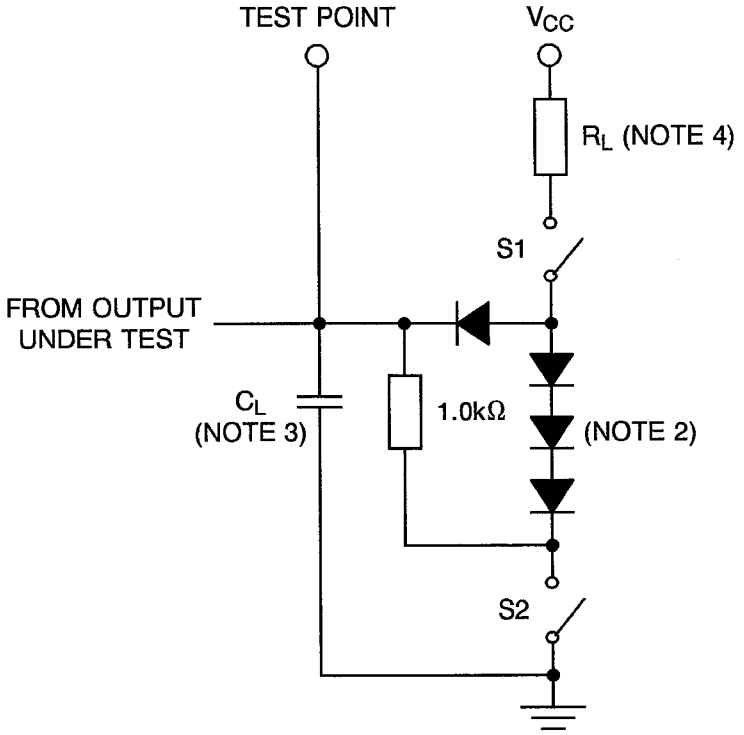



**NOTES**

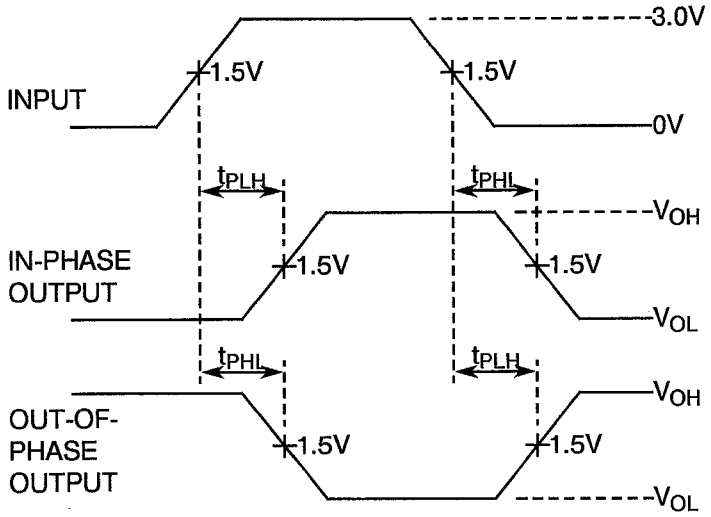
1. Output Control and D inputs at $V_{IH}$.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - DYNAMIC TEST AND SWITCHING WAVEFORMS




VOLTAGE WAVEFORMS

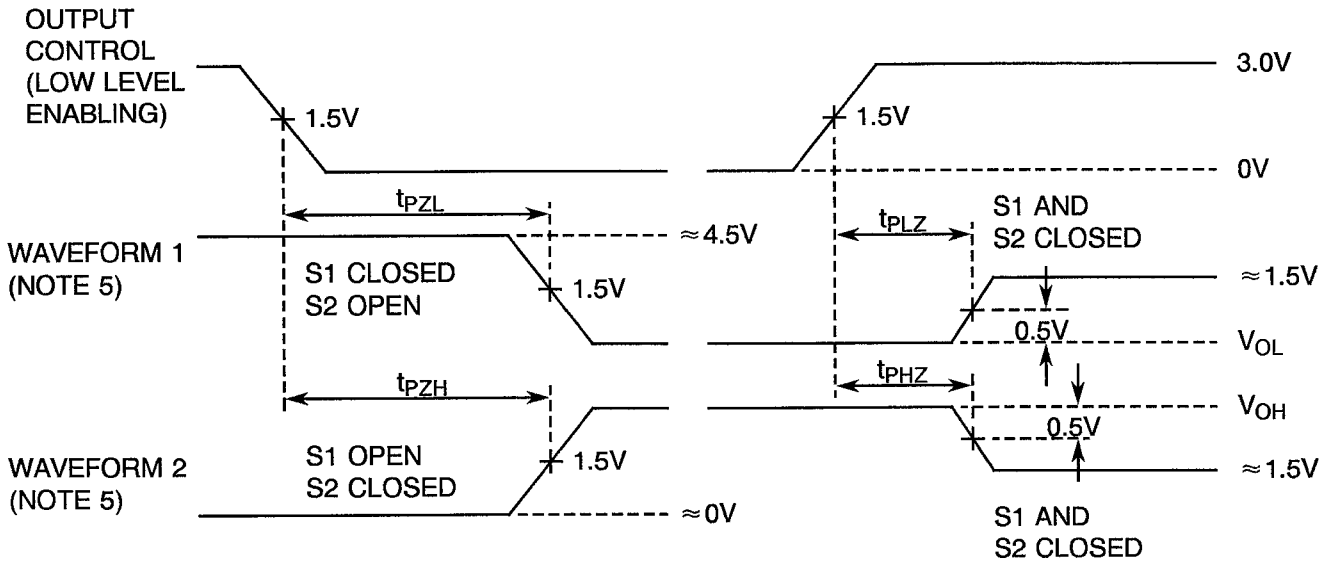



**NOTES:** See Page 22.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - DYNAMIC TEST AND SWITCHING WAVEFORMS (CONTINUED)

VOLTAGE WAVEFORMS (CONTINUED)




**NOTES**

1. All inputs are supplied by generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, $t_p = 0.5\mu$s, PRR $\leq$ 1.0MHz, $Z_{OUT} = 50\Omega$.
2. All diodes are 1N916 or 1N3064.
3. $C_L = 15$pF or 5.0pF $\pm$ 5% (see Table 2) including scope probe, wiring and stray capacitance without package in test fixture.
4. $R_L = 280\Omega \pm 5\%$.
5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
6. When measuring propagation delay time of 3-State Outputs, S1 and S2 are closed.

## TABLE 4 - PARAMETER DRIFT VALUES

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS (Δ) | UNIT |
|---|---|---|---|---|---|---|
| 2 to 11 | Input Current High Level 1 | $I_{IH1}$ | As per Table 2 | As per Table 2 | ±20 or (1) ±10 | % µA |
| 32 to 41 | Input Current Low Level | $I_{IL}$ | As per Table 2 | As per Table 2 | ±200 | µA |
| 42 to 49 | Output Voltage Low Level | $V_{OL}$ | As per Table 2 | As per Table 2 | ±60 | mV |
| 50 to 57 | Output Voltage High Level | $V_{OH}$ | As per Table 2 | As per Table 2 | ±240 | mV |

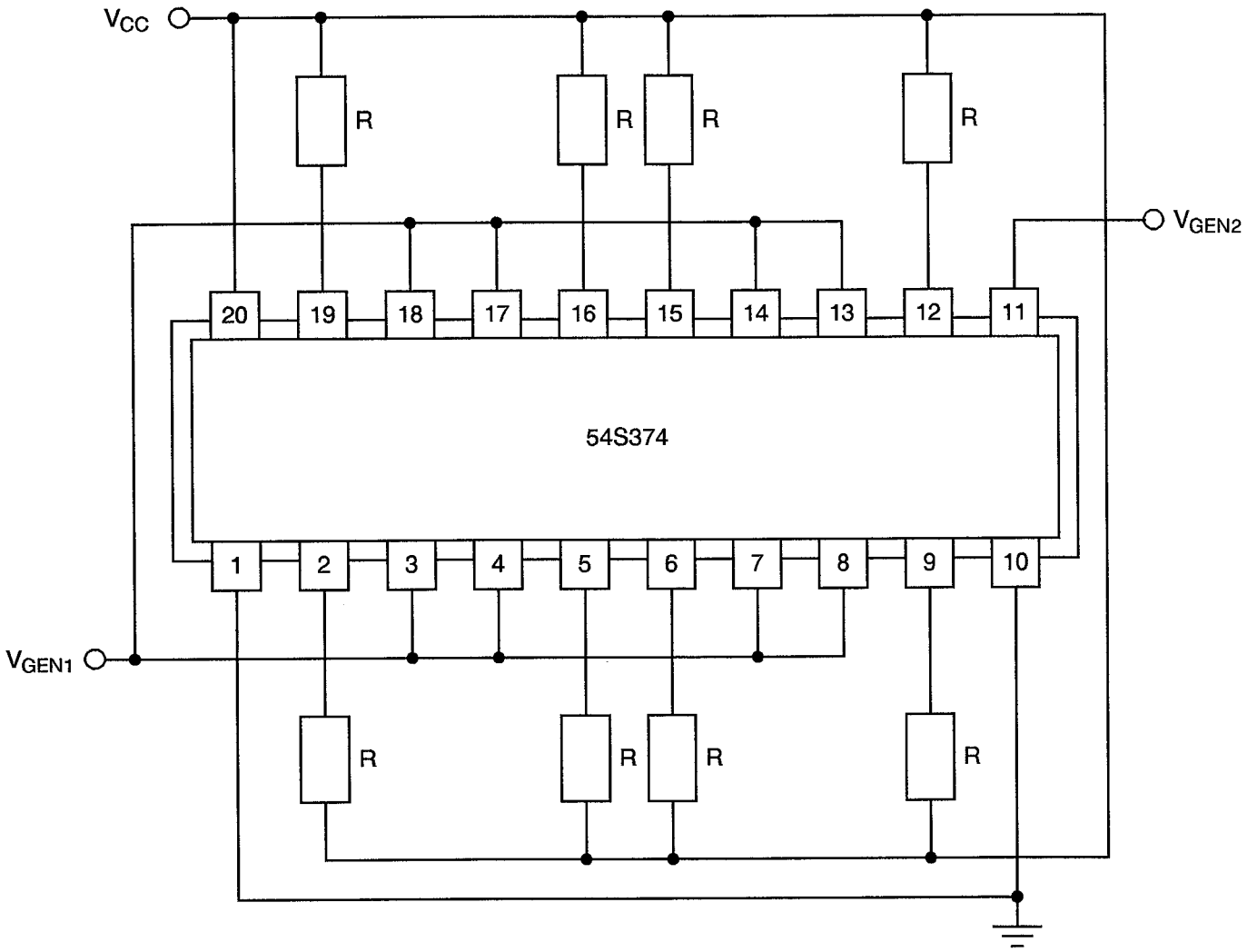
**NOTES**
1. Whichever is greater, referred to the initial value.

## TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST

| No. | CHARACTERISTICS | SYMBOL | CONDITION | UNIT |
|---|---|---|---|---|
| 1 | Ambient Temperature | $T_{amb}$ | +125(+0−5) | °C |
| 2 | Power Supply Voltage | $V_{CC}$ | 5(+0.5−0) | V |
| 3 | Pulse Voltage | $V_{GEN}$ | 0.5 max. to 3.0 min. | V |
| 4 | Frequency | $f_{GEN1}$ $f_{GEN2}$ | 50<br>100<br>(Note 1) | Hz |
| 5 | Fan-out | - | 10 | - |
| 6 | Rise Time | $t_r$ | 50 max. | µs |
| 7 | Fall Time | $t_f$ | 50 max. | µs |
| 8 | Duty Cycle | - | 20 min. | % |

**NOTES**
1. Tolerance ±10%.

**FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST**




**NOTES**

1. R = 250Ω.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO.▮9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$▮°C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0\text{-}5)$▮°C.

**TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS**

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | | (Δ) | ABSOLUTE | |
| 2 to 11 | Input Current High Level 1 | $I_{IH1}$ | As per Table 2 | As per Table 2 | ±10 | - | µA |
| 12 to 21 | Input Current High Level 2 (Max. Input Voltage) | $I_{IH2}$ | As per Table 2 | As per Table 2 | - | 1.0 | mA |
| 32 to 41 | Input Current Low Level | $I_{IL}$ | As per Table 2 | As per Table 2 | ±25 | - | µA |
| 42 to 49 | Output Voltage Low Level | $V_{OL}$ | As per Table 2 | As per Table 2 | ±60 | - | mV |
| 50 to 57 | Output Voltage High Level | $V_{OH}$ | As per Table 2 | As per Table 2 | ±240 | - | mV |
| 82 | Supply Current Outputs High | $I_{CCH}$ | As per Table 2 | As per Table 2 | ±20 | - | % |

**APPENDIX 'A'**



AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|---|---|
| Para. 4.2.1 | Scanning Electron Microscope (SEM) Inspection may be performed using TIF document TIF 3.61.610.001. |
| Para. 4.2.2 | Prior to Die Shear Test TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test, using TIF document TIF 50.42-3002. |
| Para. 4.2.3 | Radiographic Inspection may be performed using TIF document TIF 50.42-3002. |