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INTEGRATED CIRCUITS, SILICON MONOLITHIC,

CMOS, 16 CHANNEL MULTIPLEXER,

RADIATION HARDENED,

BASED ON TYPE HS-1840RH

ESA/SCC Detail Specification No. 9408/019

space components
coordination group

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		SCCG Chairman	ESA Director General or his Deputy
Issue 2	February 1999		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
		This Issue supersedes Issue 1 and incorporates all modifications defined in Revision 'A' to Issue 1 and the changes agreed in the following DCRs:-		
		Cover page		None
		DCN		None
		Table 1(a)	: Lead Finish column heading and entries amended	21025
		Para. 2	: Item "(c)" deleted	21025
			: New Item "(c)" added	None
		Para. 4.2.2	: Deviation deleted and "None" added	21048
		Para. 4.2.4	: Deviation deleted and "None" added	22919
		Para. 4.2.5	: Deviation deleted and "None" added	22919
		Para. 4.4.2	: Existing text deleted and new text added	21025
		Para. 4.5.3	: Type Variant entry amended	21025

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APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon, monolithic, radiation hardened, 16 channel multiplexer, constructed with the Linear Dielectric CMOS technology, based on Type HS-1840RH. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION

As per Figure 1.

1.5 PHYSICAL DIMENSIONS

As per Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, test, packaging, shipping and any handling. Devices may be damaged if the following conditions are exceeded:-

C = 100pF R = 1500Ω V = ±400V.

The following handling practices are recommended:-

(a) Devices should be handled on benches with conductive and grounded surfaces.

(b) Ground test equipment and tools.

(c) Do not handle devices by the terminations.

(d) Store devices in conductive foam or carriers.

(e) Avoid use of plastic, rubber or silk in the fabrication and assembly areas.

(f) Maintain relative humidity above 50%, if practical.

(g) Ground all handling personnel with a conductive bracelet through a 1.0MΩ resistor to ground.

(h) Ionised air blowers reduce charge build-up areas where grounding is not possible or desirable.

1.11 INPUT PROTECTION NETWORKS

Double diode protection shall be incorporated into each input as shown in Figure 3(e).

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

(c) MIL-M-38510, Microcircuits, General Specification for.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

I_{IH}	=	Input current, high level
I_{IL}	=	Input current, low level
$I_{S(OFF)}$	=	Leakage current into the source terminal of an "OFF" switch.
$I_{S(OFF)\pm}$	=	Leakage current into the source terminal with power "OFF".
$I_{D(OFF)}$	=	Leakage current into the drain terminal of an "OFF" switch.
$I_{D(ON)}$	=	Leakage current from an "OFF" driver into the switch (drain).
$I_{D(OVP)}$	=	Overvoltage protection, leakage current into the drain terminal of an "OFF" switch.
$I_{S(OVP)}$	=	Overvoltage protection, leakage current into the source terminal of an "OFF" switch.
$I_{+(PSC)}$	=	Positive supply current.
$I_{-(PSC)}$	=	Negative supply current.
$I_{+(STDBY)}$	=	Positive supply standby current.
$I_{-(STDBY)}$	=	Negative supply standby current.
R_{ON}	=	Switch "ON" resistance.
C_A	=	Address capacitance.
C_{OS}	=	Output switch capacitance.
C_{IS}	=	Input switch capacitance.
t_{PLH1}	=	Rise Time, Address inputs to I/O channels.
t_{PHL1}	=	Fall Time, Address inputs to I/O channels.
t_{PLH2}	=	Rise Time, Enable to I/O channels.
t_{PHL2}	=	Fall Time, Enable to I/O channels.

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND FINISH
01	D.I.L	2	D2 or G2
02	D.I.L	2	D3 or G3

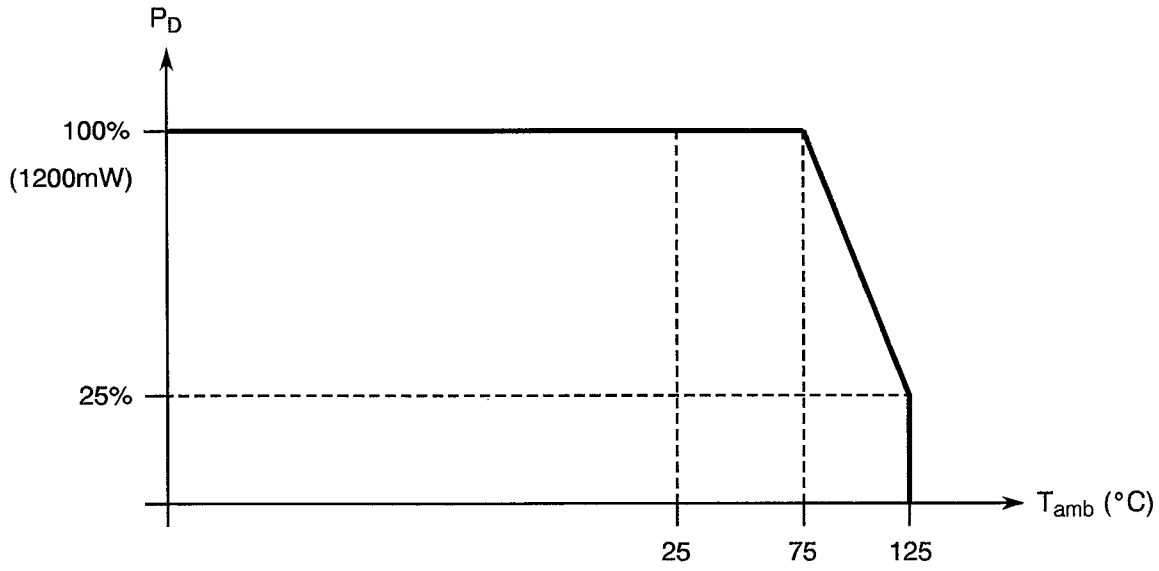
TABLE 1(b) - MAXIMUM RATINGS

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNITS	REMARKS
1	Supply Voltage	V_{CC}	+40	V	Between Pins 1 and 27
2	Reference	V_{REF}	+20	V	to Gnd
3	Digital Input Overvoltage	V_{EN}, V_A V_A	V_{REF} +4.0 Gnd −4.0	V	
4	Analog Input Overvoltage	V_S	+V supply +20 −V supply −20	V	
5	Device Dissipation	P_D	1200	mWdc	Per package. Note 1
6	Output Dissipation	P_{DSO}	100	mWdc	Note 2
7	Operating Temperature	T_{opr}	−55 to +125	°C	
8	Storage Temperature	T_{stg}	−65 to +150	°C	
9	Soldering Temperature	T_{sol}	+300	°C	Note 3
10	Junction Temperature	T_J	+175	°C	

NOTES

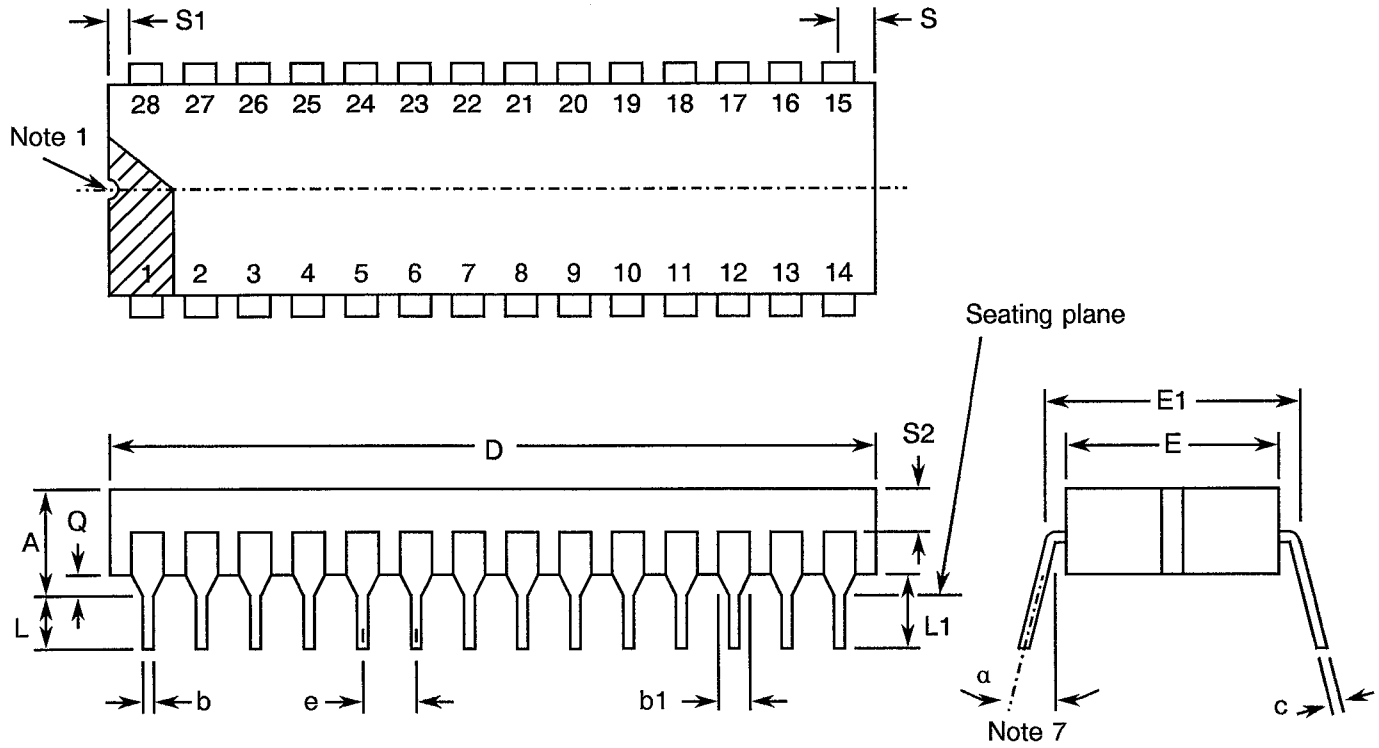
1. Derate 8mW/°C above T_{amb} = +25°C.
2. The maximum power dissipation.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.

FIGURE 1 - PARAMETER DERATING INFORMATION



Device Dissipation versus Temperature

FIGURE 2 - PHYSICAL DIMENSIONS

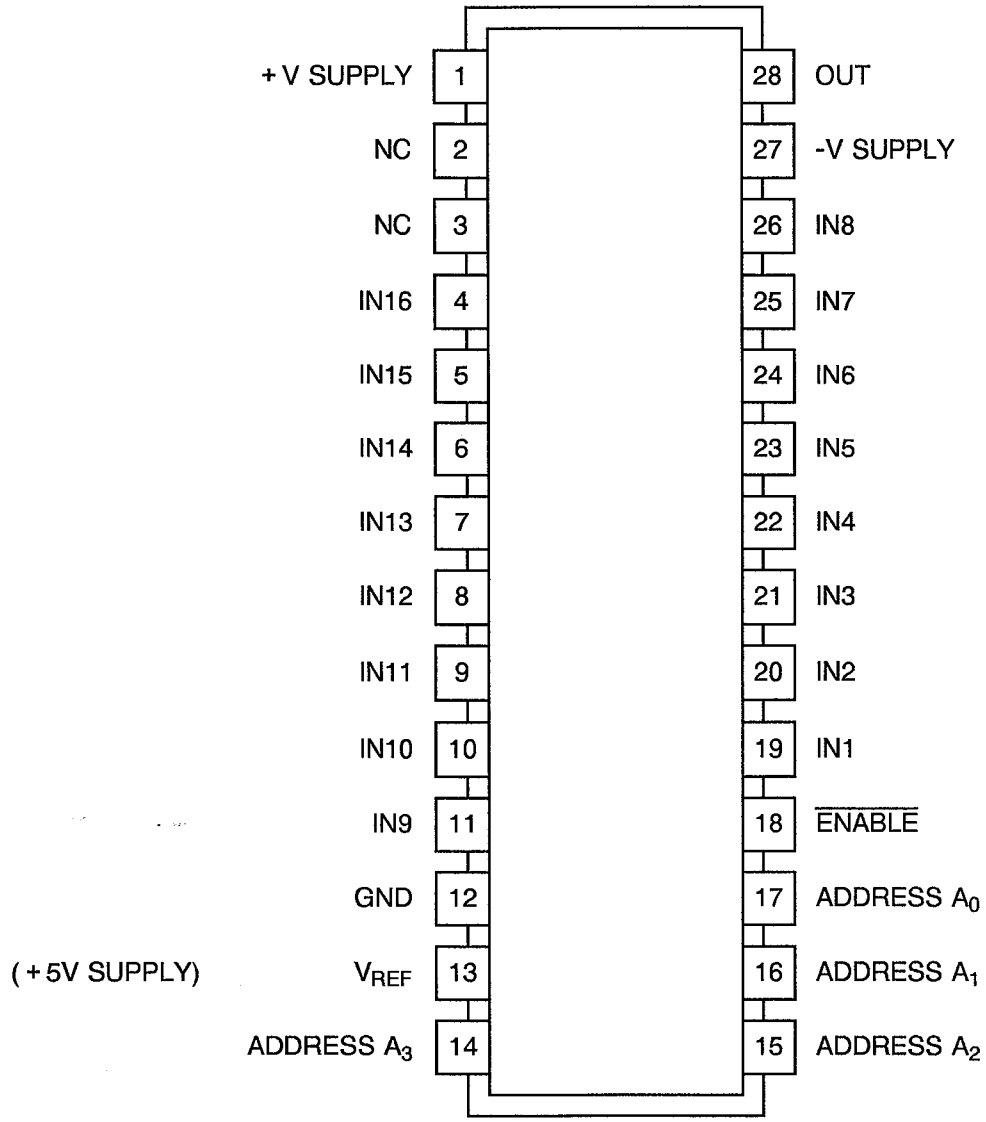


SYMBOL	MILLIMETRES		NOTES
	MIN.	MAX.	
A	-	5.08	
b	0.36	0.58	8
b1	1.02	1.78	2, 8
C	0.20	0.36	8
D	36.6	37.6	4
E	13.21	13.97	4
E1	14.99	15.75	7
E2	N/A	N/A	
E3	N/A	N/A	
e	2.54 BSC		5, 9
L	3.18	4.57	
L1	3.81	5.08	
Q	0.51	1.27	3
Q1	N/A	N/A	
S	-	2.49	6
S1	0.13	-	6
S2	N/A	N/A	
α	0°	15°	

NOTES

1. Index area; a notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be located within the shaded area shown. The Manufacturer's identification shall not be used as a pin 1 identification mark.
2. The minimum limit for dimension b1 may be 0.58mm for leads number 1, 14, 15 and 28 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lid, meniscus and glass overrun.
5. The basic pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ±0.25mm of its exact longitudinal position relative to pins 1 and 28.
6. Applies to all 4 corners (leads number 1, 14, 15 and 28), and 40.5 appendix C of MIL-M-38510 shall apply.
7. Lead centre when $\alpha = 0°$. E1 shall be measured at the centreline of the leads (see 40.4 appendix C of MIL-M-38510).
8. All leads - Increase maximum limit by 0.08mm measured at the centre of the flat, when lead finish A is applied.
9. 26 spaces.

FIGURE 3(a) - PIN ASSIGNMENT



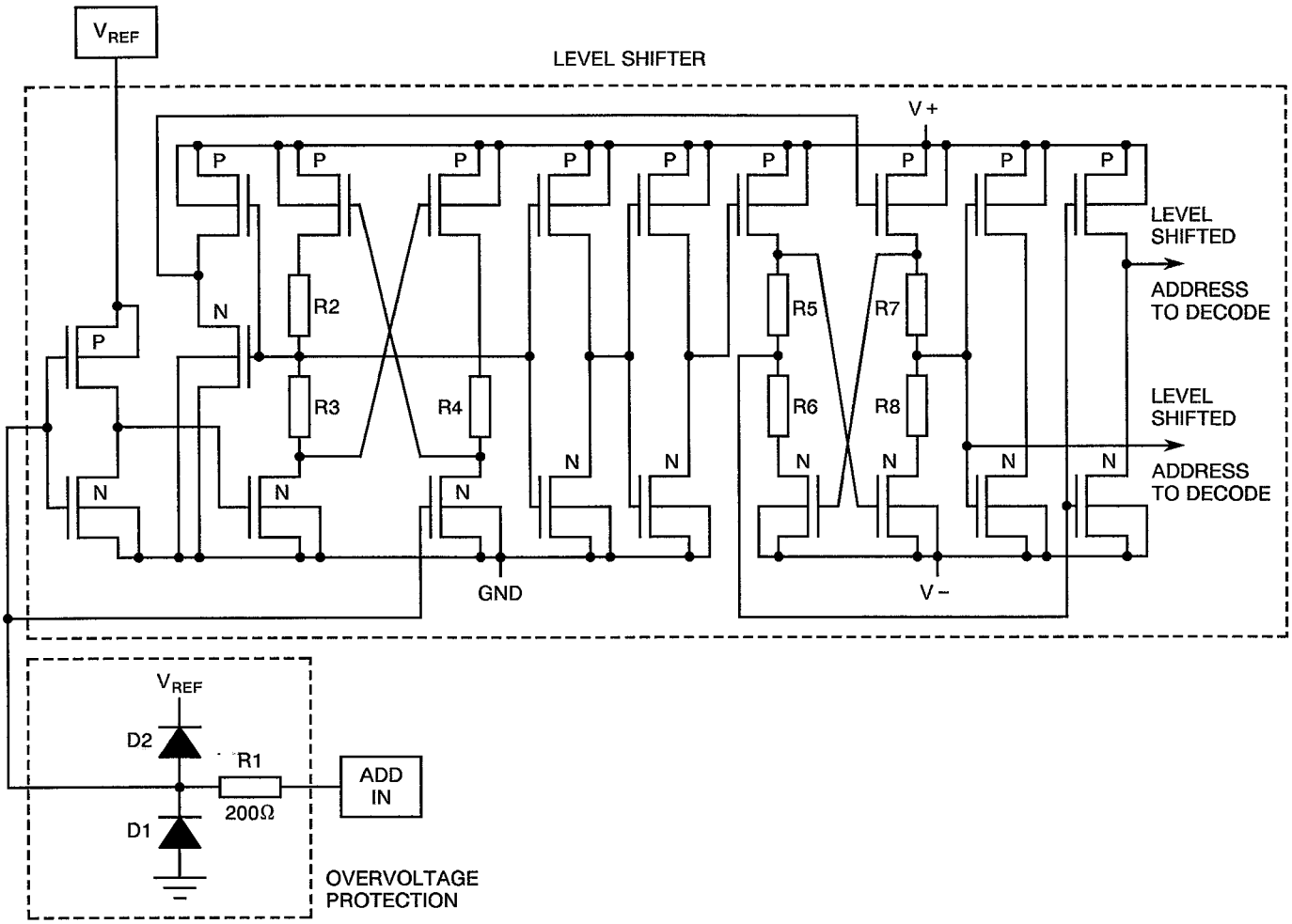
TOP VIEW

FIGURE 3(b) - TRUTH TABLE

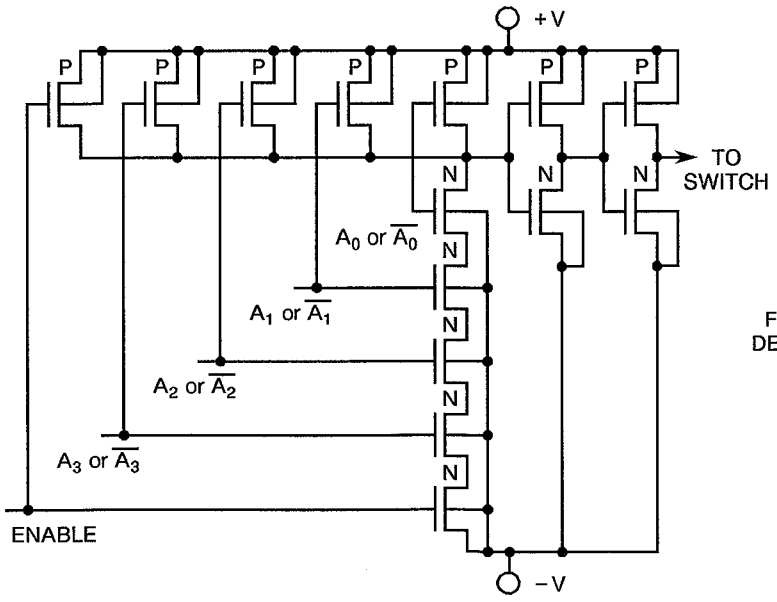
A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

FIGURE 3(c) - CIRCUIT SCHEMATIC

ADDRESS AND ENABLE INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEXER SWITCH

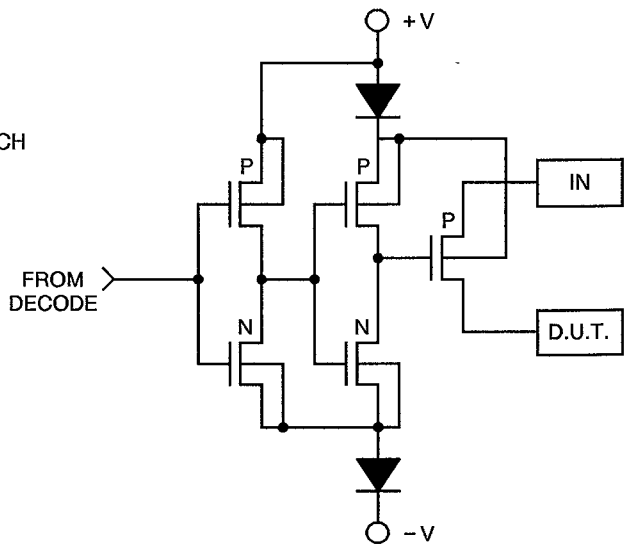


FIGURE 3(d) - FUNCTIONAL DIAGRAM

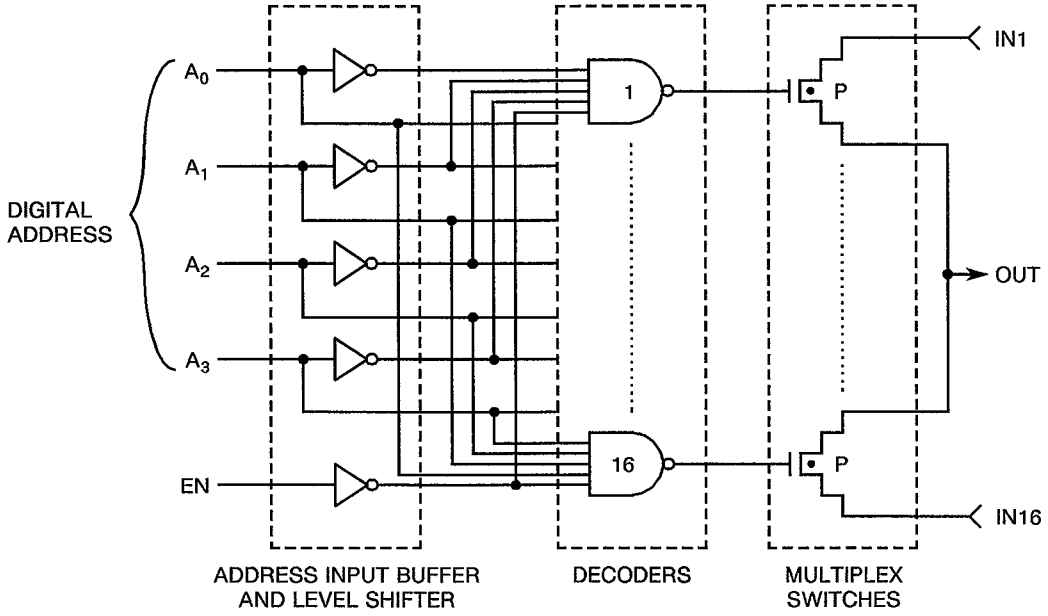
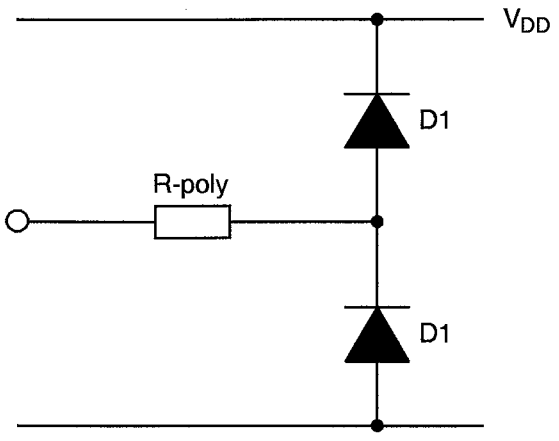


FIGURE 3(e) - INPUT PROTECTION NETWORK



4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 9, "High Temperature Reverse Bias" (H.T.R.B.): Not applicable.

4.2.4 Deviations from Qualification Tests (Chart IV)

None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

4.2.6 Radiation Screening Procedure

All devices supplied in accordance with this specification shall be from lots whose samples passed the radiation screening procedure as follows:-

STEP	RADIATION SCREENING PROCEDURE
1	Two (2) probed good samples per wafer will be selected from 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallisation).
2	The sample die shall be assembled and tested for functionality.
3	The sample devices shall be subjected to a Total Dose Radiation level of 2×10^4 Rad Si ($\pm$ 10%) from a Gamma Cell 220 rads/sec.
4	The samples will be tested to the data sheet limits within 1 hour ($\pm$ 15 minutes) after irradiation. The Lot will be accepted only if all units, exclusive of non-radiation failures, meet the Table 2 parameter limits.
5	The sample devices shall pass functional test(s) consisting of Logic 1's, Logic 0's and a checkerboard pattern.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 2.5 grammes for the dual-in-line package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed or preform-soldered.

4.4.2 Lead Material and Finish

The material shall be either Type 'D' or Type 'G' with either Type '2' or Type '3' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of components delivered to this specification shall be in accordance with ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

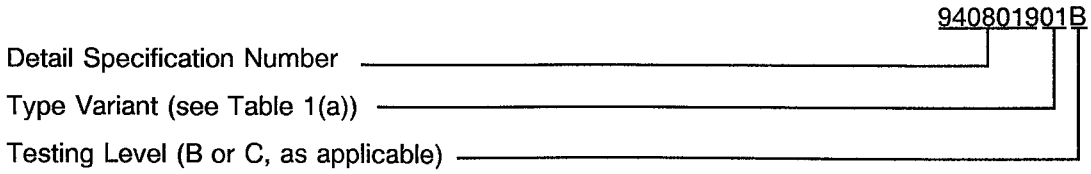
(c) Traceability Information.

4.5.2 Lead Identification

An index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab will be used to identify Pin No. 1. The pin numbering shall be read with the index or tab on the left-hand side.

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +25 \pm 5$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits and functional test sequence for use in performing the electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +25 \pm 5$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for H.T.R.B. and Burn-in

The requirements for H.T.R.B. and burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for H.T.R.B. and burn-in shall be as specified in Tables 5(a) and 5(b) of this specification.

4.7.3 Electrical Circuits for H.T.R.B. and Burn-in

Circuits for use in performing the H.T.R.B. and burn-in tests are shown in Figures 5(a) and 5(b) of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
1	Functional Test	-		4(a)	Verify Truth Table.	-	-	-
2 to 22	Input Current High Level 1, All Inputs	I_{IH1}	3010	4(b)	V_{IN} (under test) = 15V V_{IN} (other Inputs) = 0V $\overline{EN}$ = GND A_0, A_1, A_2, A_3 = 4.0V (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
23 to 44	Input Current High Level 2, All Inputs	I_{IH2}	3010	4(b)	V_{IN} (under test) = 4.0V V_{IN} (other Inputs) = GND $\overline{EN}$ = 15V A_0, A_1, A_2, A_3 = GND (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
45 to 66	Input Current Low Level 1, All Inputs	I_{IL1}	3009	4(c)	V_{IN} (under test) = 0V V_{IN} (other Inputs) = 15V A_0, A_1, A_2, A_3 = 4.0V (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
67 to 89	Input Current Low Level 2, All Inputs	I_{IL2}	3009	4(c)	V_{IN} (under test) = 4.0V V_{IN} (other Inputs) = GND A_0, A_1, A_2, A_3 = GND (Pins 4-5-6-7-8-9-10-11-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
90 to 106	Leakage Current into the Source Terminal of an "Off" Switch	$I_{S+(OFF)}$	-	4(d)	V_{IN} = −10V, OUT = 10V All unused inputs = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA
107 to 123		$I_{S-(OFF)}$			V_{IN} = 10V, OUT = 10V All unused inputs = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA
124 to 140	Leakage Current into the Source Terminal with Power "Off"	$I_{S\pm(OFF)}$	-	4(e)	$+V_S$, $-V_S$, V_{REF}, A_0, A_1, A_2, A_3, $\overline{EN}$ = Open Inputs = +10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
141 to 156	Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OFF)}$	-	4(f)	Connect All Inputs to −10V Output = 10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
157 to 172		$I_{D-(OFF)}$			Connect All Inputs to +10V Output = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
173 to 188	Leakage Current from an "Off" Driver into the Switch (Drain)	$I_{D+(ON)}$	-	4(g)	Connect All Unused Inputs to +10V, V_{IN} = −10V Output = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
189 to 204	Leakage Current from an "Off" Driver into the Switch (Drain)	$I_{D-(ON)}$	-	4(g)	Connect All Unused Inputs to −10V, V_{IN} = −10V Output = +10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
205 to 217	Overvoltage Protection, Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OVP)}$	3008	4(h)	Measure Inputs Sequentially V_{IN} = 35V, OUT = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	-	2.0	µA
218 to 233		$I_{D-(OVP)}$			Measure Inputs Sequentially V_{IN} = −25V, OUT = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
234 to 249	Overvoltage Protection, Leakage Current into the Source Terminal of an "Off"	$I_{S+(OVP)}$	3008	4(i)	Measure Inputs Sequentially V_{OUT} = +35V, V_{IN} = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−2.0	2.0	µA
250 to 265		$I_{S-(OVP)}$			Measure Inputs Sequentially V_{OUT} = −20V, V_{IN} = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	2.0	µA

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
266	Positive Supply Current	$I_{+(PSC)}$	3005	4(j)	$\underline{V_{IN}} = 0V$ $\overline{EN} = 0.8V$ (Pin 1)	-	500	µA
267	Negative Supply Current	$I_{-(PSC)}$	3005	4(j)	$\underline{V_{IN}} = 0V$ $\overline{EN} = 0.8V$ (Pin 27)	-	−500	µA
268	Positive Supply Standby Current	$I_{+(STDBY)}$	3005	4(j)	$\underline{V_{IN}} = 0V$ $\overline{EN} = 4.0V$ (Pin 1)	-	100	µA
269	Negative Supply Standby Current	$I_{-(STDBY)}$	3005	4(j)	$\underline{V_{IN}} = 0V$ $\overline{EN} = 4.0V$ (Pin 27)	-	−100	µA
270 to 285	Switch "On" Resistance	R_{1ON+}	-	4(k)	$\underline{V_{IN}} = +15V$ $\overline{EN} = 0.8V$ $I_{OUT} = +1.0mA$ (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 29)	-	1.0	kΩ
286 to 301		R_{2ON+}			$\underline{V_{IN}} = +5.0V$ $\overline{EN} = 0.8V$ $I_{OUT} = +1.0mA$ (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 28)	-	3.0	kΩ
302 to 317	Switch "On" Resistance	R_{1ON-}	-	4(k)	$\underline{V_{IN}} = 5.0V$ $\overline{EN} = 0.8V$ $I_{OUT} = +1.0mA$ (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 28)	-	5.0	kΩ

NOTES: See Page 20.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
318 to 319	Propagation Delay Times: Address Inputs	t_{PLH1}	-	-	$\overline{R_L}$ = 10mΩ, C_L = 14pF $\overline{EN}$ = 15V See Figure 4(a)	50	1000	ns
		t_{PHL1}				50	1000	
320 to 322	Enable to I/O	t_{PLH2} (t_{ON} EN)	-	-	$\overline{R_L}$ = 1.0kΩ, C_L = 12.5pF $\overline{EN}$ = Input V_{AL} = GND See Figure 4(a)	50	1000	ns
		t_{PHL2} (t_{OFF} EN)				50	1000	
323 to 326	Address Capacitance	C_A	-	-	V_{IN} = V_{CC} or GND f = 1.0MHz Note 3 (Pins 14-15-16-17)	-	5.0	pF
327	Output Capacitance	C_{OS}	-	-	V_{IN} = V_{EE} or GND f = 1.0MHz Note 3 (Pin 28)	-	50	pF
328 to 343	Input Capacitance	C_{IS}	-	-	V_{IN} = V_{CC} or GND f = 1.0MHz Note 3 (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	-	5.0	pF

NOTES

1. Current flowing in either direction between any associated input and output terminals of switch shall be 30mA maximum.
2. V_{IN} is the voltage applied to the channel inputs.
3. Guaranteed but not tested.
4. Unless otherwise specified:-
   $+V_S$ = 15V, $-V_S$ = −15V, V_{REF} = +15V, V_{N1} = 4.0V and V_{AL} = 0.8V.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C
d.c. PARAMETERS

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
1	Functional Test	-		4(a)	Verify Truth Table.	-	-	-
2 to 22	Input Current High Level 1, All Inputs	I_{IH1}	3010	4(b)	V_{IN} (under test) = 15V V_{IN} (other Inputs) = 0V $\overline{EN}$ = GND A_0, A_1, A_2, A_3 = 4.0Vdc (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
23 to 44	Input Current High Level 2, All Inputs	I_{IH2}	3010	4(b)	V_{IN} (under test) = 4.0V V_{IN} (other Inputs) = GND $\overline{EN}$ = 15V A_0, A_1, A_2, A_3 = GND (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
45 to 66	Input Current Low Level 1, All Inputs	I_{IL1}	3009	4(c)	V_{IN} (under test) = 0V V_{IN} (other Inputs) = 15V A_0, A_1, A_2, A_3 = 4.0V (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
67 to 89	Input Current Low Level 2, All Inputs	I_{IL2}	3009	4(c)	V_{IN} (under test) = 4.0V V_{IN} (other Inputs) = GND A_0, A_1, A_2, A_3 = GND (Pins 4-5-6-7-8-9-10-11-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
90 to 106	Leakage Current into the Source Terminal of an "Off" Switch	$I_{S+(OFF)}$	-	4(d)	V_{IN} = −10V, OUT = 10V All unused inputs = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA
107 to 123		$I_{S-(OFF)}$			V_{IN} = 10V, OUT = 10V All unused inputs = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA
124 to 140	Leakage Current into the Source Terminal with Power "Off"	$I_{S\pm(OFF)}$	-	4(e)	$+V_S$, $-V_S$, V_{REF}, A_0, A_1, A_2, A_3, $\overline{EN}$ = Open Inputs = +10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA

NOTES: See Page 20.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C
d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
141 to 156	Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OFF)}$	-	4(f)	Connect All Inputs to −10V Output = 10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
157 to 172		$I_{D-(OFF)}$			Connect All Inputs to +10V Output = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
173 to 188	Leakage Current from an "Off" Driver into the Switch (Drain)	$I_{D+(ON)}$	-	4(g)	Connect All Unused Inputs to +10V, V_{IN} = −10V Output = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
189 to 204	Leakage Current from an "Off" Driver into the Switch (Drain)	$I_{D-(ON)}$	-	4(g)	Connect All Unused Inputs to −10V, V_{IN} = −10V Output = +10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
205 to 217	Overvoltage Protection, Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OVP)}$	3008	4(h)	Measure Inputs Sequentially $\overline{V_{IN}}$ = 35V, OUT = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	-	2.0	µA
218 to 233		$I_{D-(OVP)}$			Measure Inputs Sequentially $\overline{V_{IN}}$ = −25V, OUT = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
234 to 249	Overvoltage Protection, Leakage Current into the Source Terminal of an "Off"	$I_{S+(OVP)}$	3008	4(i)	Measure Inputs Sequentially $\overline{V_{OUT}}$ = +35V, V_{IN} = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−2.0	2.0	µA
250 to 265		$I_{S-(OVP)}$			Measure Inputs Sequentially $\overline{V_{OUT}}$ = −20V, V_{IN} = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	2.0	µA

NOTES: See Page 20.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C
d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
266	Positive Supply Current	$I_{+(PSC)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 0.8V (Pin 1)	-	500	µA
267	Negative Supply Current	$I_{-(PSC)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 0.8V (Pin 27)	-	−500	µA
268	Positive Supply Standby Current	$I_{+(STDBY)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 4.0V (Pin 1)	-	100	µA
269	Negative Supply Standby Current	$I_{-(STDBY)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 4.0V (Pin 27)	-	−100	µA
270 to 285	Switch "On" Resistance	R_{1ON+}	-	4(k)	$\overline{V_{IN}}$ = +15V $\overline{EN}$ = 0.8V I_{OUT} = +1.0mA (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 29)	-	1.0	kΩ
286 to 301		R_{2ON+}			$\overline{V_{IN}}$ = +5.0V $\overline{EN}$ = 0.8V I_{OUT} = +1.0mA (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 28)	-	3.0	kΩ
302 to 317	Switch "On" Resistance	R_{1ON-}	-	4(k)	$\overline{V_{IN}}$ = 5.0V $\overline{EN}$ = 0.8V I_{OUT} = +1.0mA (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 28)	-	5.0	kΩ

NOTES: See Page 20.

TABLE 3(a) - ELECTRICAL MEASUREMENTS AT HIGH TEMPERATURE, +125(+0−5) °C
a.c. PARAMETERS

No.	Characteristics	Symbol	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
				Min	Max	
318 to 319	Propagation Delay Times: Address Inputs to I/O Channels	t_{PLH1}	R_L = 10mΩ, C_L = 14pF $\overline{EN}$ = 15V See Figure 4(a)	75	1000	ns
		t_{PHL1}		75	1000	
320 to 322	Enable to I/O	t_{PLH2} (t_{ON} EN)	R_L = 1.0kΩ, C_L = 12.5pF $\overline{EN}$ = Input V_{AL} = GND, V_{AH} = 15V See Figure 4(a)	75	1000	ns
		t_{PHL2} (t_{OFF} EN)		75	1000	

NOTES: See Page 20.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C
d.c. PARAMETERS

No.	Characteristics	Symbol	MIL-STD-883 Test Method	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
1	Functional Test	-		4(a)	Verify Truth Table.	-	-	-
2 to 22	Input Current High Level 1, All Inputs	I_{IH1}	3010	4(b)	V_{IN} (under test) = 15V $\underline{V_{IN}}$ (other Inputs) = 0V $\overline{EN}$ = GND A_0, A_1, A_2, A_3 = 4.0V (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
23 to 44	Input Current High Level 2, All Inputs	I_{IH2}	3010	4(b)	V_{IN} (under test) = 4.0V $\underline{V_{IN}}$ (other Inputs) = GND $\overline{EN}$ = 15V A_0, A_1, A_2, A_3 = GND (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
45 to 66	Input Current Low Level 1, All Inputs	I_{IL1}	3009	4(c)	V_{IN} (under test) = 0V V_{IN} (other Inputs) = 15V A_0, A_1, A_2, A_3 = 4.0V (Pins 4-5-6-7-8-9-10-11-12-14-15-16-17-18-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
67 to 89	Input Current Low Level 2, All Inputs	I_{IL2}	3009	4(c)	V_{IN} (under test) = 4.0V V_{IN} (other Inputs) = GND A_0, A_1, A_2, A_3 = GND (Pins 4-5-6-7-8-9-10-11-14-15-16-17-18-19-20-21-22-23-24-25-26-28)	−1.0	1.0	µA
90 to 106	Leakage Current into the Source Terminal of an "Off" Switch	$I_{S+(OFF)}$	-	4(d)	V_{IN} = −10V, OUT = 10V All unused inputs = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA
107 to 123		$I_{S-(OFF)}$			V_{IN} = 10V, OUT = 10V All unused inputs = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA
124 to 140	Leakage Current into the Source Terminal with Power "Off"	$I_{S\pm(OFF)}$	-	4(e)	$+\underline{V_S}$, $-V_S$, V_{REF}, A_0, A_1, A_2, A_3, $\overline{EN}$ = Open Inputs = +10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−100	100	nA

NOTES: See Page 20.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C
d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD-883	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
141 to 156	Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OFF)}$	-	4(f)	Connect All Inputs to −10V Output = 10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
157 to 172		$I_{D-(OFF)}$			Connect All Inputs to +10V Output = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
173 to 188	Leakage Current from an "Off" Driver into the Switch (Drain)	$I_{D+(ON)}$	-	4(g)	Connect All Unused Inputs to +10V, V_{IN} = −10V Output = −10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
189 to 204	Leakage Current from an "Off" Driver into the Switch (Drain)	$I_{D-(ON)}$	-	4(g)	Connect All Unused Inputs to −10V, V_{IN} = −10V Output = +10V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
205 to 217	Overvoltage Protection, Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OVP)}$	3008	4(h)	Measure Inputs Sequentially V_{IN} = 35V, OUT = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	-	2.0	µA
218 to 233		$I_{D-(OVP)}$			Measure Inputs Sequentially V_{IN} = −25V, OUT = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	1.0	µA
234 to 249	Overvoltage Protection, Leakage Current into the Source Terminal of an "Off"	$I_{S+(OVP)}$	3008	4(i)	Measure Inputs Sequentially V_{OUT} = +35V, V_{IN} = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−2.0	2.0	µA
250 to 265		$I_{S-(OVP)}$			Measure Inputs Sequentially V_{OUT} = −20V, V_{IN} = 0V $\overline{EN}$ = 4.0V (Pins 4-5-6-7-8-9-10-11-19-20-21-22-23-24-25-26)	−1.0	2.0	µA

NOTES: See Page 20.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C
d.c. PARAMETERS (CONT'D)

No.	Characteristics	Symbol	Test Method MIL-STD-883	Test Fig.	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
						Min	Max	
266	Positive Supply Current	$I_{+(PSC)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 0.8V (Pin 1)	-	500	µA
267	Negative Supply Current	$I_{-(PSC)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 0.8V (Pin 27)	-	−500	µA
268	Positive Supply Standby Current	$I_{+(STDBY)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 4.0V (Pin 1)	-	100	µA
269	Negative Supply Standby Current	$I_{-(STDBY)}$	3005	4(j)	$\overline{V_{IN}}$ = 0V $\overline{EN}$ = 4.0V (Pin 27)	-	−100	µA
270 to 285	Switch "On" Resistance	R_{1ON+}	-	4(k)	$\overline{V_{IN}}$ = +15V $\overline{EN}$ = 0.8V I_{OUT} = +1.0mA (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 29)	-	1.0	kΩ
286 to 301		R_{2ON+}			$\overline{V_{IN}}$ = +5.0V $\overline{EN}$ = 0.8V I_{OUT} = +1.0mA (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 28)	-	3.0	kΩ
302 to 317	Switch "On" Resistance	R_{1ON-}	-	4(k)	$\overline{V_{IN}}$ = 5.0V $\overline{EN}$ = 0.8V I_{OUT} = +1.0mA (Pins 4-5-6-7-8-9-10-11 to 28) (Pins 19-20-21-22-23-24-25-26 to 28)	-	5.0	kΩ

NOTES: See Page 20.

TABLE 3(b) - ELECTRICAL MEASUREMENTS AT LOW TEMPERATURE, −55(+5−0) °C
a.c. PARAMETERS

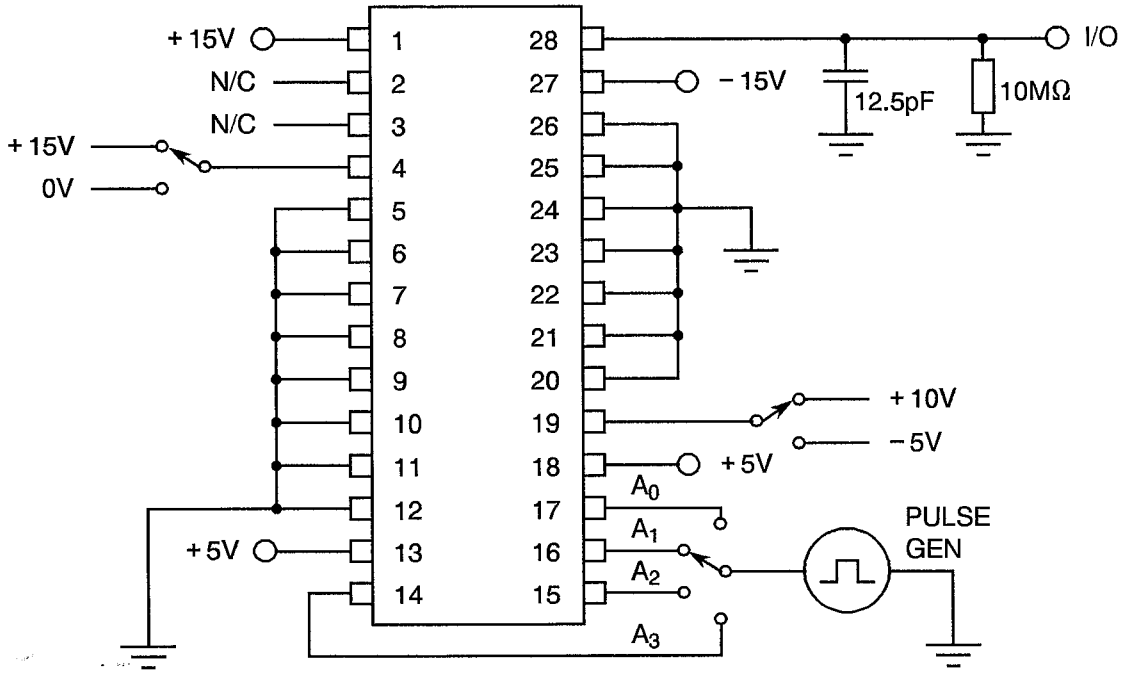
No.	Characteristics	Symbol	Test Conditions (Pins Under Test) (Notes 1, 2 and 4)	Limits		Unit
				Min	Max	
318 to 319	Propagation Delay Times: Address Inputs to I/O Channels	t_{PLH1}	R_L = 10mΩ, C_L = 14pF $\overline{EN}$ = 15V See Figure 4(a)	75	1000	ns
		t_{PHL1}		75	1000	
320 to 322	Enable to I/O	t_{PLH2} (t_{ON} EN)	R_L = 1.0kΩ, C_L = 12.5pF $\overline{EN}$ = Input V_{AL} = GND, V_{AH} = 15V See Figure 4(a)	75	1000	ns
		t_{PHL2} (t_{OFF} EN)		75	1000	

NOTES: See Page 20.

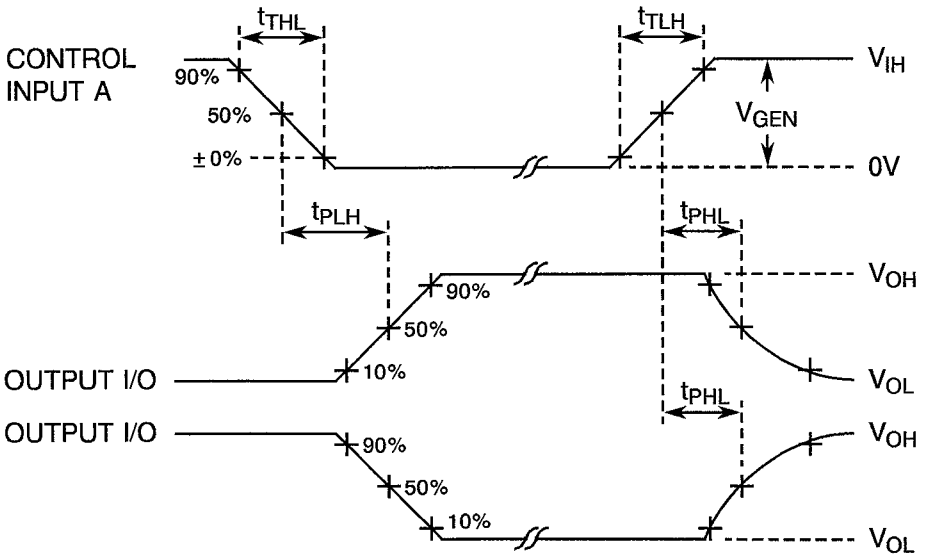
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

ADDRESS INPUTS TO I/O



DYNAMIC TEST WAVEFORMS



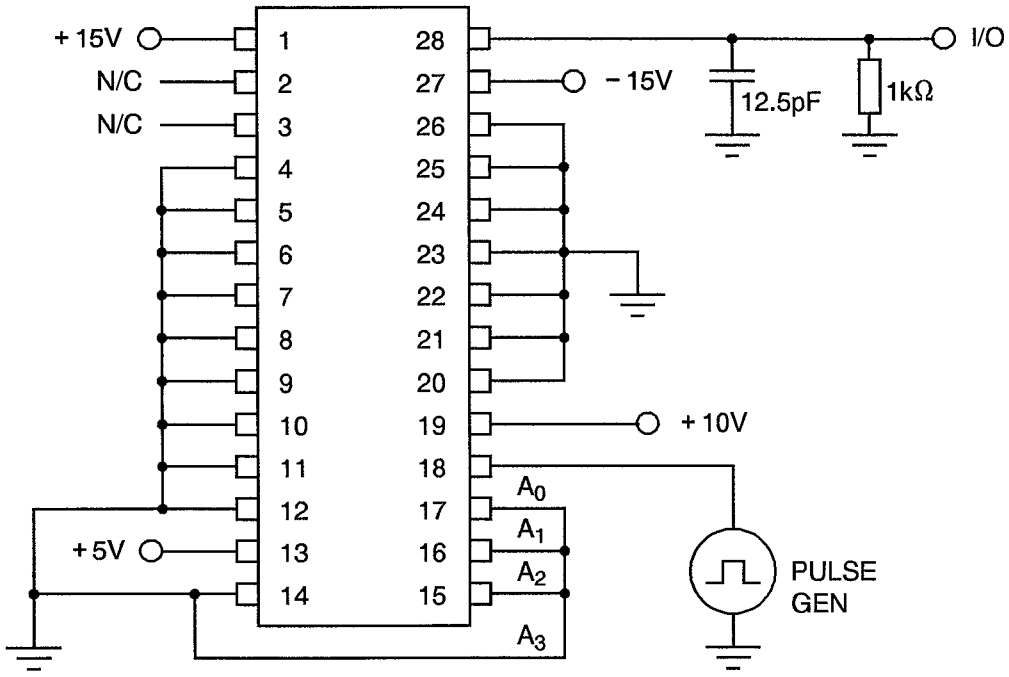
NOTES

1. Input pulse requirements: $V_{GEN} = 4.0V$, $t_{THL(1)} = t_{TLH(1)} \leq 20ns$.

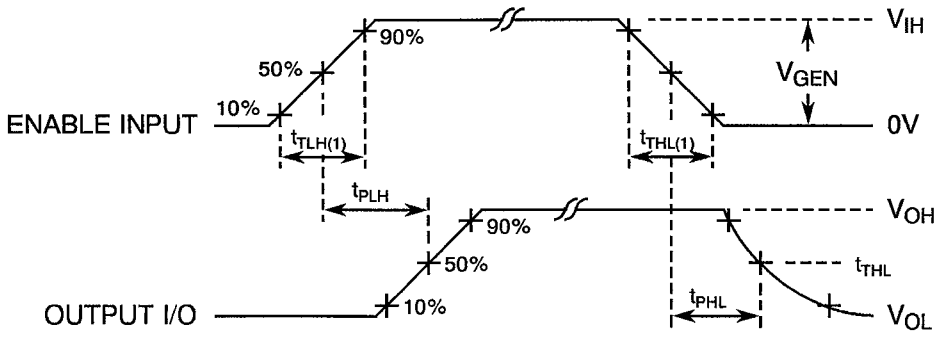
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONT'D)

FIGURE 4(a) - SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS (CONTINUED)

ENABLE TO I/O



DYNAMIC TEST WAVEFORMS

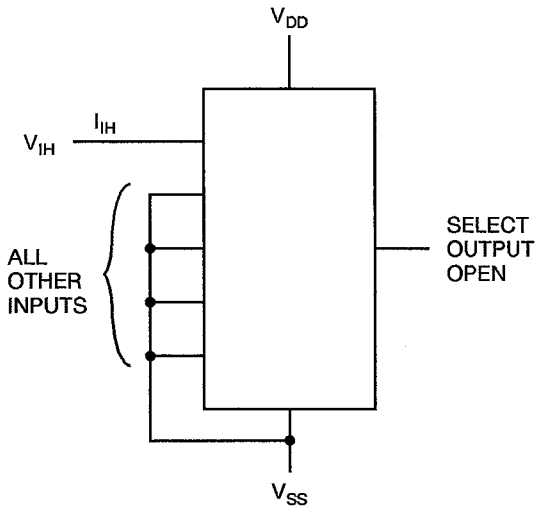


NOTES

1. Input pulse requirements: $V_{GEN} = 4.0V$, $t_{THL(1)} = t_{TLH(1)} \leq 20ns$.

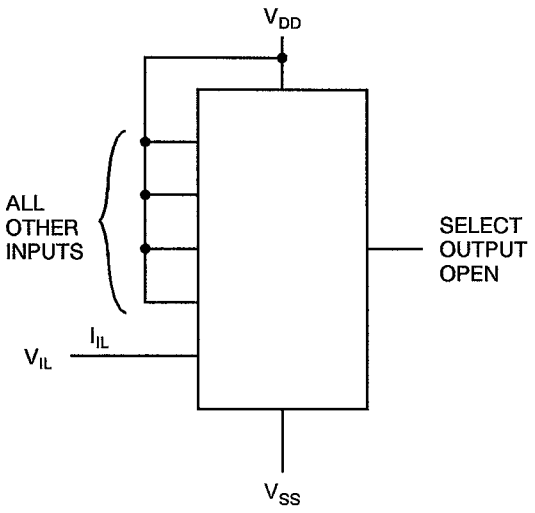
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(b) - INPUT CURRENT HIGH LEVEL



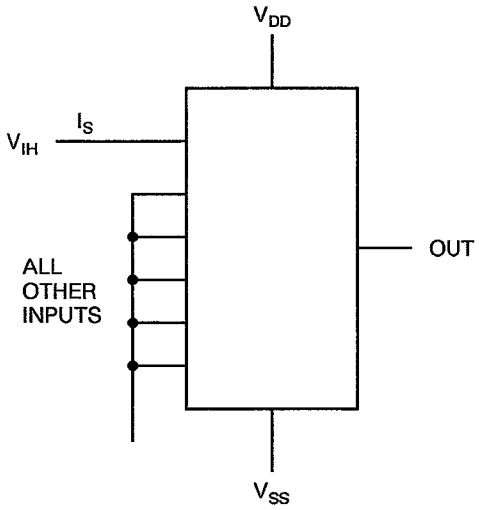
NOTES
1. Each input to be tested separately.

FIGURE 4(c) - INPUT CURRENT LOW LEVEL



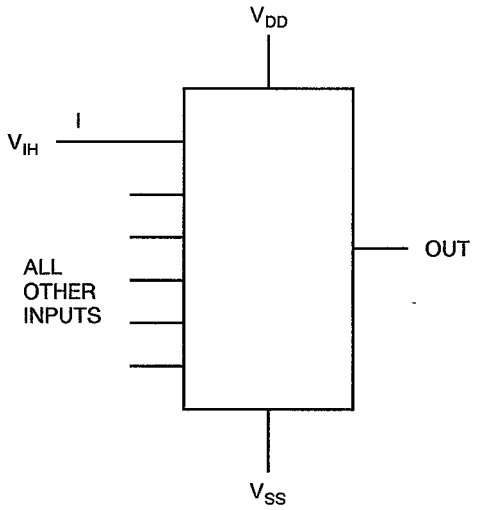
NOTES
1. Each input to be tested separately.

FIGURE 4(d) - LEAKAGE CURRENT INTO THE SOURCE TERMINAL OF AN "OFF" SWITCH



NOTES
1. All unused inputs to − 10V.

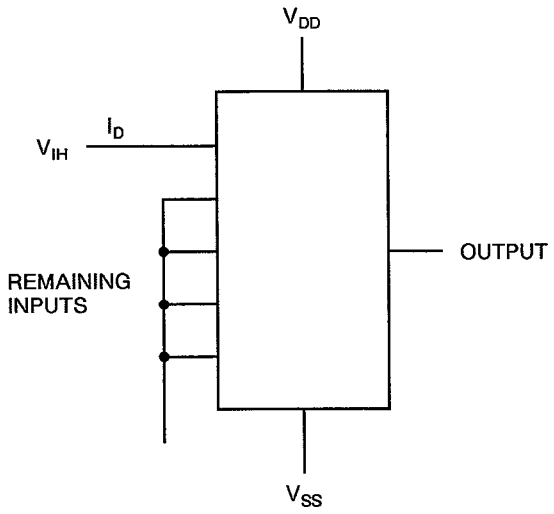
FIGURE 4(e) - LEAKAGE CURRENT INTO THE SOURCE TERMINAL WITH POWER "OFF"



NOTES
1. All unused inputs open.

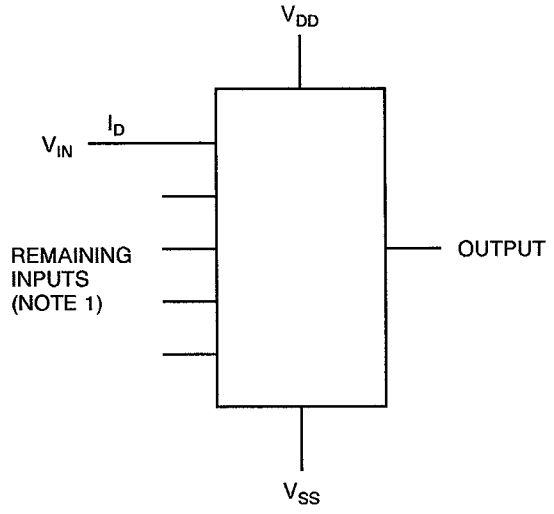
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(f) - LEAKAGE CURRENT INTO THE DRAIN TERMINAL OF AN "OFF" SWITCH



NOTES
1. Each input to be tested separately.

FIGURE 4(g) - LEAKAGE CURRENT FROM AN "OFF" DRIVER INTO THE SWITCH (DRAIN)



NOTES
1. Connect all unused inputs to −10V.

FIGURE 4(h) - OVERVOLTAGE PROTECTION, LEAKAGE CURRENT INTO THE DRAIN TERMINAL OF AN "OFF" SWITCH

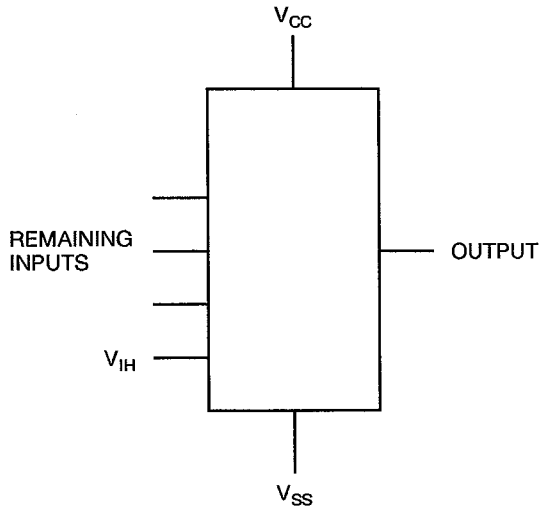
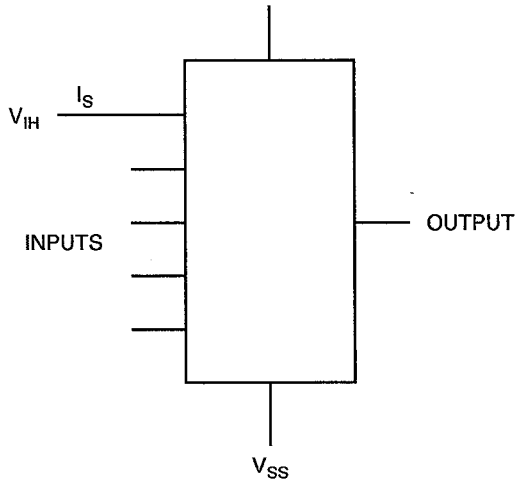


FIGURE 4(i) - OVERVOLTAGE PROTECTION, LEAKAGE CURRENT INTO THE SOURCE TERMINAL OF AN "OFF" SWITCH



NOTES
1. Measure inputs sequentially.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(j) - SUPPLY CURRENT

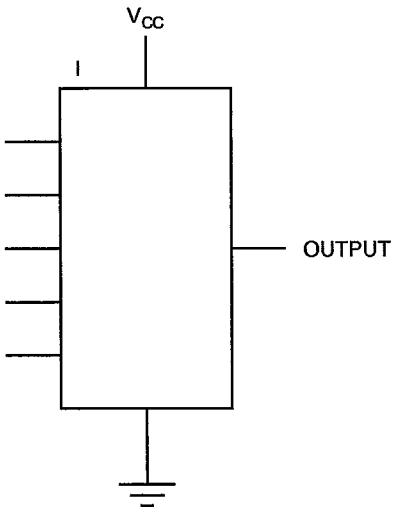
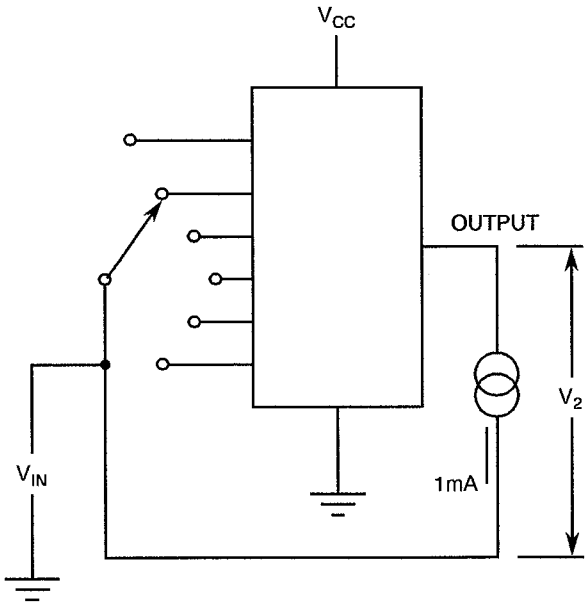


FIGURE 4(k) - SWITCH "ON" RESISTANCE



NOTES

1. $R_{ON} = \frac{V_2}{1mA}$

TABLE 4 - PARAMETER DRIFT VALUES

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2 to 22	Input Current High Level 1, All Inputs	I_{IH1}	As per Table 2	As per Table 2	±100 or (1) ±20	nA %
23 to 44	Input Current High Level 2, All Inputs	I_{IH2}	As per Table 2	As per Table 2	±100 or (1) ±20	nA %
45 to 66	Input Current Low Level 1, All Inputs	I_{IL1}	As per Table 2	As per Table 2	±100 or (1) ±15	nA %
67 to 89	Input Current Low Level 2, All Inputs	I_{IL2}	As per Table 2	As per Table 2	±100 or (1) ±15	nA %
266	Positive Supply Current	$I_{+(PSC)}$	As per Table 2	As per Table 2	Note 2	-
267	Negative Supply Current	$I_{-(PSC)}$	As per Table 2	As per Table 2	Note 2	-
270 to 285	Switch "On" Resistance 1	R_{1ON+}	As per Table 2	As per Table 2	±10	%
286 to 301	Switch "On" Resistance 2	R_{2ON+}	As per Table 2	As per Table 2	±10	%

NOTES

1. Whichever is greater, referred to the initial value.
2. The absolute value of Table 2, only, shall be applied.

TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+135 min.	°C
2	Input Signals		None	
3	Positive Supply Voltage	$+V_S$	+15 ± 10%	V
4	Negative Supply Voltage	$-V_S$	−15 ± 10%	V
5	Reference Voltage	V_R	+5 ± 10%	V
6	Duration	t	≥48	Hrs

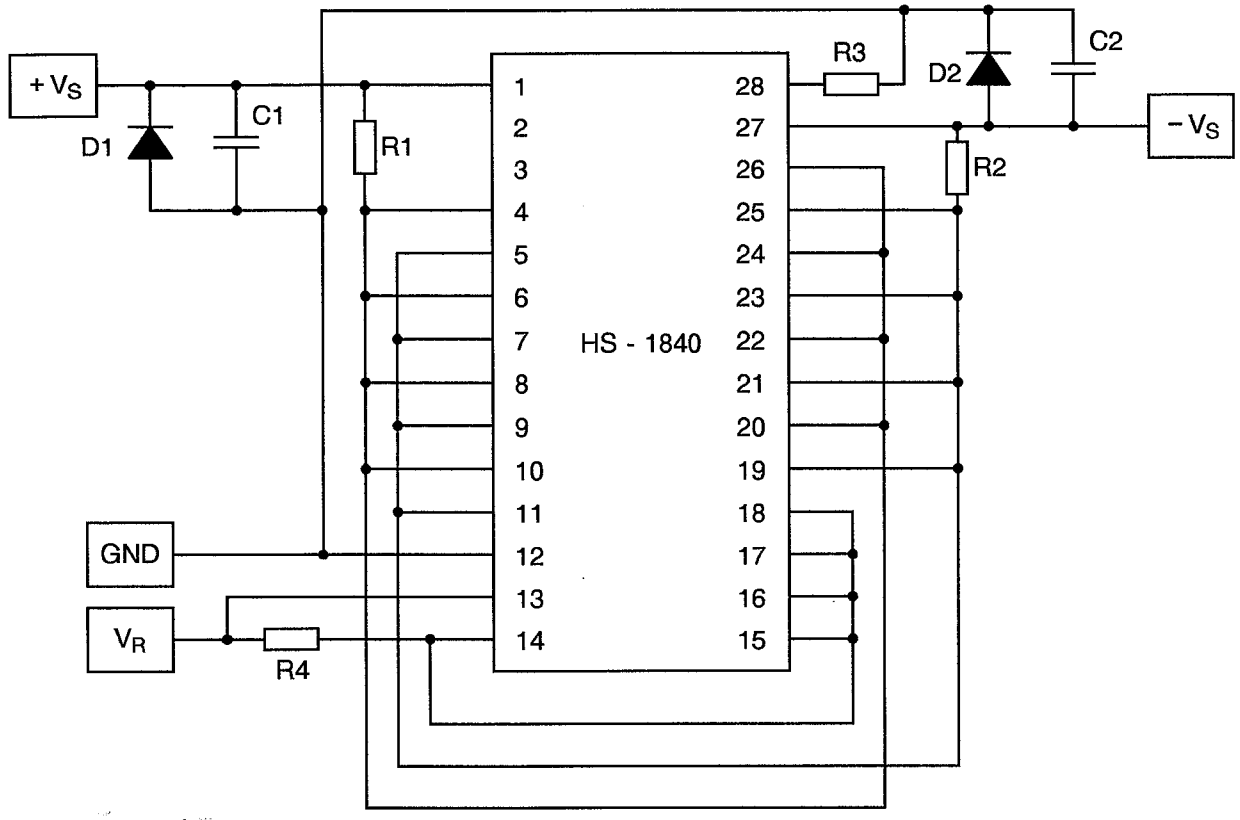
NOTES

1. Cool device down to ≤ +35°C, under bias, measure within 24 hours, after removal from bias.

TABLE 5(b) - CONDITIONS FOR BURN-IN, DYNAMIC AND OPERATING LIFE TESTS

No.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125 min.	°C
2	Outputs	V_{OUT}	$V_{DD/2}$	V
3	Input	V_{IN}	V_{GEN}	Vac
4	Input	V_{IN}	V_{GEN2}	Vac
5	Pulse Voltage	V_{GEN1} V_{GEN2}	0V to +15 peak minimum	Vac
6	Pulse Frequency Square Wave (V_{GEN1}) - (Pin 17)	F_1	100	kHz
7	Pulse Frequency Square Wave (V_{GEN2}) - (Pin 16)	F_2	50	kHz
8	Pulse Frequency Square Wave (V_{GEN3}) - (Pin 15)	F_3	25	kHz
9	Pulse Frequency Square Wave (V_{GEN4}) - (Pin 14)	F_4	12.5	kHz
10	Pulse Frequency Square Wave (V_{GEN5}) - (Pin 18)	F_5	6.25	kHz
11	Positive Supply Voltage - (Pin 1)	$+V_S$	+15 ± 10%	V
12	Negative Supply Voltage - (Pin 27)	$-V_S$	−15 ± 10%	V

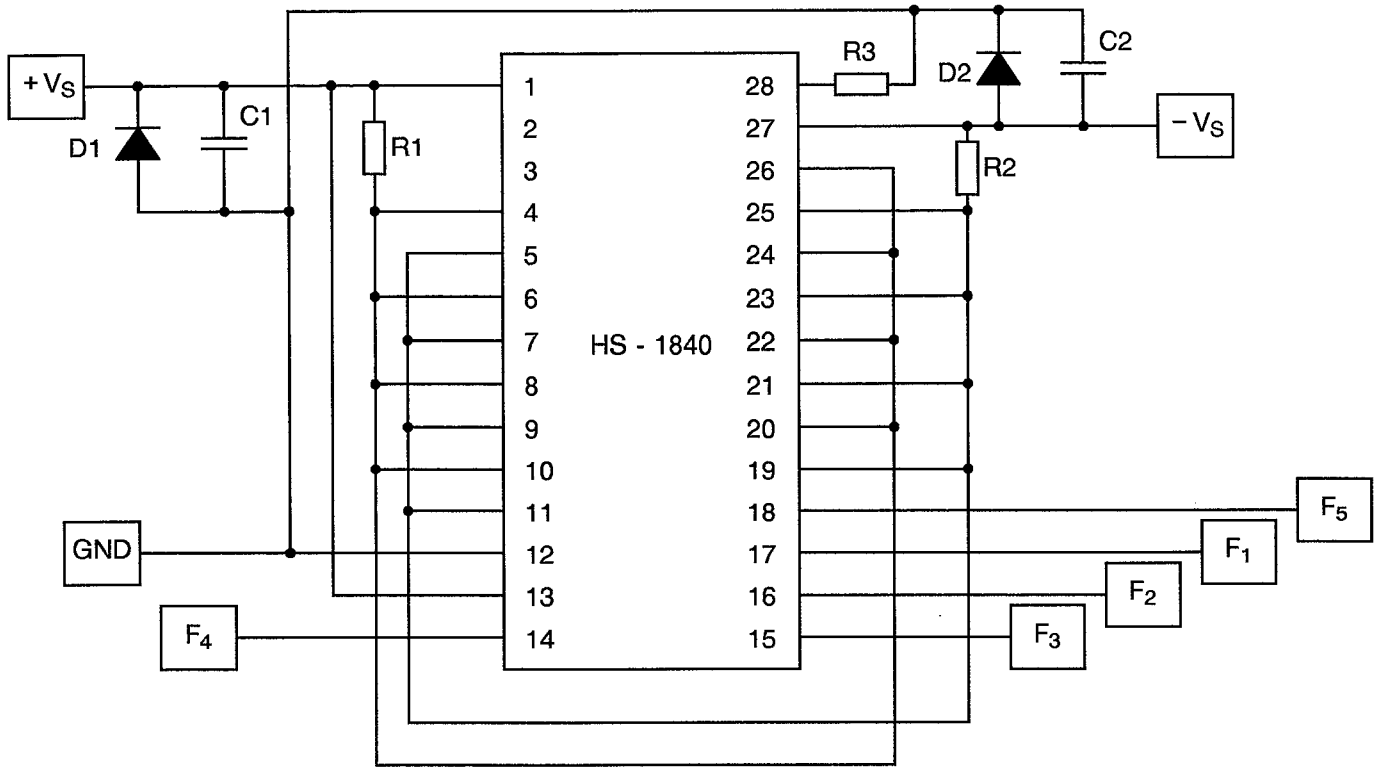
FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN AND ACCELERATED LIFE



Ambient temp. = +135°C min.
Package = 28 pin CerDIP, 1M
Input signals = none.

R1 - R4 = 1kΩ ±5%
C1 - C2 = 0.01μF, one each per socket
D1 - D2 = 1N4002 or equivalent, one each per board
$-V_S$ = −15V ±10%, $+V_S$ = +15V ±10%
V_R = +15V ±10%
$I_{(+V_S)}$ ≤ 100μA per device
$I_{(-V_S)}$ ≤ 100μA per device

FIGURE 5(b) - ELECTRICAL CIRCUIT FOR BURN-IN, DYNAMIC AND OPERATING LIFE TESTS



Ambient temp. = +125°C min.
Package = 28 pin CerDIP, 1M
Input signals:
(a) Square wave, 50% duty cycle, 0 to +15V peak, minimum
(b) F_1 = 100kHz
F_2 = 50kHz
F_3 = 25kHz
F_4 = 12.5kHz
F_5 = 6.25kHz
(c) t_{TLH} and t_{THL} < 1µs

R1 - R3 = 1kΩ ± 5%, ¼ watt min.
C1 - C2 = 0.01µF, one each per socket
D1 - D2 = 1N4002 or equivalent, one each per board
$+V_S$ = +15V ± 10%
$-V_S$ = −15V ± 10%

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 5$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 5$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +25 \pm 5$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0-5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

No.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	LIMITS		UNIT
					MIN	MAX	
1	Functional Test	-	As per Table 2	As per Table 2	-	-	-
2 to 22	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	−1.0	1.0	µA
23 to 44	Input Current High Level 2	I_{IH2}	As per Table 2	As per Table 2	−1.0	1.0	µA
45 to 66	Input Leakage Current Low Level 1	I_{IL1}	As per Table 2	As per Table 2	−1.0	1.0	µA
67 to 89	Input Leakage Current Low Level 2	I_{IL2}	As per Table 2	As per Table 2	−1.0	1.0	µA
141 to 156	Overvoltage Protection, Leakage Current into the Drain Terminal of an "Off" Switch	$I_{D+(OFF)}$	As per Table 2	As per Table 2	−2.0	2.0	µA
157 to 172		$I_{D-(OFF)}$			−1.0	1.0	
266	Positive Supply Current	$I_{+(PSC)}$	As per Table 2	As per Table 2	-	500	µA
267	Negative Supply Current	$I_{-(PSC)}$	As per Table 2	As per Table 2	-	−500	µA
270 to 285	Switch "On" Resistance	R_{1ON+}	As per Table 2	As per Table 2	-	1.5	kΩ
286 to 301	Switch "On" Resistance	R_{2ON+}	As per Table 2	As per Table 2	-	3.0	kΩ
302 to 317	Switch "On" Resistance	R_{1ON-}	As per Table 2	As per Table 2	-	5.0	kΩ

APPENDIX 'A'

AGREED DEVIATIONS FOR HARRIS (U.S.)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Deviations from Special In-process Controls (Para. 5.1) (a) Para. 5.1.1, "Scanning Electron Microscope Inspection" (SEM) This shall be performed in accordance with Method 2018 of MIL-STD-883, with the following exceptions:- 1. A SEM lot is defined at the metallisation step. One wafer is selected from the inside row and one from the outside row of the same planet. Sampling condition B_2 (segment, prior to glassivation) is used regardless of the glassivation temperature. 2. All four directional edges of every type of oxide step shall be examined on each wafer. The Manufacturer shall mount each of the wafer's four sample dice 90° out of phase from each other, so that all four edge directions can be properly inspected on each wafer. Questionable steps which are not at the proper viewing angle are inspected by rotating the sample as needed. 3. A lot is unacceptable if the directional edge of any contact window, or other type of oxide step, has a reduced cross-sectional area greater than 50%, or if it is reduced in thickness such that, at worst case specified the limits specified in MIL-M-38510, Para. 3.5.5 (5×10^5 A/cm^2 for glassivated aluminium products). The current density is determined per Para. 3.5.5(a) of MIL-M-38510. Reduced cross-sectional area due to voids or defects that can be readily observed by Method 2010 of MIL-STD-883, "Visual Inspection of Metallisation", is no cause for SEM lot rejection. 4. A lot is unacceptable if the general metallisation (metallisation at all locations except at oxide steps) shows peeling or lifting as a result of poor adhesion. General metallisation is unacceptable if voiding or undercutting of the metal reduces the cross-sectional area by more than 50% or if it is reduced in thickness such that, at worst case specified operating conditions, the current density exceeds the limits specified in MIL-M-38510, Para. 3.5.5. Voids and defects in the general metallisation that can be readily observed by Method 2010 of MIL-STD-883, "Visual Inspection of Metallisation", are no cause for SEM lot rejection.

APPENDIX 'A'

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Deviations from Special In-process Controls (Para. 5.1) 1.0 PRE-CAP INSPECTION The criteria of Para. 3.1.1.1 of Method 2010 Test Condition A shall be changed to read as follows: 1.1 Metallisation Scratches. A scratch is any tearing defect including probe marks in the surface of the metallisation: (a) Scratch in the metallisation excluding bonding pads and beam leads that leaves less than 50% of the original metal width undisturbed (see Figure 2010-1). (b) Scratch in the metallisation over a passivation step that leaves less than 50% of the original metal width at the step undisturbed. (c) Scratch in the bonding pad or fillet area that reduces the metallisation path width connecting the bond to the interconnecting metallisation to less than 50% of the narrowest entering interconnect metallisation stripe width. If two or more stripes enter a bonding pad, each shall be considered separately. (d) Scratch in the metallisation, over the gate oxide bridge (see Figure 2010-3) (applicable to MOS structures). (e) Scratch in the multilayered metallisation excluding bonding pads and beam leads that exposes underlying metal or passivation anywhere along its length and leaves less than 50% of the original metal width undisturbed (see Figure 2010-1). (f) Scratch(es) (probe mark(s), etc.,) in the bonding area that exposes underlying passivation over more than 50% of the original unglassivated metallisation area.