european space agency
agence spatiale européenne

Pages 1 to 37

INTEGRATED CIRCUITS, SILICON MONOLITHIC, BIPOLAR, ADVANCED LOW POWER SCHOTTKY, OCTAL BUS TRANSCEIVERS WITH INDEPENDANT REGISTERS FOR A AND B BUSES, TRUE DATA PATHS AND 3-STATE BUFFERED OUTPUTS, BASED ON TYPE 54ALS646

ESA/SCC Detail Specification No. 9405/009

space components
coordination group

Issue/Rev.	Date	Approved by	
		SCCG Chairman	ESA Director General or his Deputy
Issue 1	August 1991		
Revision 'A'	February 1992		
Revision 'B'	June 1994		

DOCUMENTATION CHANGE NOTICE

Rev. Letter	Rev. Date	Reference	CHANGE Item	Approved DCR No.
'A'	Feb.'92	Cover Page		None
		DCN		None
		P12. Figure 3(b)	: In Table line 2, Operation or Function corrected	22973
			: Notes 2 and 3 added	22973
		P14. Para. 4.2.3	: New deviation "(a)" added and existing deviation renumbered "(b)"	21048
		Para. 4.2.4	: Deviation deleted, "None" added	22919
		Para. 4.2.5	: Deviation deleted, "None" added	22919
		P34. Figure 5	: Resistor reference corrected on Pins 1,2, 23	22973
			: Resistors R1 added to Pins 3, 21, 22	22973
			: Note 2 corrected.	22973
'B'	June '94	P1. Cover Page		None
		P2. DCN		None
		P15. Para. 4.3.2	: Weights amended	221047

TABLE OF CONTENTS

Page

TABLES

FIGURES

APPENDICES (Applicable to specific Manufacturers only)

1. GENERAL

1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a silicon monolithic, bipolar, advanced low power Schottky, Octal Bus Transceiver with Independant Registers for A and B Buses, True Data Path and 3-State Buffered Outputs, based on Type 54ALS646. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

1.5 PHYSICAL DIMENSIONS

The physical dimensions of the integrated circuits specified herein are shown in Figure 2.

1.6 PIN ASSIGNMENT

As per Figure 3(a).

1.7 TRUTH TABLE

As per Figure 3(b).

1.8 CIRCUIT SCHEMATIC

As per Figure 3(c).

1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

TABLE 1(a) - TYPE VARIANTS

VARIANT	CASE	FIGURE	LEAD MATERIAL AND/OR FINISH
02	FLAT	2(a)	G4
03	CHIP CARRIER	2(b)	7
04	CHIP CARRIER	2(b)	4
06	DIL	2(c)	G4

TABLE 1(b) - MAXIMUM RATINGS

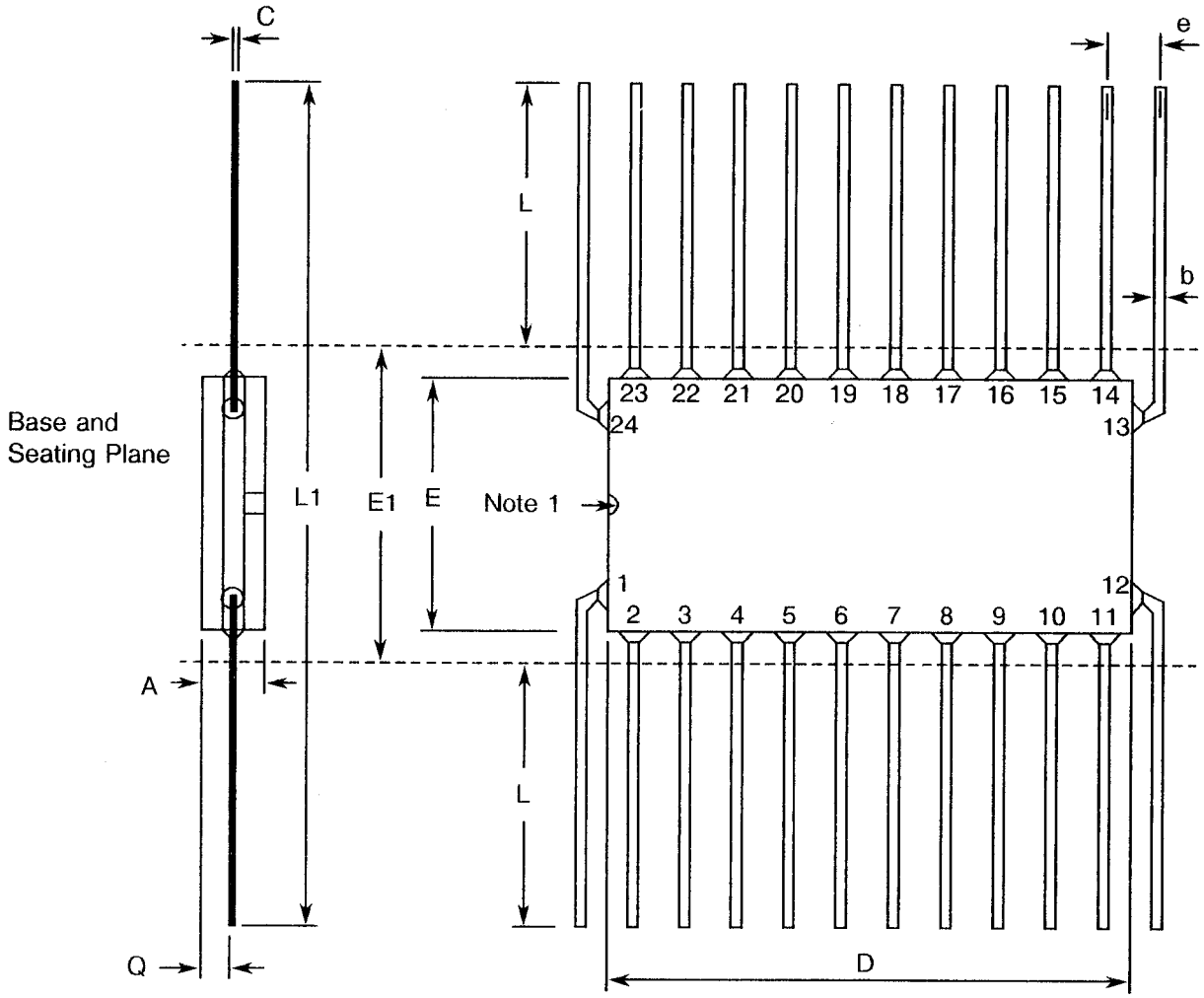
NO.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
1	Supply Voltage	V_{CC}	– 0.5 to 7.0	V	-
2	Input Voltage	V_{IN}	– 0.5 to 7.0	V	Note 1
3	Voltage Applied to Disabled 3-State Output	V_Z	5.5	V	-
4	Device Dissipation	P_D	484	mWdc	Note 2
5	Operating Temperature Range	T_{op}	– 55 to + 125	°C	T_{amb}
6	Storage Temperature Range	T_{stg}	– 65 to + 150	°C	-
7	Soldering Temperature For FP and DIP For CCP	T_{sol}	 + 265 + 245	°C	 Note 3 Note 4

NOTES

1. Input Current limited to – 18mA.
2. Must withstand added P_D due to short circuit conditions (i.e. I_{OS}) at 1 output for 5 seconds.
3. Duration 10 seconds maximum at a distance of not less than 1.5mm from the package and the same lead shall not be resoldered until 3 minutes have elapsed.
4. Duration 5 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - FLAT PACKAGE, 24 PIN

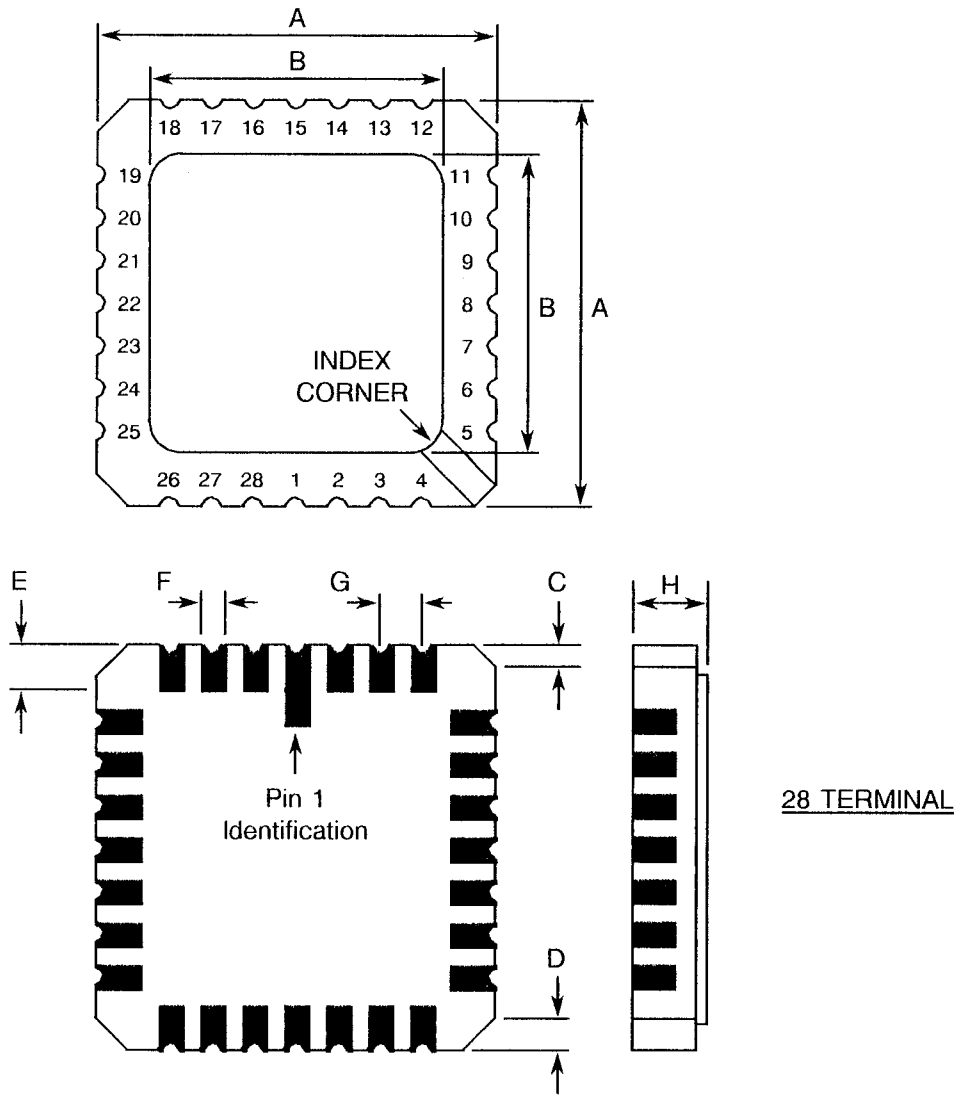


SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.39	2.16	
b	0.38	0.56	8
C	0.08	0.23	8
D	12.30	-	
E	8.50	10.10	
E_1	10.16 TYPICAL		4
e	1.27 TYPICAL		5, 9
L	6.98	10.16	
L_1	24.13	30.48	
Q	0.25	1.02	2

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(b) - SQUARE CHIP CARRIER PACKAGE (3 LAYER BASE)



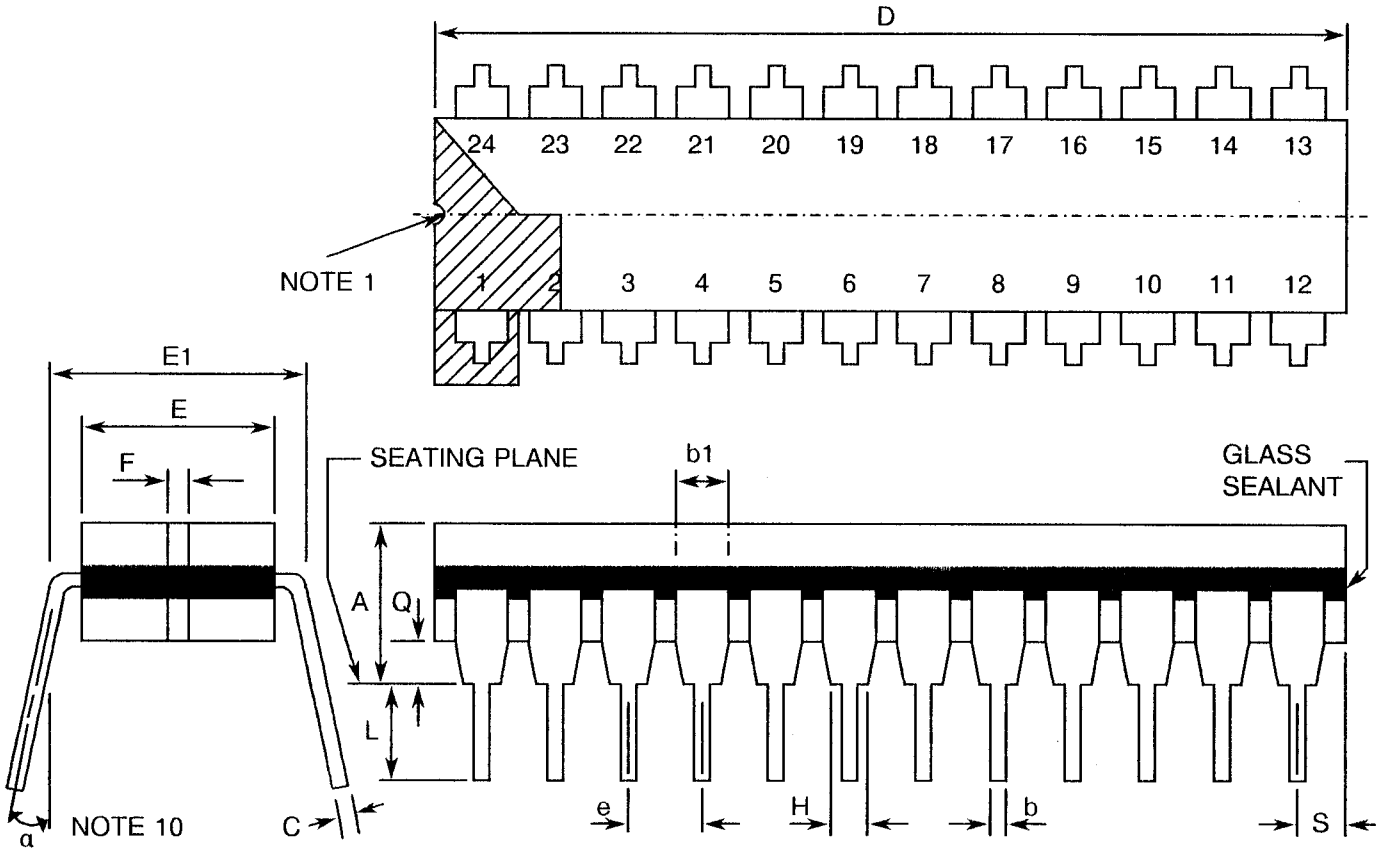
28 TERMINAL

SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	11.23	11.63	
B	10.31	11.63	
C	0.25	0.51	11
D	0.89	1.14	12
E	1.14	1.40	8
F	0.56	0.71	8
G	1.27 TYPICAL		5, 9
H	1.63	2.54	

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - DUAL-IN-LINE PACKAGE, 24 PIN



SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	-	5.08	
b	0.38	0.66	8
b1	-	1.78	8
C	0.20	0.44	8
D	31.50	32.51	4
E	6.22	7.62	4
E1	7.37	8.13	4
e	2.54 TYPICAL		6, 9
F	1.27 TYPICAL		
H	0.76	-	8
L	3.30	5.08	8
Q	0.51	-	3
S	1.78	2.54	7
α	0°	15°	10

NOTES: See Page 10.

FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

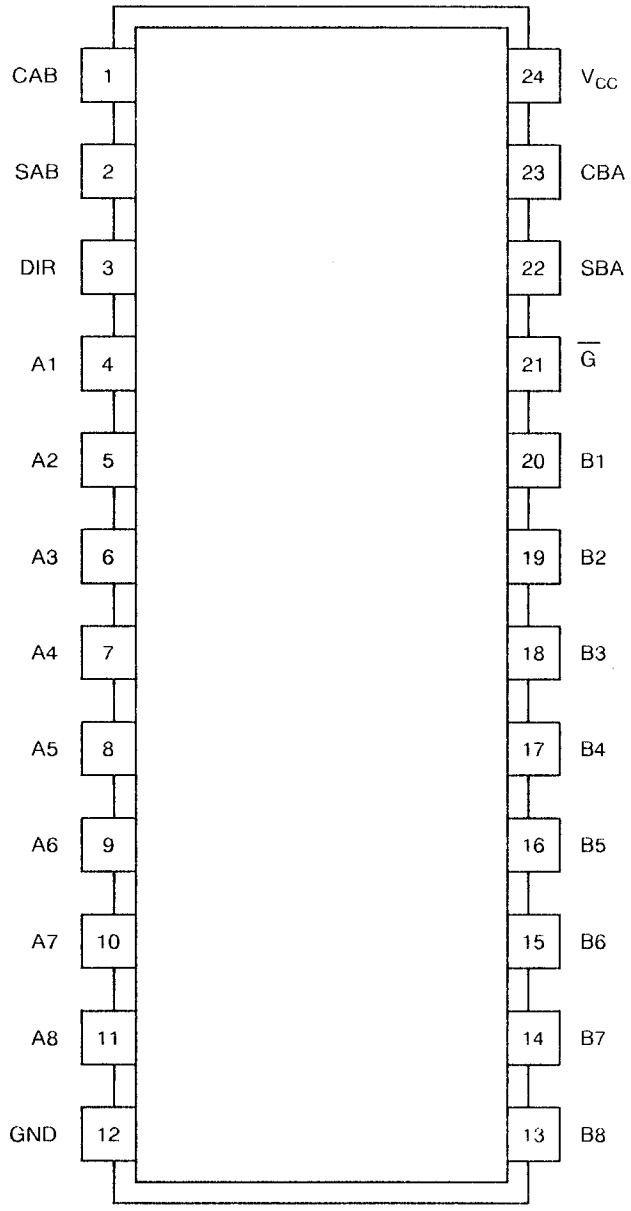
NOTES TO FIGURES 2(a) TO 2(c) INCLUSIVE

1. Index area; a notch or dot shall be located adjacent to Pin 1 and shall be within the shaded area shown. For chip carrier packages the index shall be as defined in Figure 2(b).
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-centre lids, meniscus and glass overrun.
5. The true position pin or terminal spacing is 1.27mm between centrelines. Each pin or terminal centreline shall be located within ± 0.13mm of its true longitudinal position relative to Pins 1 and the highest pin number.
6. The true position pin spacing is 2.54mm between centrelines. Each pin centreline shall be located within ± 0.25mm of its true longitudinal position relative to Pins 1 and the highest pin number.
7. Applies to all 4 corners.
8. All leads or terminals.
9. 22 spaces for flat and dual-in-line packages.

   26 spaces for chip carrier packages.
10. Lead centre when α is 0°.
11. Index corner only - 2 dimensions.
12. 3 non-index corners - 6 dimensions.

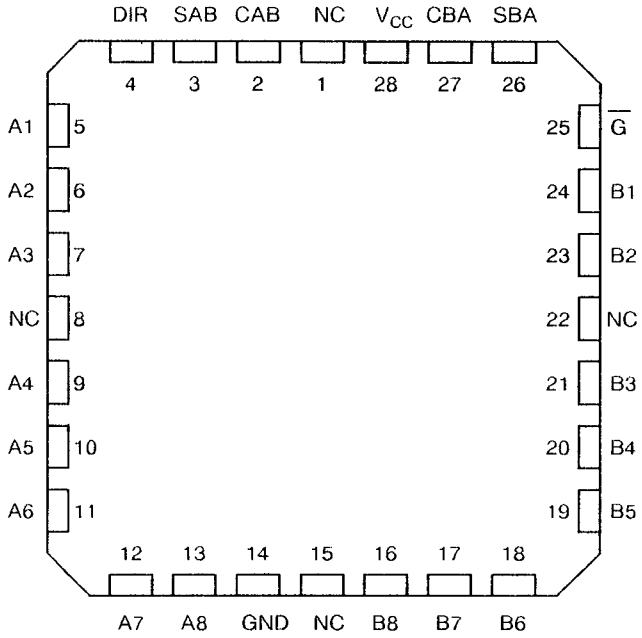
FIGURE 3(a) - PIN ASSIGNMENT

DUAL-IN-LINE AND FLAT PACKAGE



TOP VIEW

CHIP CARRIER PACKAGE



TOP VIEW

FLAT PACKAGE AND DUAL-IN-LINE TO CHIP CARRIER PIN ASSIGNMENT

FLAT PACKAGE AND DUAL-IN-LINE PIN OUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
CHIP CARRIER PIN OUTS	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28

FIGURE 3(b) - TRUTH TABLE

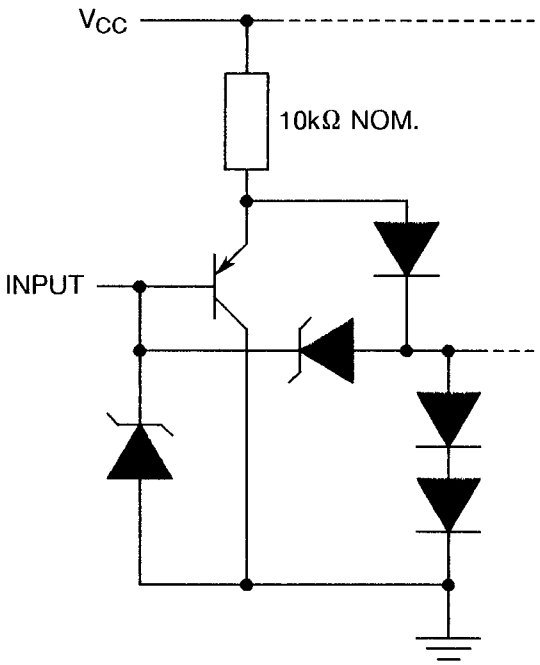
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	INPUT	UNSPECIFIED (1)	STORE A, B UNSPECIFIED (1)
X	X	X	↑	X	X	UNSPECIFIED (1)	INPUT	STORE B, A UNSPECIFIED (1)
H	X	↑	↑	X	X	INPUT	INPUT	STORE A AND B DATA
H	X	H OR L	H OR L	X	X			ISOLATION, HOLD STORAGE WITH OUT AT 2 LEVEL
L	L	X	H OR L	X	L	OUTPUT	INPUT	REAL TIME B DATA TO A BUS
L	L	X	H OR L	X	H			STORED B DATA TO A BUS
L	H	H OR L	X	L	X	INPUT	OUTPUT	REAL TIME A DATA TO B BUS
L	H	H OR L	X	H	X			STORED A DATA TO B BUS

NOTES

1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every Low-to-High transition on the clock inputs.
2. Logic Level Definitions: L = Low Level, H = High Level, X = Irrelevant.
3. ↑ = Transition from Low to High Level.

FIGURE 3(c) - CIRCUIT SCHEMATIC

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS

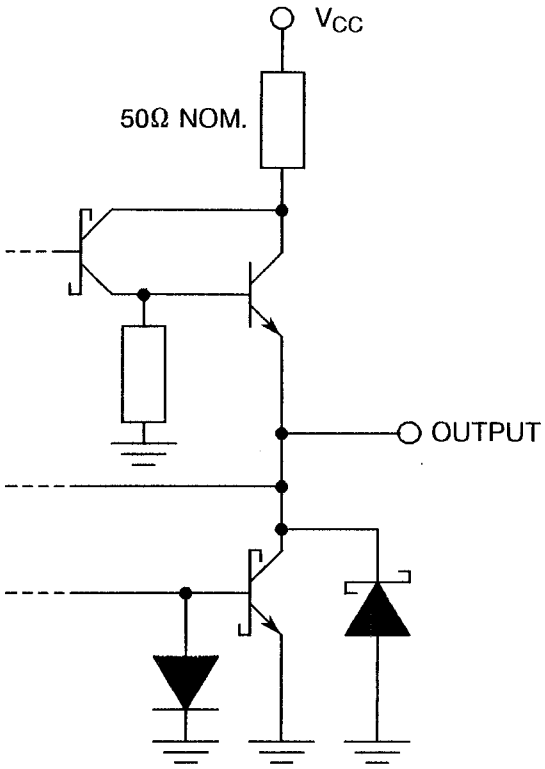
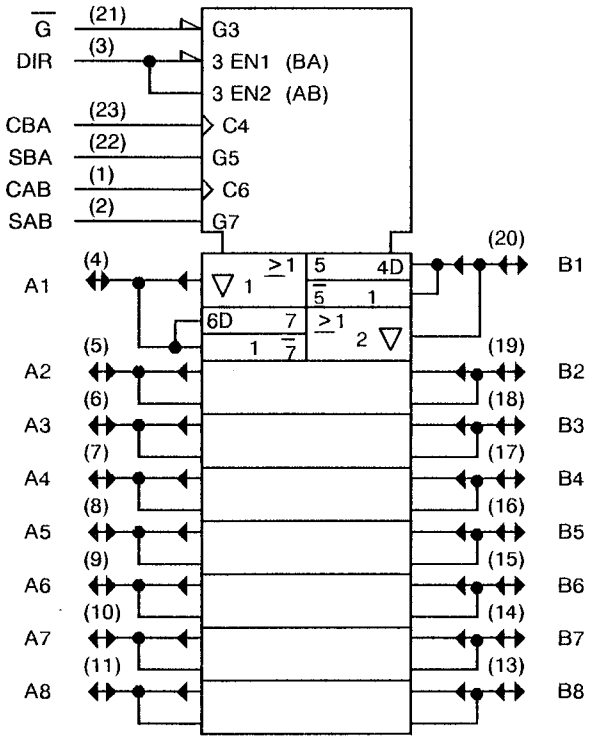


FIGURE 3(d) - FUNCTIONAL DIAGRAM



NOTES

1. Pin numbers shown are for flat and dual-in-line packages; for chip carrier pins, see Figure 3(a).

2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviation is used:-

$I_{OS/2}$ - One half of the true output short circuit current.

I_{CCZ} - Supply current, outputs disabled.

4. REQUIREMENTS

4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein shall be as stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

4.2 DEVIATIONS FROM GENERIC SPECIFICATION

4.2.1 Deviations from Special In-process Controls

None.

4.2.2 Deviations from Final Production Tests (Chart II)

None.

4.2.3 Deviations from Burn-in Tests (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" tests and subsequent electrical measurements related to this test shall be omitted.

(b) Para. 9.9.2, "Electrical Measurements at High and Low Temperatures": Only a test result summary, based on go-no-go tests and presented in histogram form is required.

4.2.4 Deviations from Qualification Tests (Chart IV)

(a) None.

4.2.5 Deviations from Lot Acceptance Tests (Chart V)

(a) None.

4.3 MECHANICAL REQUIREMENTS

4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 1.2 grammes for the flat package, 0.8 grammes for the chip carrier package and 5.0 grammes for the dual-in-line package.

4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

4.4.1 Case

The case shall be hermetically sealed and have a metal body with hard glass seals or a ceramic body and the lids shall be welded, brazed, preform-soldered or glass frit-sealed.

4.4.2 Lead Material and Finish

For dual-in-line and flat packages, the material shall be Type 'G' with Type '4' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For chip carrier packages the finish shall be either Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

4.5 MARKING

4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

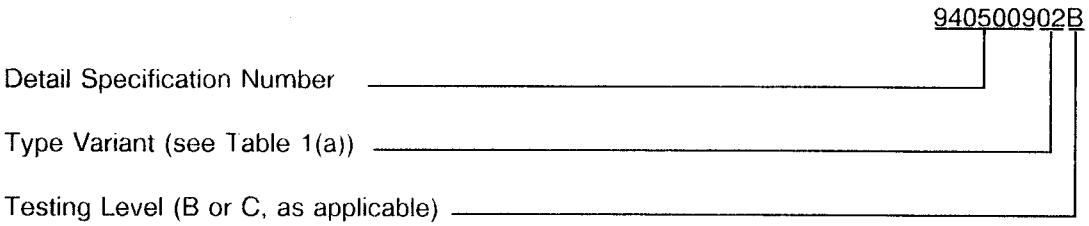
(c) Traceability Information.

4.5.2 Lead Identification

For dual-in-line and flat packages, an index shall be located at the top of the package in the position defined in Note 1 to Figure 2 or, alternatively, a tab may be used to identify Pin No. 1. The pin numbering must be read with the index or tab on the left-hand side. For chip carrier packages, the index shall be as defined by Figure 2 (b).

4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:



4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

4.6 ELECTRICAL MEASUREMENTS

4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

4.7 BURN-IN TESTS

4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values (Δ) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

4.7.2 Conditions for Power Burn-in

The requirements for power burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for power burn-in shall be as specified in Table 5 of this specification.

4.7.3 Electrical Circuits for Power Burn-in

Circuits for use in performing the power burn-in tests are shown in Figure 5 of this specification.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	3(b)	Verify Truth Table with Load. Note 1	-	-	-
2 to 23	Input Current High Level 1	I_{IH1}	3010	4(a)	V_{CC} = 5.5V, V_{IN} = 2.7V Note 2 (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20-21-22-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24-25-26-27)	-	20	µA
24 to 29	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	3010	4(a)	V_{CC} = 5.5V, V_{IN} = 7.0V (Pins D/F 1-2-3-21-22-23) (Pins C 2-3-4-25-26-27)	-	100	µA
30 to 45	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	3010	4(a)	V_{CC} = 5.5V, V_{IN} = 5.5V Note 2 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24)	-	100	µA
46 to 67	Input Clamp Voltage	V_{IC}	3008	4(b)	V_{CC} = 4.5V, I_{IN} = – 18mA Note 3 (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20-21-22-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24-25-26-27)	-	– 1.2	V
68 to 89	Input Current Low Level	I_{IL}	3009	4(c)	V_{CC} = 5.5V, V_{IL} = 0.4V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20-21-22-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24-25-26-27)	-	– 200	µA

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
90 to 105	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OL} = 12mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	-	0.4	V
106 to 121	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = – 3mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	2.4	-	V
122 to 137	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = – 12mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	2.0	-	V
138 to 153	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = – 0.4mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	2.5	-	V
154 to 169	Output Voltage High Level 4	V_{OH4}	3006	4(e)	V_{CC} = 5.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = – 0.4mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	3.5	-	V

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
170 to 185	One Half of the True Output Short Circuit Current	$I_{OS/2}$	3011	4(f)	V_{CC} = 5.5V, V_{OUT} = 2.25V Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	- 30	- 112	mA
186	Supply Current Outputs High	I_{CCH}	3005	4(g)	V_{CC} = 5.5V Note 5 (Pin D/F 24) (Pin C 28)	-	76	mA
187	Supply Current Outputs Low	I_{CCL}	3005	4(g)	V_{CC} = 5.5V Note 5 (Pin D/F 24) (Pin C 28)	-	88	mA
188	Supply Current Outputs Disabled	I_{CCZ}	3005	4(g)	V_{CC} = 5.5V Note 5 (Pin D/F 24) (Pin C 28)	-	88	mA

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 6)	LIMITS MIN	LIMITS MAX	UNIT
189 to 220	Propagation Delay Low to High, from CAB to B or CBA to A	t_{PLH1}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 1 to 13 23 to 4 — 2 to 16 27 to 5 1 to 14 23 to 5 — 2 to 17 27 to 6 1 to 15 23 to 6 — 2 to 18 27 to 7 1 to 16 23 to 7 — 2 to 19 27 to 9 1 to 17 23 to 8 — 2 to 20 27 to 10 1 to 18 23 to 9 — 2 to 21 27 to 11 1 to 19 23 to 10 — 2 to 23 27 to 12 1 to 20 23 to 11 — 2 to 24 27 to 13	-	30	ns
221 to 252	Propagation Delay High to Low, from CAB to B or CBA to A	t_{PHL1}	3003	4(i)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 1 to 13 23 to 4 — 2 to 16 27 to 5 1 to 14 23 to 5 — 2 to 17 27 to 6 1 to 15 23 to 6 — 2 to 18 27 to 7 1 to 16 23 to 7 — 2 to 19 27 to 9 1 to 17 23 to 8 — 2 to 20 27 to 10 1 to 18 23 to 9 — 2 to 21 27 to 11 1 to 19 23 to 10 — 2 to 23 27 to 12 1 to 20 23 to 11 — 2 to 24 27 to 13	-	17	ns
253 to 284	Propagation Delay Low to High, from A to B or B to A	t_{PLH2}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 4 to 20 20 to 4 — 5 to 24 24 to 5 5 to 1919 to 5 — 6 to 23 23 to 6 6 to 18 18 to 6 — 7 to 21 21 to 7 7 to 17 17 to 7 — 9 to 20 20 to 9 8 to 16 16 to 8 — 10 to 19 19 to 10 9 to 15 15 to 9 — 11 to 18 18 to 11 10 to14 14 to 10 — 12 to 17 17 to 12 11 to13 13 to 11 — 13 to 16 16 to 13	-	20	ns
285 to 316	Propagation Delay High to Low, from A to B or B to A	t_{PHL2}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 4 to 20 20 to 4 — 5 to 24 24 to 5 5 to 1919 to 5 — 6 to 23 23 to 6 6 to 18 18 to 6 — 7 to 21 21 to 7 7 to 17 17 to 7 — 9 to 20 20 to 9 8 to 16 16 to 8 — 10 to 19 19 to 10 9 to 15 15 to 9 — 11 to 18 18 to 11 10 to14 14 to 10 — 12 to 17 17 to 12 11 to13 13 to 11 — 13 to 16 16 to 13	-	12	ns

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 6)	LIMITS MIN	LIMITS MAX	UNIT
317 to 348	Propagation Delay Low to High, from SAB to B or SBA to A with A or B Low	t_{PLH3}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 7 Pins D/F — Pins C 2 to 13 22 to 4 — 3 to 16 26 to 5 2 to 14 22 to 5 — 3 to 17 26 to 6 2 to 15 22 to 6 — 3 to 18 26 to 7 2 to 16 22 to 7 — 3 to 19 26 to 9 2 to 17 22 to 8 — 3 to 20 26 to 10 2 to 18 22 to 9 — 3 to 21 26 to 11 2 to 19 22 to 10 — 3 to 23 26 to 12 2 to 20 22 to 11 — 3 to 24 26 to 13	-	35	ns
349 to 380	Propagation Delay High to Low, from SAB to B or SBA to A with A or B Low	t_{PHL3}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 7 Pins D/F — Pins C 2 to 13 22 to 4 — 3 to 16 26 to 5 2 to 14 22 to 5 — 3 to 17 26 to 6 2 to 15 22 to 6 — 3 to 18 26 to 7 2 to 16 22 to 7 — 3 to 19 26 to 9 2 to 17 22 to 8 — 3 to 20 26 to 10 2 to 18 22 to 9 — 3 to 21 26 to 11 2 to 19 22 to 10 — 3 to 23 26 to 12 2 to 20 22 to 11 — 3 to 24 26 to 13	-	20	ns
381 to 412	Propagation Delay Low to High, from SAB to B or SBA to A with A or B High	t_{PLH4}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 7 Pins D/F — Pins C 2 to 13 22 to 4 — 3 to 16 26 to 5 2 to 14 22 to 5 — 3 to 17 26 to 6 2 to 15 22 to 6 — 3 to 18 26 to 7 2 to 16 22 to 7 — 3 to 19 26 to 9 2 to 17 22 to 8 — 3 to 20 26 to 10 2 to 18 22 to 9 — 3 to 21 26 to 11 2 to 19 22 to 10 — 3 to 23 26 to 12 2 to 20 22 to 11 — 3 to 24 26 to 13	-	25	ns

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 6)	LIMITS MIN	LIMITS MAX	UNIT
413 to 444	Propagation Delay High to Low. from SAB to B or SBA to A with A or B High	t_{PHL4}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 7 Pins D/F — Pins C 2 to 13 22 to 4 — 3 to 16 26 to 5 2 to 14 22 to 5 — 3 to 17 26 to 6 2 to 15 22 to 6 — 3 to 18 26 to 7 2 to 16 22 to 7 — 3 to 19 26 to 9 2 to 17 22 to 8 — 3 to 20 26 to 10 2 to 18 22 to 9 — 3 to 21 26 to 11 2 to 19 22 to 10 — 3 to 23 26 to 12 2 to 20 22 to 11 — 3 to 24 26 to 13	-	20	ns
445 to 476	Output Enable Time to High Level, from DIR to A or B	t_{PZH}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 3 to 4 3 to 13 — 4 to 5 4 to 16 3 to 5 3 to 14 — 4 to 6 4 to 17 3 to 6 3 to 15 — 4 to 7 4 to 18 3 to 7 3 to 16 — 4 to 9 4 to 19 3 to 8 3 to 17 — 4 to 10 4 to 20 3 to 9 3 to 18 — 4 to 11 4 to 21 3 to 10 3 to 19 — 4 to 12 4 to 23 3 to 11 3 to 20 — 4 to 13 4 to 24	-	30	ns
477 to 508	Output Enable Time to Low Level, from DIR to A or B	t_{PZL}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 3 to 4 3 to 13 — 4 to 5 4 to 16 3 to 5 3 to 14 — 4 to 6 4 to 17 3 to 6 3 to 15 — 4 to 7 4 to 18 3 to 7 3 to 16 — 4 to 9 4 to 19 3 to 8 3 to 17 — 4 to 10 4 to 20 3 to 9 3 to 18 — 4 to 11 4 to 21 3 to 10 3 to 19 — 4 to 12 4 to 23 3 to 11 3 to 20 — 4 to 13 4 to 24	-	25	ns
509 to 540	Output Disable Time from High Level, from DIR to A or B	t_{PHZ}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 3 to 4 3 to 13 — 4 to 5 4 to 16 3 to 5 3 to 14 — 4 to 6 4 to 17 3 to 6 3 to 15 — 4 to 7 4 to 18 3 to 7 3 to 16 — 4 to 9 4 to 19 3 to 8 3 to 17 — 4 to 10 4 to 20 3 to 9 3 to 18 — 4 to 11 4 to 21 3 to 10 3 to 19 — 4 to 12 4 to 23 3 to 11 3 to 20 — 4 to 13 4 to 24	-	10	ns

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP) (NOTE 6)	LIMITS MIN	LIMITS MAX	UNIT
541 to 572	Output Disable Time from Low Level, from DIR to A or B	t_{PLZ}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 3 to 4 3 to 13 — 4 to 5 4 to 16 3 to 5 3 to 14 — 4 to 6 4 to 17 3 to 6 3 to 15 — 4 to 7 4 to 18 3 to 7 3 to 16 — 4 to 9 4 to 19 3 to 8 3 to 17 — 4 to 10 4 to 20 3 to 9 3 to 18 — 4 to 11 4 to 21 3 to 10 3 to 19 — 4 to 12 4 to 23 3 to 11 3 to 20 — 4 to 13 4 to 24	-	16	ns
573 to 604	Output Enable Time to High Level, from $\overline{G}$ to A or B	t_{PZH}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 21 to 4 21 to 13 — 25 to 5 25 to 16 21 to 5 21 to 14 — 25 to 6 25 to 17 21 to 6 21 to 15 — 25 to 7 25 to 18 21 to 7 21 to 16 — 25 to 9 25 to 19 21 to 8 21 to 17 — 25 to 10 25 to 20 21 to 9 21 to 18 — 25 to 11 25 to 21 21 to10 21 to 19 — 25 to 12 25 to 23 21 to11 21 to 20 — 25 to 13 25 to 24	-	17	ns
605 to 636	Output Enable Time to Low Level, from $\overline{G}$ to A or B	t_{PZL}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Pins D/F — Pins C 21 to 4 21 to 13 — 25 to 5 25 to 16 21 to 5 21 to 14 — 25 to 6 25 to 17 21 to 6 21 to 15 — 25 to 7 25 to 18 21 to 7 21 to 16 — 25 to 9 25 to 19 21 to 8 21 to 17 — 25 to 10 25 to 20 21 to 9 21 to 18 — 25 to 11 25 to 21 21 to10 21 to 19 — 25 to 12 25 to 23 21 to11 21 to 20 — 25 to 13 25 to 24	-	20	ns

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
637 to 668	Output Disable Time from High Level, from $\overline{G}$ to A or B	t_{PHZ}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 6 Pins D/F Pins C 21 to 4 21 to 13 25 to 5 25 to 16 21 to 5 21 to 14 25 to 6 25 to 17 21 to 6 21 to 15 25 to 7 25 to 18 21 to 7 21 to 16 25 to 9 25 to 19 21 to 8 21 to 17 25 to 10 25 to 20 21 to 9 21 to 18 25 to 11 25 to 21 21 to10 21 to 19 25 to 12 25 to 23 21 to11 21 to 20 25 to 13 25 to 24	-	10	ns
669 to 700	Output Disable Time from Low Level, from $\overline{G}$ to A or B	t_{PLZ}	3003	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 6 Pins D/F Pins C 21 to 4 21 to 13 25 to 5 25 to 16 21 to 5 21 to 14 25 to 6 25 to 17 21 to 6 21 to 15 25 to 7 25 to 18 21 to 7 21 to 16 25 to 9 25 to 19 21 to 8 21 to 17 25 to 10 25 to 20 21 to 9 21 to 18 25 to 11 25 to 21 21 to10 21 to 19 25 to 12 25 to 23 21 to11 21 to 20 25 to 13 25 to 24	-	16	ns
701 to 708	Maximum Clock Frequency	f_{max}	-	4(h)	V_{CC} = 4.5 and 5.5V C_L = 50pF, $R_1 = R_2$ = 500Ω Note 8 (Pins D/F 4-11-13-20) (Pins C 5-13-16-24)	35	-	MHz

NOTES: See Page 25.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)

NOTES

1. Go-no-go test with V_{IL} = 0.3V, V_{IH} = 3.0V, trip point 1.5V.
2. For I/O Ports, the parameters I_{IH} and I_{IL} include the off-state output current (I_{OZL}, I_{OZH}).
3. All inputs and outputs not under test shall be open.
4. No more than 1 output should be tested at a time.
5. For I_{CCH}: DIR, $\overline{G}$ and SBA Grounded, all other inputs at 4.5V.

   For I_{CCL}: SAB and $\overline{G}$ Grounded, CAB, DIR, SBA and CBA at 4.5V.

   For I_{CCZ}: $\overline{G}$ Grounded.
6. This parameter shall be tested as a go-no-go on 100% basis. Read-and-record measurements shall be performed on an LTPD7 sample basis following Chart III Burn-in Test.
7. Parameters are measured with the internal output state of the storage register opposite to that of the bus input.
8. This parameter shall be tested as go-no-go on 100% basis.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-5) °C AND -55(+5-0) °C

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
1	Functional Test	-	-	3(b)	Verify Truth Table with Load. Note 1	-	-	-
2 to 23	Input Current High Level 1	I_{IH1}	3010	4(a)	V_{CC} = 5.5V, V_{IN} = 2.7V Note 2 (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20-21-22-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24-25-26-27)	-	20	µA
24 to 29	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	3010	4(a)	V_{CC} = 5.5V, V_{IN} = 7.0V (Pins D/F 1-2-3-21-22-23) (Pins C 2-3-4-25-26-27)	-	100	µA
30 to 45	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	3010	4(a)	V_{CC} = 5.5V, V_{IN} = 5.5V Note 2 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24)	-	100	µA
46 to 67	Input Clamp Voltage	V_{IC}	3008	4(b)	V_{CC} = 4.5V, I_{IN} = - 18mA Note 3 (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20-21-22-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24-25-26-27)	-	- 1.2	V
68 to 89	Input Current Low Level	I_{IL}	3009	4(c)	V_{CC} = 5.5V, V_{IL} = 0.4V (Pins D/F 1-2-3-4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20-21-22-23) (Pins C 2-3-4-5-6-7-9-10-11-12-13-16-17-18-19-20-21-23-24-25-26-27)	-	- 200	µA

NOTES: See Page 25.

TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-5) °C AND -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
90 to 105	Output Voltage Low Level	V_{OL}	3007	4(d)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OL} = 12mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	-	0.4	V
106 to 121	Output Voltage High Level 1	V_{OH1}	3006	4(e)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = -3mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	2.4	-	V
122 to 137	Output Voltage High Level 2	V_{OH2}	3006	4(e)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = -12mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	2.0	-	V
138 to 153	Output Voltage High Level 3	V_{OH3}	3006	4(e)	V_{CC} = 4.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = -0.4mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	2.5	-	V
154 to 169	Output Voltage High Level 4	V_{OH4}	3006	4(e)	V_{CC} = 5.5V, V_{IH} = 2.0V V_{IL} = 0.7V, I_{OH} = -0.4mA (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	3.5	-	V

NOTES: See Page 25.

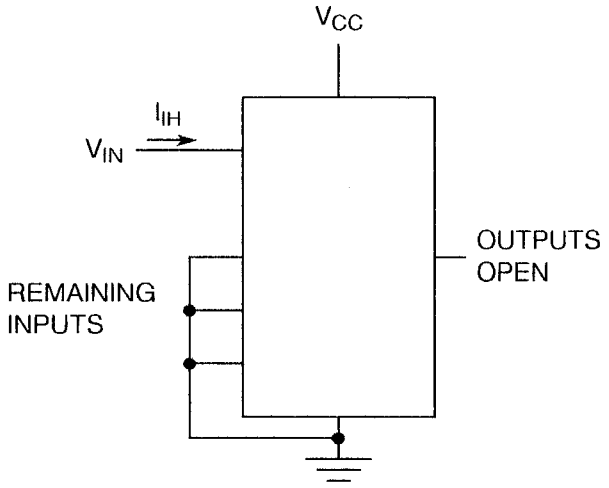
TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES, +125(+0-5) °C AND -55(+5-0) °C (CONT'D)

NO.	CHARACTERISTICS	SYMBOL	TEST METHOD MIL-STD 883	TEST FIG.	TEST CONDITIONS (PINS UNDER TEST D/F = DIP AND FP C = CCP)	LIMITS		UNIT
						MIN	MAX	
170 to 185	One Half of the True Output Short Circuit Current	$I_{OS/2}$	3011	4(f)	V_{CC} = 5.5V, V_{OUT} = 2.25V Note 4 (Pins D/F 4-5-6-7-8-9-10-11-13-14-15-16-17-18-19-20) (Pins C 5-6-7-9-10-11-12-13-16-17-18-19-29-21-23-24)	-30	-112	mA
186	Supply Current Outputs High	I_{CCH}	3005	4(g)	V_{CC} = 5.5V Note 5 (Pin D/F 24) (Pin C 28)	-	76	mA
187	Supply Current Outputs Low	I_{CCL}	3005	4(g)	V_{CC} = 5.5V Note 5 (Pin D/F 24) (Pin C 28)	-	88	mA
188	Supply Current Outputs Disabled	I_{CCZ}	3005	4(g)	V_{CC} = 5.5V Note 5 (Pin D/F 24) (Pin C 28)	-	88	mA

NOTES: See Page 25.

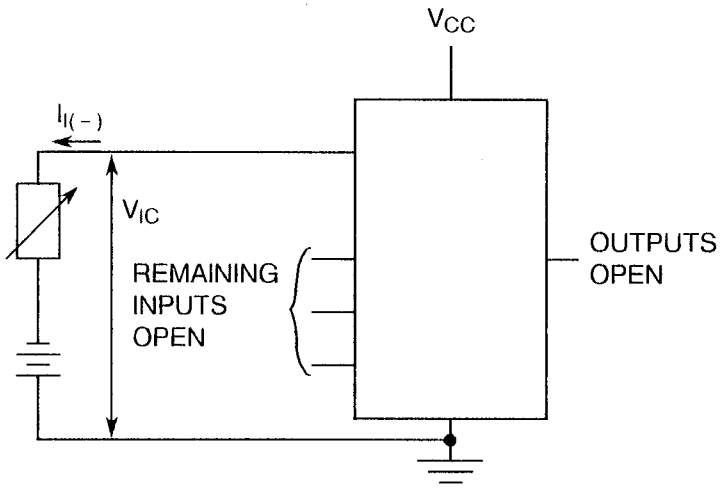
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

FIGURE 4(a) - HIGH LEVEL INPUT CURRENT



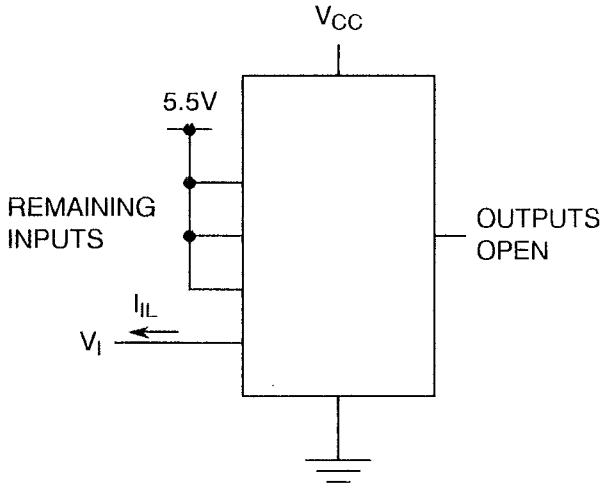
NOTES
1. Each input to be tested separately.

FIGURE 4(b) - INPUT CLAMP VOLTAGE



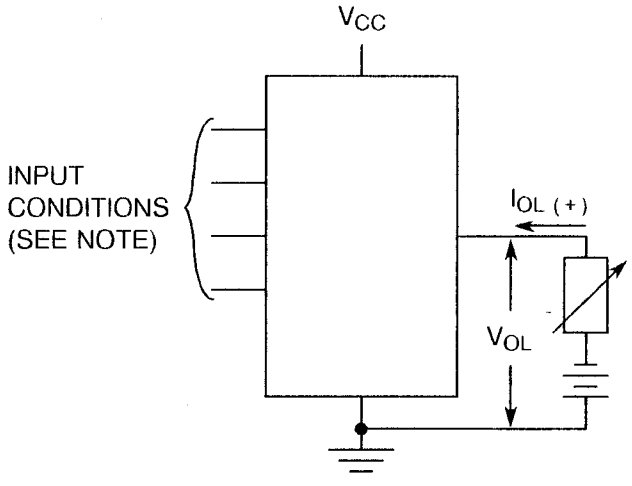
NOTES
1. Each input to be tested separately.

FIGURE 4(c) - LOW LEVEL INPUT CURRENT



NOTES
1. Each input to be tested separately.

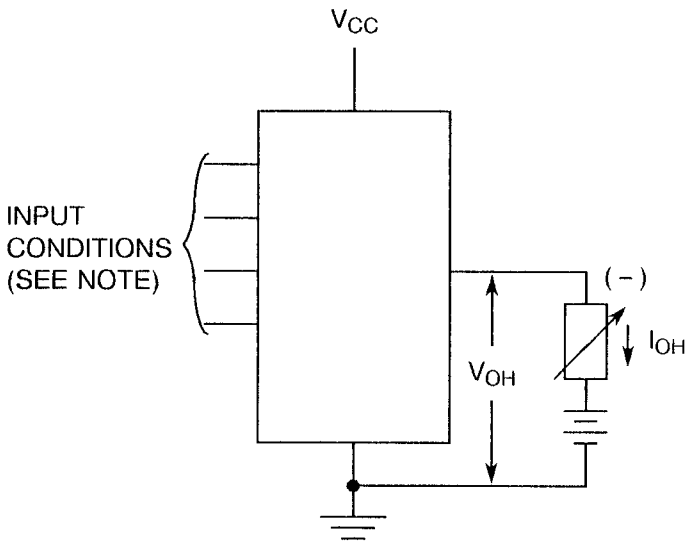
FIGURE 4(d) - LOW LEVEL OUTPUT VOLTAGE



NOTES
1. Inputs as per Truth table to give low level output voltage.

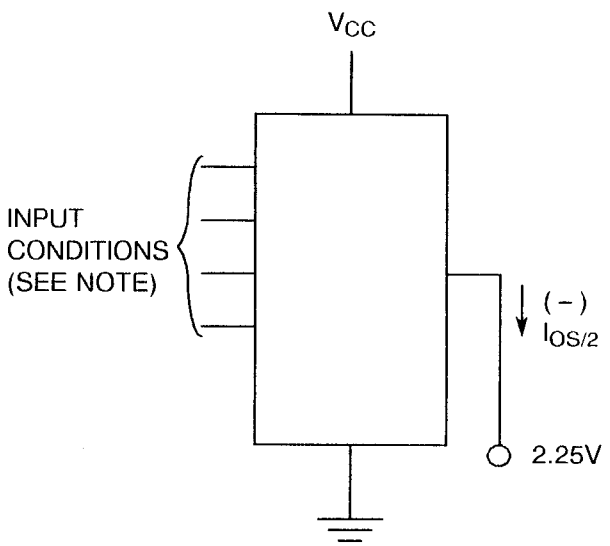
FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(e) - HIGH LEVEL OUTPUT VOLTAGE



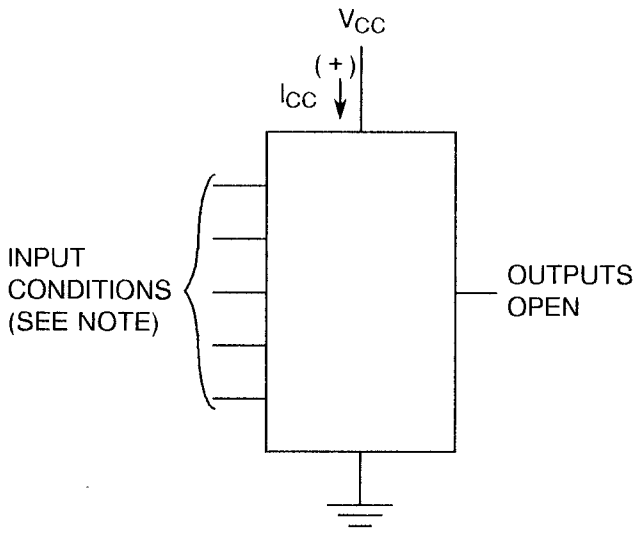
NOTES
1. Inputs as per truth table to give high level output voltage.

FIGURE 4(f) - ONE HALF SHORT CIRCUIT OUTPUT CURRENT



NOTES
1. Inputs as per truth table to give high level output voltage.

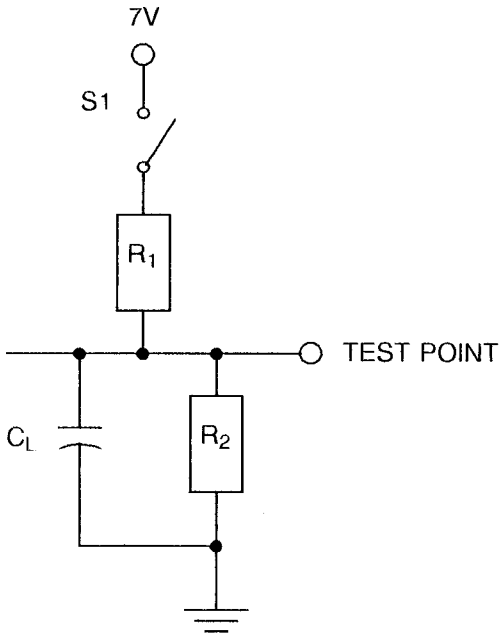
FIGURE 4(g) - SUPPLY CURRENT



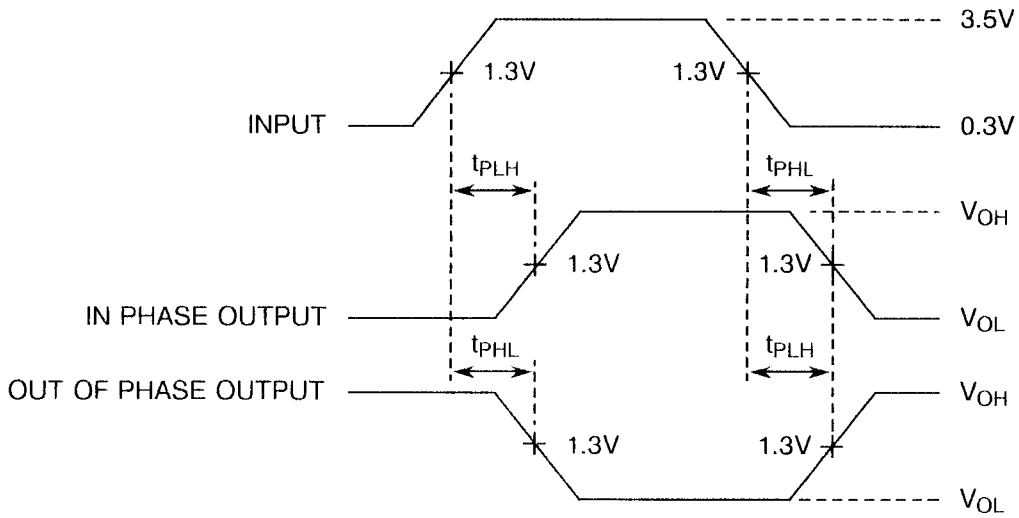
NOTES
1. See Note 5 on Page 25.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(h) - DYNAMIC TEST AND SWITCHING WAVEFORMS



VOLTAGE WAVEFORMS - PROPAGATION DELAY TIMES

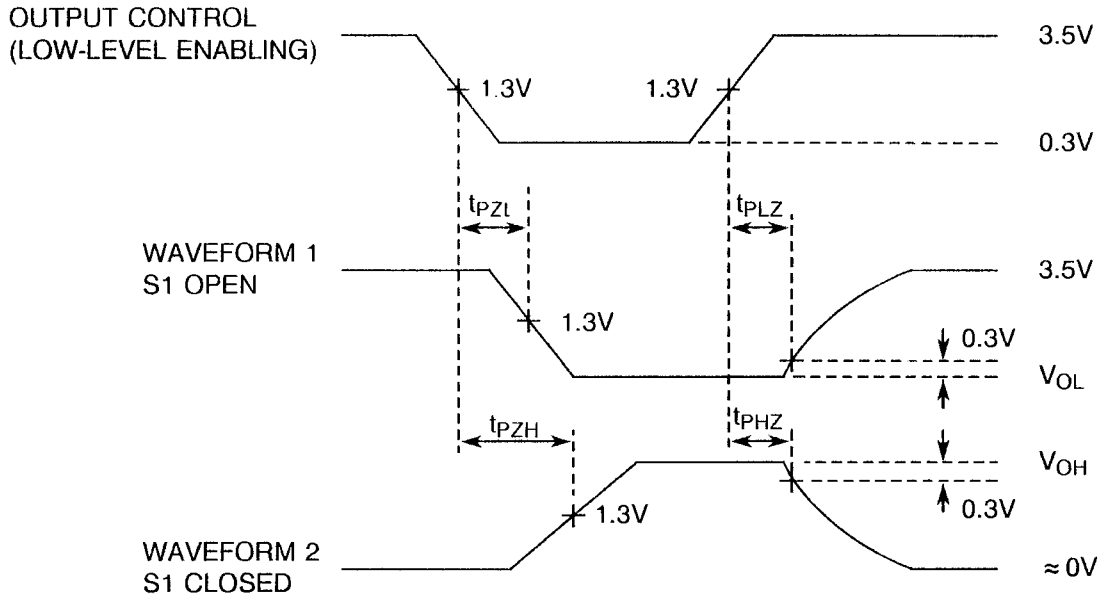


NOTES: See Note 4 on Page 32.

FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(i) - DYNAMIC TEST AND SWITCHING WAVEFORMS (CONTINUED)

VOLTAGE WAVEFORMS - ENABLE AND DISABLE TIMES



NOTE 6

NOTES

1. The generator has the following characteristics: $t_r = t_f = 2ns$, PRR = 1MHz, $Z_{out} = 50\Omega$, Duty Cycle = 50%.
2. $C_L = 50pF \pm 5\%$ including scope probe, wiring and stray capacitance without package in test fixture.
3. $R_1 = R_2 = 500\Omega \pm 5\%$.
4. For measurement of Propagation Times, Switch S1 is open.
5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the Output Control.

   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the Output Control.

TABLE 4 - PARAMETER DRIFT VALUES

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS (Δ)	UNIT
2 to 23	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	±20 or (1) ±0.5	% µA
68 to 89	Input Current Low Level	I_{IL}	As per Table 2	As per Table 2	±10	µA
90 to 105	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±60	mV
106 to 121	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±240	mV
122 to 137	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	±240	mV
138 to 153	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	±240	mV
154 to 169	Output Voltage High Level 4	V_{OH4}	As per Table 2	As per Table 2	±240	mV

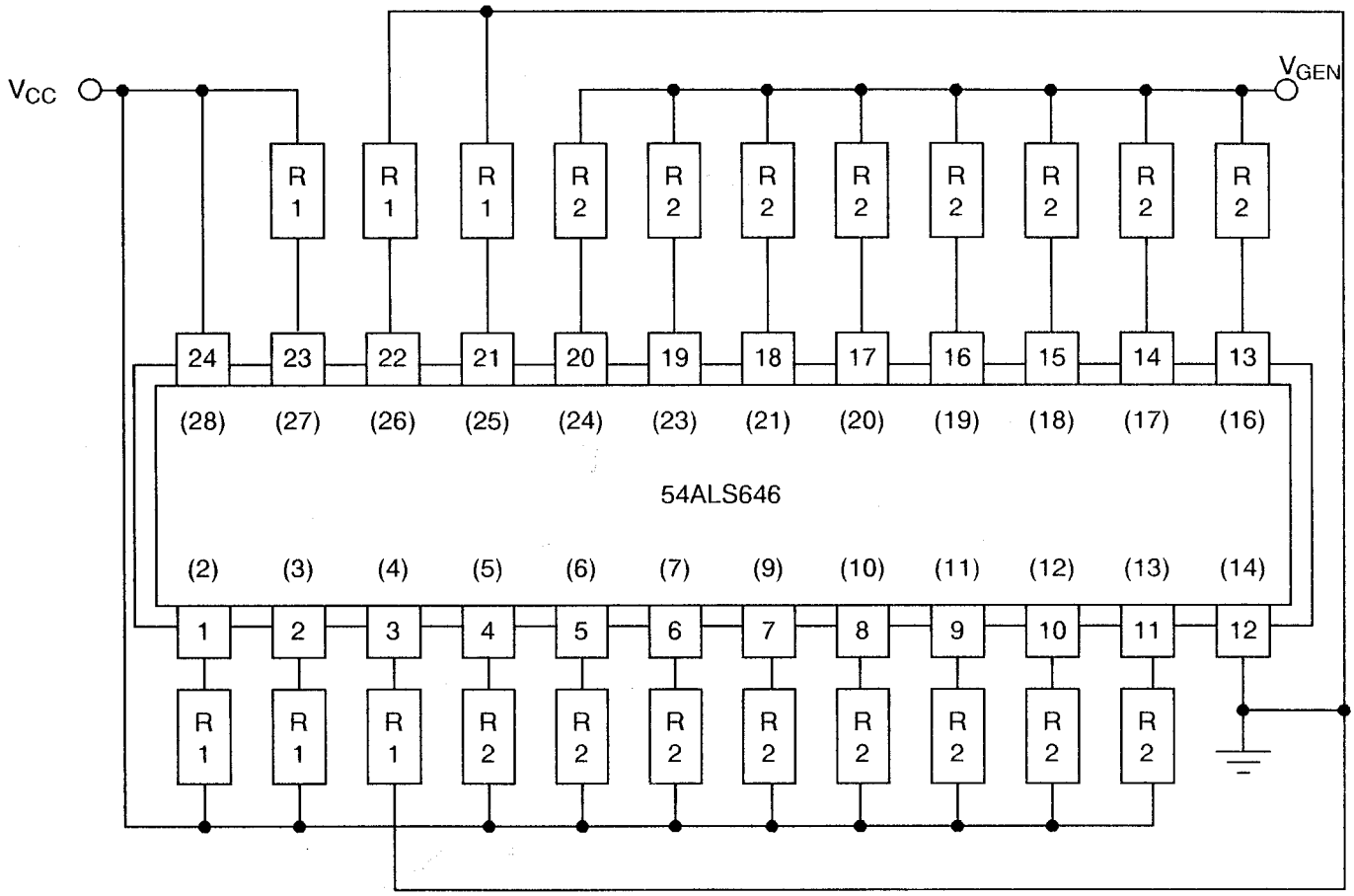
NOTES 1. Whichever is greater referred to the initial value.

TABLE 5 - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TEST

NO.	CHARACTERISTICS	SYMBOL	CONDITION	UNIT
1	Ambient Temperature	T_{amb}	+125(+0−5)	°C
2	Power Supply Voltage	V_{CC}	+5(+0.5−0)	V
3	Pulse Voltage	V_{GEN}	0.5 max. to 3.0 min.	V
4	Frequency	f	50k (See Note 1)	Hz
5	Fan-out	-	10	-
6	Rise Time	t_r	50 max.	µs
7	Fall Time	t_f	50 max.	µs
8	Duty Cycle	-	20 min.	%

NOTES
1. Tolerance ±10%.

FIGURE 5 - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TEST



NOTES

1. Pin numbers in parenthesis are for the chip carrier package.
2. R_1 = 1.0kΩ ($\frac{1}{4}$W), R_2 = 390Ω ($\frac{1}{4}$W).

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5 of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5 of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The conditions for high temperature storage shall be $T_{amb} = +150(+0\text{-}5)$ °C.

TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTS

NO.	CHARACTERISTICS	SYMBOL	SPEC. AND/OR TEST METHOD	TEST CONDITIONS	CHANGE LIMITS		UNIT
					(Δ)	ABSOLUTE	
2 to 23	Input Current High Level 1	I_{IH1}	As per Table 2	As per Table 2	±1.0	-	µA
24 to 29	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	As per Table 2	As per Table 2	-	100	µA
30 to 45	Input Current High Level 2 (Max. Input Voltage)	I_{IH2}	As per Table 2	As per Table 2	-	100	µA
68 to 89	Input Current Low Level	I_{IL1}	As per Table 2	As per Table 2	±10	-	µA
90 to 105	Output Voltage Low Level	V_{OL}	As per Table 2	As per Table 2	±60	-	mV
106 to 121	Output Voltage High Level 1	V_{OH1}	As per Table 2	As per Table 2	±200	-	mV
122 to 137	Output Voltage High Level 2	V_{OH2}	As per Table 2	As per Table 2	±200	-	mV
138 to 153	Output Voltage High Level 3	V_{OH3}	As per Table 2	As per Table 2	±200	-	mV
154 to 169	Output Voltage High Level 4	V_{OH4}	As per Table 2	As per Table 2	±200	-	mV
186	Supply Current Outputs High	I_{CCH}	As per Table 2	As per Table 2	±20	-	%
187	Supply Current Outputs Low	I_{CCL}	As per Table 2	As per Table 2	±20	-	%
188	Supply Current Outputs Disabled	I_{CCZ}	As per Table 2	As per Table 2	±20	-	%

APPENDIX 'A'

AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

ITEMS AFFECTED	DESCRIPTION OF DEVIATIONS
Para. 4.2.1	Scanning Electron Microscope (SEM) Inspection may be performed using TIF document TIF 3.61.610.001.
Para. 4.2.2	Prior to Die Shear Test TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test, using TIF document TI 50.42-3002.
Para. 4.2.3	Radiographic Inspection may be performed using TIF document TI 50.42-3002.