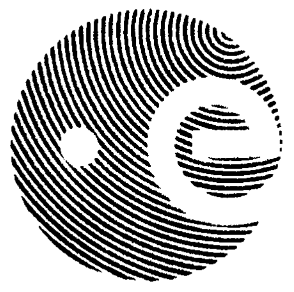

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Pages 1 to 54

# INTEGRATED CIRCUITS, SILICON MONOLITHIC,

# CMOS DIGITAL SIGNAL PROCESSOR

# BASED ON TYPE 320C25

## ESA/SCC Detail Specification No. 9512/001

space components
coordination group

| Issue/Rev. | Date | Approved by | |
|---|---|---|---|
| | | SCCG Chairman | ESA Director General or his Deputy |
| Issue 1 | February 1995 | [signature] | [signature] |
| | | | |
| | | | |
| | | | |

## DOCUMENTATION CHANGE NOTICE

| Rev. Letter | Rev. Date | CHANGE Reference | CHANGE Item | Approved DCR No. |
|---|---|---|---|---|
| | | | | |

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**APPENDICES** (Applicable to specific Manufacturers only)

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# 1. GENERAL

## 1.1 SCOPE

This specification details the ratings, physical and electrical characteristics, test and inspection data for a monolithic, CMOS Silicon Digital Signal Processor, based on Type 320C25. It shall be read in conjunction with ESA/SCC Generic Specification No. 9000, the requirements of which are supplemented herein.

## 1.2 COMPONENT TYPE VARIANTS

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1(a).

## 1.3 MAXIMUM RATINGS

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 1(b).

## 1.4 PARAMETER DERATING INFORMATION (FIGURE 1)

Not applicable.

## 1.5 PHYSICAL DIMENSIONS

As per Figure 2.

## 1.6 PIN ASSIGNMENT

As per Figure 3(a).

## 1.7 TRUTH TABLE

As per Figure 3(b).

## 1.8 CIRCUIT DESCRIPTION

As per Figure 3(c).

## 1.9 FUNCTIONAL DIAGRAM

As per Figure 3(d).

## 1.10 HANDLING PRECAUTIONS

These devices are susceptible to damage by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

These components are categorised as Class 2 with a Minimum Critical Path Failure Voltage of 2000Volts.

## 1.11 INPUT PROTECTION NETWORK

Protection networks shall be incorporated into each input and input/output (I/O) as shown in Figure 3(e).

**TABLE 1(a) - TYPE VARIANTS**

| VARIANT | CASE | FIGURE | LEAD MATERIAL AND/OR FINISH |
|---|---|---|---|
| 01 | Leadless Chip Carrier | 2(a) | 7 |
| 02 | Leadless Chip Carrier | 2(a) | 4 |
| 03 | Leaded Chip Carrier | 2(b) | G7 |
| 04 | Leaded Chip Carrier | 2(b) | G4 |
| 05 | Flat Pack | 2(c) | G7 |
| 06 | Flat Pack | 2(c) | G4 |

**TABLE 1(b) - MAXIMUM RATINGS**

| No. | CHARACTERISTICS | SYMBOL | MAXIMUM RATINGS | UNIT | REMARKS |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $V_{DD}$ | −0.3 to +7.0 | V | Note 1, 2 |
| 2 | Input Voltage | $V_{IN}$ | −0.3 to +7.0 | V | Note 1 |
| 3 | Output Voltage | $V_{OUT}$ | −0.3 to +7.0 | V | Note 1 |
| 4 | DC Output Current | $I_{OUT}$ | 2.0 | mA | |
| 5 | Power Dissipation | $P_D$ | 1.0 | W | |
| 6 | Input Clock Frequency | F | 40 | MHz | |
| 7 | Operating Temperature Range | $T_{op}$ | −55 to +125 | °C | Note 3 |
| 8 | Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C | |
| 9 | Thermal Resistance, Junction-to-Case<br>Variants 01-02<br>Variants 01-02<br>Variants 01-02 | $R_{th(J-C)}$ | <br><br>7.0<br>6.6<br>9.9 | °C/W | |
| 10 | Soldering Temperature | $T_{sol}$ | +265 | °C | Note 4 |

**NOTES**

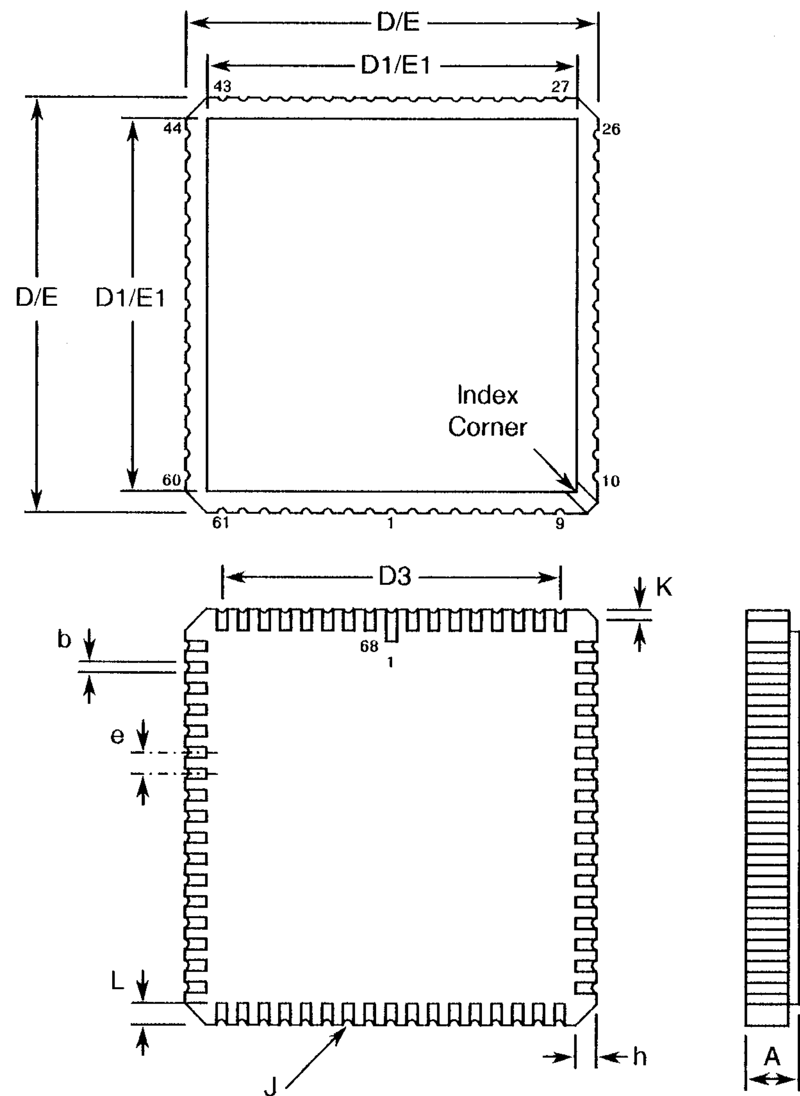
1. All voltage values are with respect to $V_{SS}$.
2. Device operating voltage range is +4.5V to 5.5V.
3. Min is free-air temperature, Max is case temperature
4. Duration 10 seconds maximum and the same terminal shall not be resoldered until 3 minutes have elapsed.

**FIGURE 1 - PARAMETER DERATING INFORMATION**

Not applicable.

## FIGURE 2 - PHYSICAL DIMENSIONS

FIGURE 2(a) - LEADLESS CERAMIC CHIP CARRIER, 68-TERMINALS



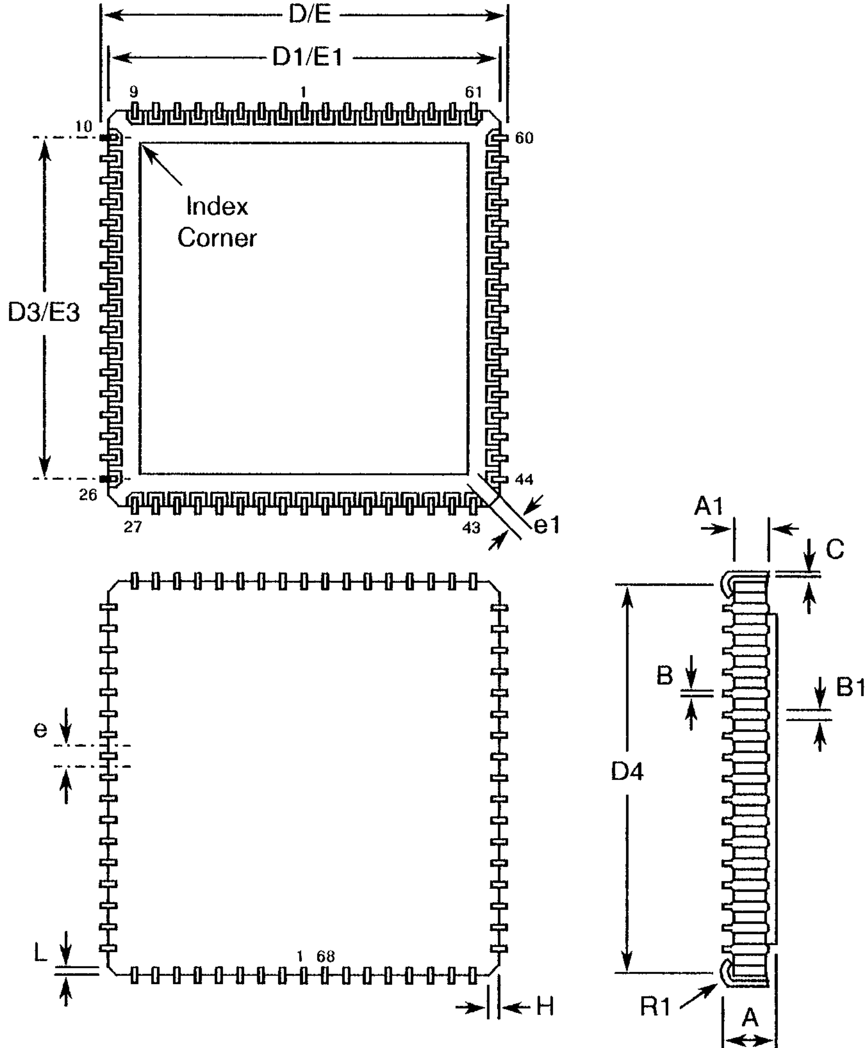

| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A | 2.08 | 3.05 | |
| B | 0.56 | 0.71 | |
| D/E | 23.88 | 24.38 | |
| D1/E1 | - | 21.89 | |
| D3 | 20.07 | 20.57 | |
| e | 1.27 TYPICAL | | 1 |
| H | 0.77 | 1.27 | |
| J | 0.20 TYPICAL | | |
| K | 0.25 | 0.76 | |
| L | 0.14 | 1.40 | |

**NOTES**

1. Contact spacing is 1.27mm between centres. The centre is identified with a half cylindrical.

**FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)**

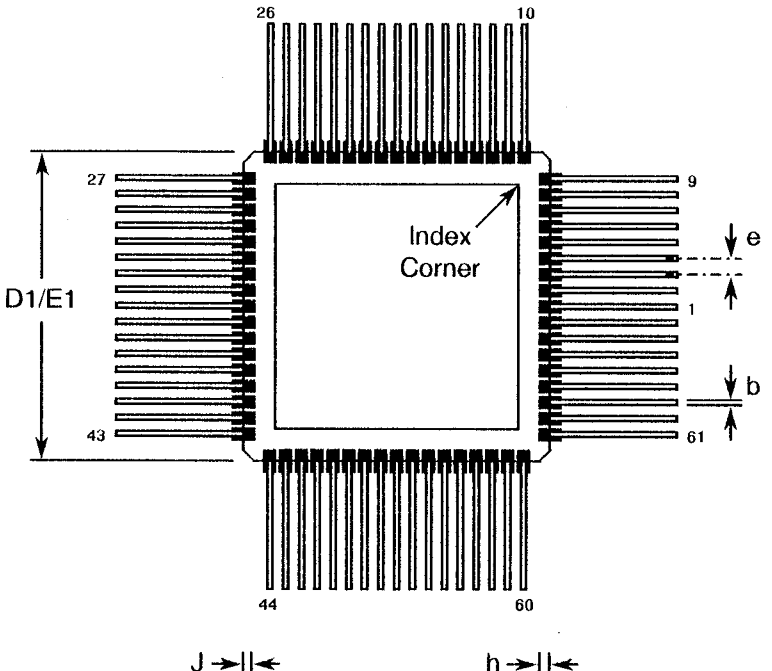
FIGURE 2(b) - J LEADED CERAMIC CHIP CARRIER, 68-TERMINALS

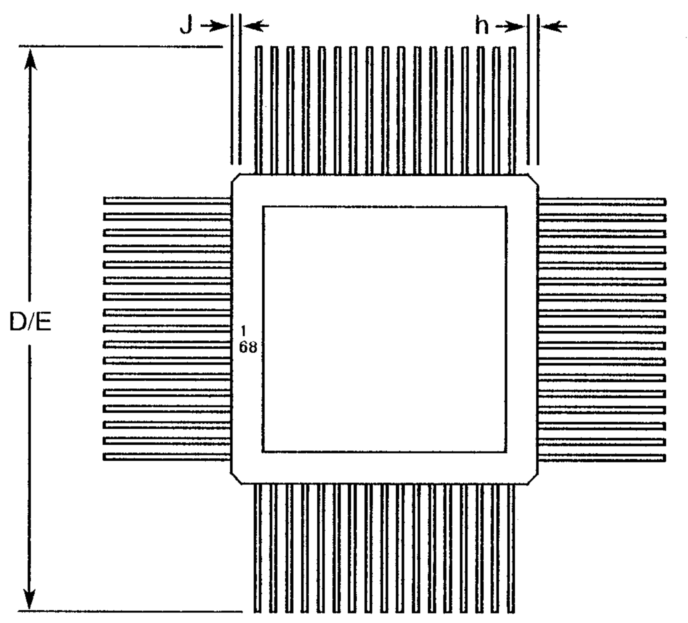


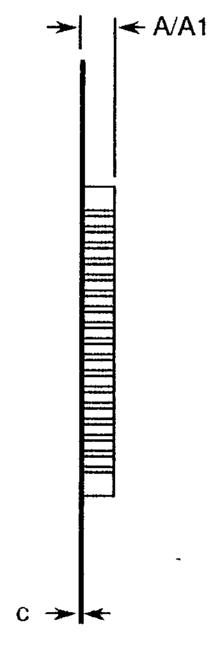

| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A | 2.92 | 3.43 | |
| A1 | 1.91 | 2.41 | |
| B | 0.33 | 0.58 | |
| B1 | 0.51 | 0.81 | |
| C | 0.18 | 0.28 | |
| D/E | 24.89 | 25.40 | |
| D1/E1 | 23.88 | 24.38 | |
| D3/E3 | 20.19 | 20.52 | |
| D4 | 23.11 | 24.13 | |
| e | 1.27 TYPICAL | | |
| e1 | 0.38 | - | |
| H | 0.76 | 1.27 | 3 places |
| J | 0.25 | 0.51 | |
| R1 | 0.64 | 0.89 | |

## FIGURE 2 - PHYSICAL DIMENSIONS (CONTINUED)

FIGURE 2(c) - CERAMIC QUAD FLAT-PACK, 68-TERMINALS

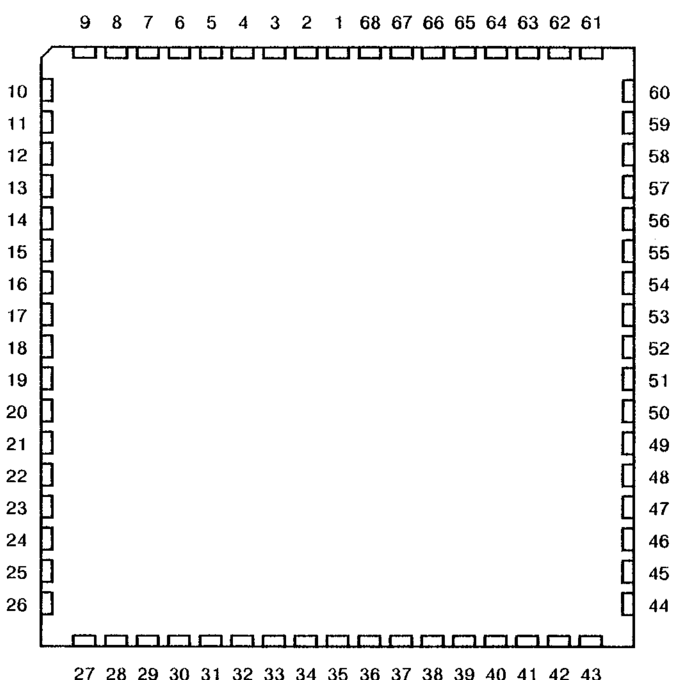



| SYMBOL | MILLIMETRES | | NOTES |
|---|---|---|---|
| | MIN | MAX | |
| A/A1 | 1.98 | 2.38 | |
| b | 0.30 TYPICAL | | |
| c | 0.10 | 0.20 | |
| D/E | 37.59 | 43.18 | |
| D1/E1 | 23.88 | 24.51 | |
| e | 1.27 TYPICAL | | |
| h | 1.01 TYPICAL | | 3 places |
| J | 0.50 TYPICAL | | |

**FIGURE 3(a) - PIN ASSIGNMENT**

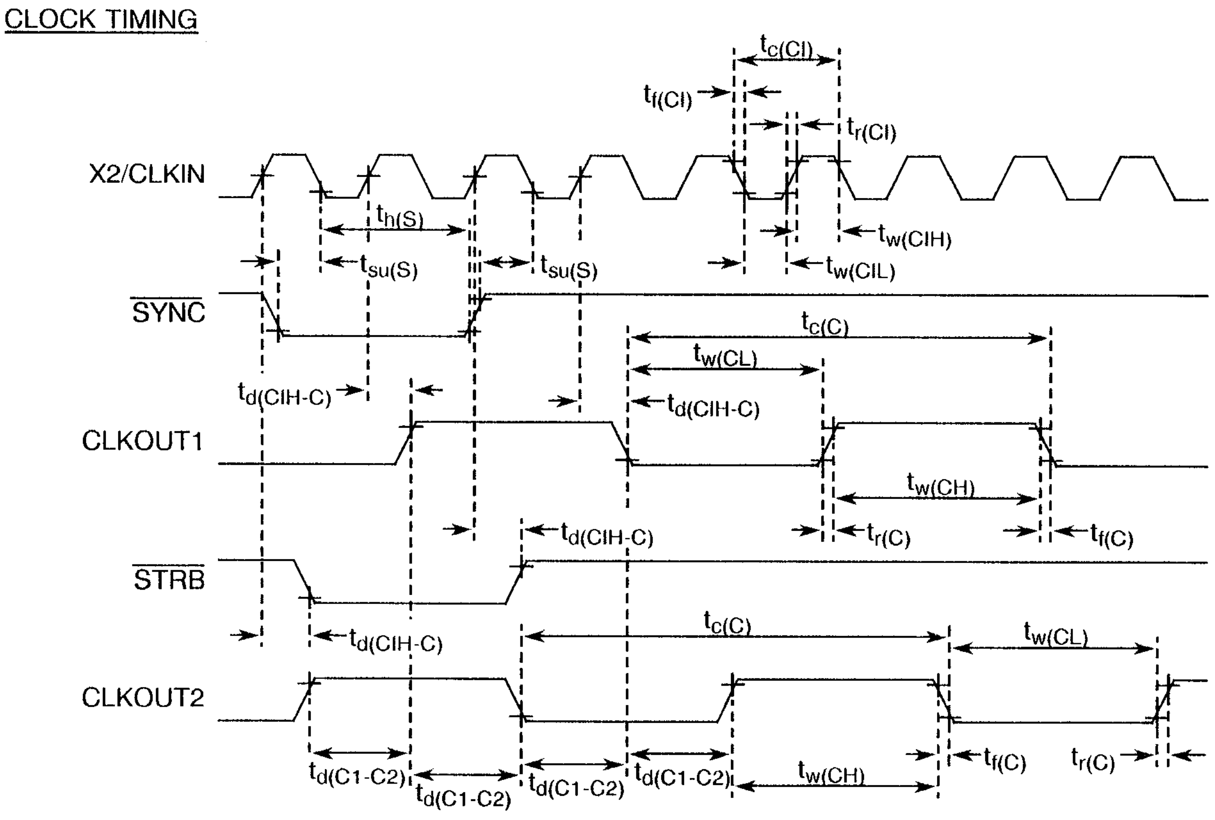



| SYMBOL | PIN No. | SYMBOL | PIN No. | SYMBOL | PIN No. |
|---|---|---|---|---|---|
| MP/$\overline{MC}$ | 1 | DR | 24 | $\overline{PS}$ | 47 |
| D15 | 2 | FSR | 25 | R/$\overline{W}$ | 48 |
| D14 | 3 | A0 | 26 | $\overline{STRB}$ | 49 |
| D13 | 4 | $V_{SS}$ | 27 | $\overline{BR}$ | 50 |
| D12 | 5 | A1 | 28 | X1 | 51 |
| D11 | 6 | A2 | 29 | X2 CLKIN | 52 |
| D10 | 7 | A3 | 30 | FSX | 53 |
| D9 | 8 | A4 | 31 | DX | 54 |
| D8 | 9 | A5 | 32 | $\overline{HOLDA}$ | 55 |
| $V_{SS}$ | 10 | A6 | 33 | XF | 56 |
| D7 | 11 | A7 | 34 | CLKOUT2 | 57 |
| D6 | 12 | $V_{DD}$ | 35 | CLKOUT1 | 58 |
| D5 | 13 | A8 | 36 | $\overline{MSC}$ | 59 |
| D4 | 14 | A9 | 37 | $\overline{IACK}$ | 60 |
| D3 | 15 | A10 | 38 | $V_{DD}$ | 61 |
| D2 | 16 | A11 | 39 | $V_{DD}$ | 62 |
| D1 | 17 | A12 | 40 | CLKX | 63 |
| D0 | 18 | A13 | 41 | CLKR | 64 |
| $\overline{SYNC}$ | 19 | A14 | 42 | RS | 65 |
| $\overline{INT}$0 | 20 | A15 | 43 | READY | 66 |
| $\overline{INT}$1 | 21 | $V_{SS}$ | 44 | $\overline{HOLD}$ | 67 |
| $\overline{INT}$2 | 22 | $\overline{DS}$ | 45 | $\overline{BIO}$ | 68 |
| $V_{DD}$ | 23 | $\overline{IS}$ | 46 | | |

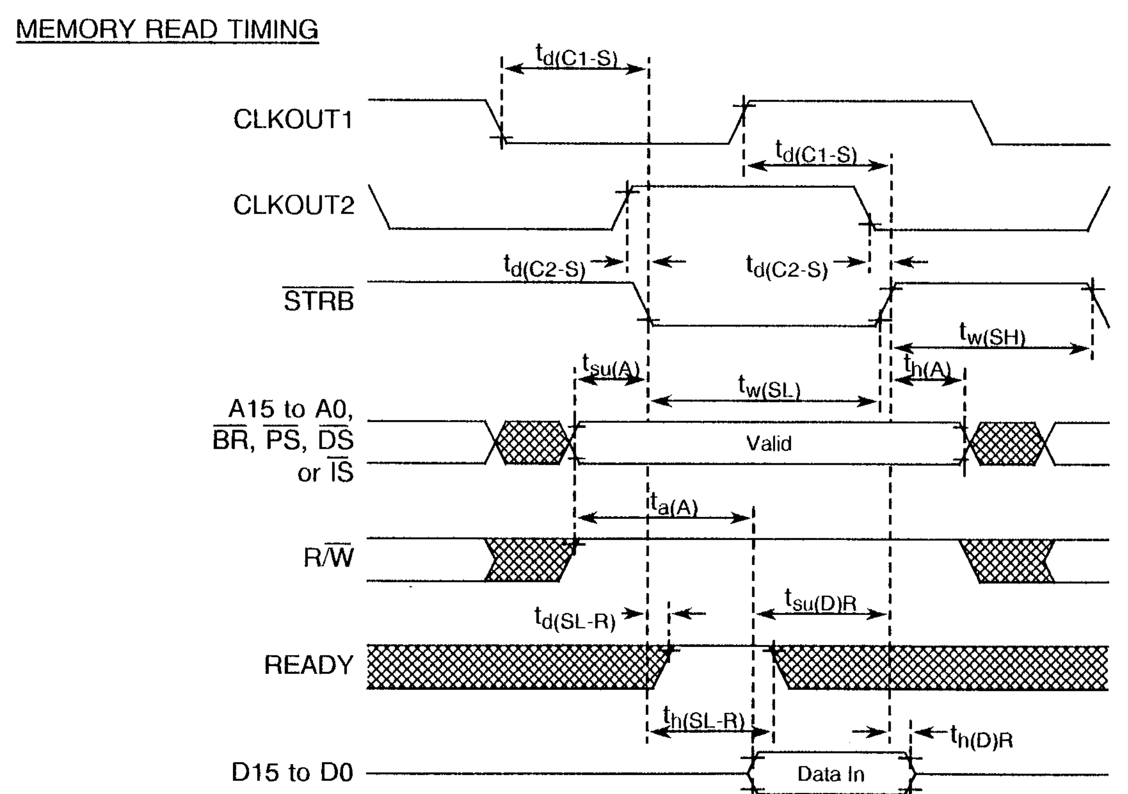
## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET

TIMING DIAGRAMS

CLOCK TIMING



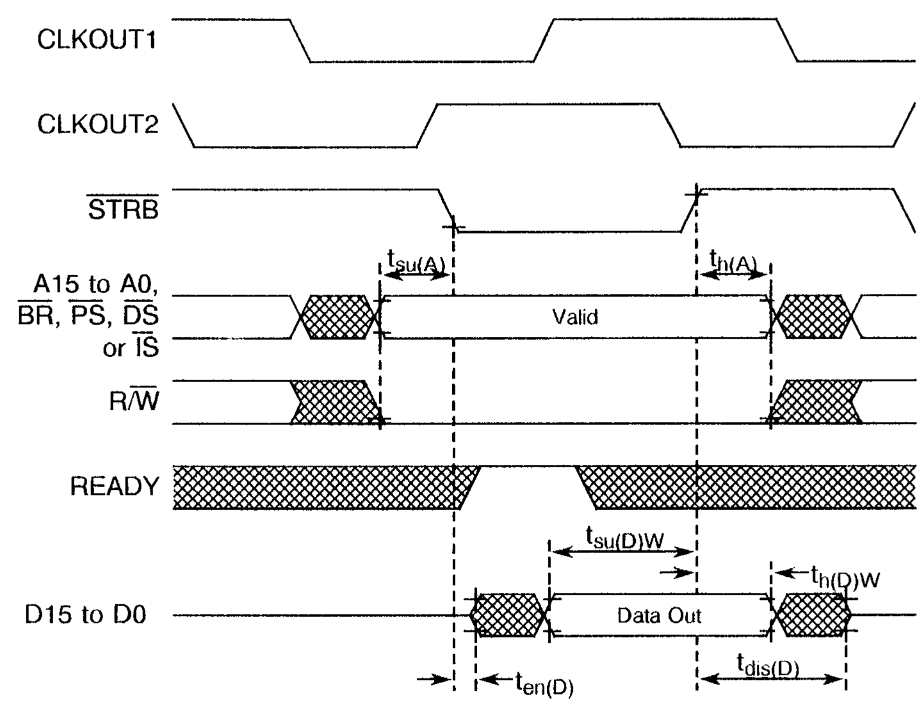

MEMORY READ TIMING



## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

MEMORY WRITE TIMING




ONE WAIT-STATE MEMORY ACCESS TIMING

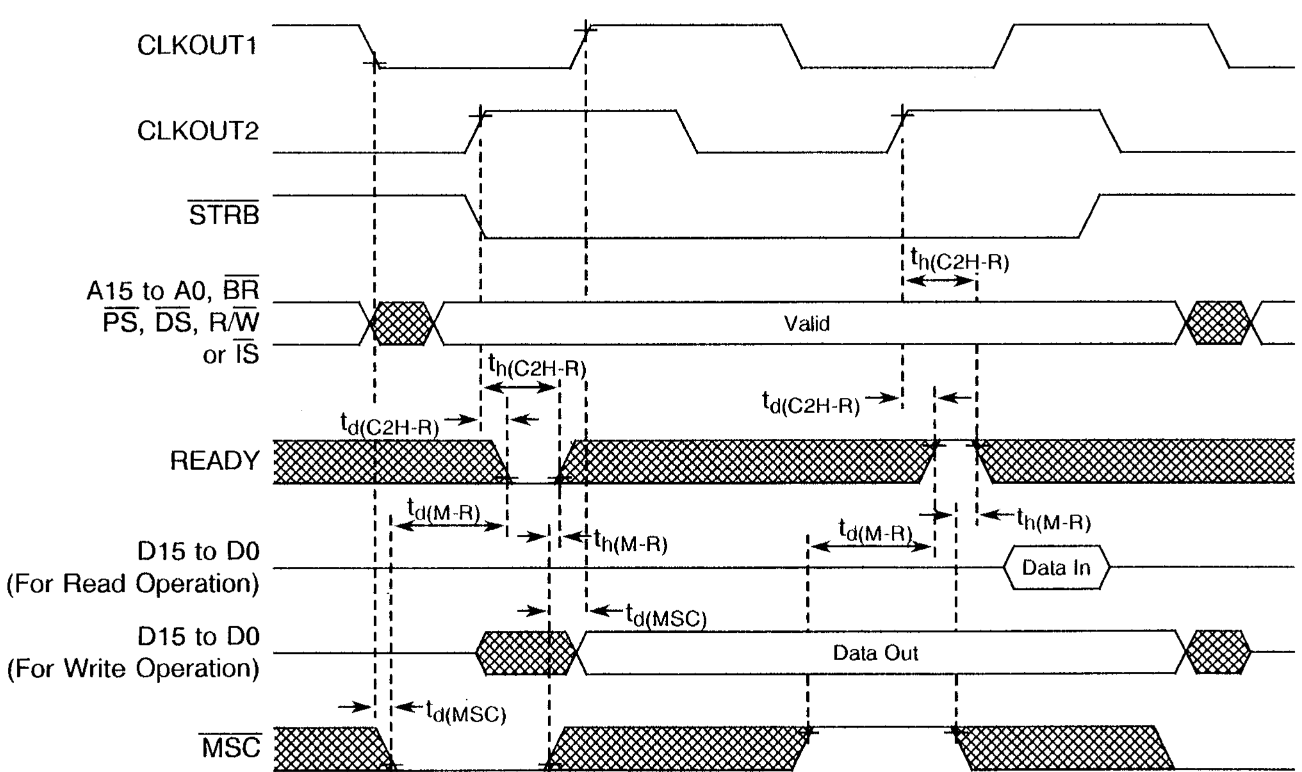
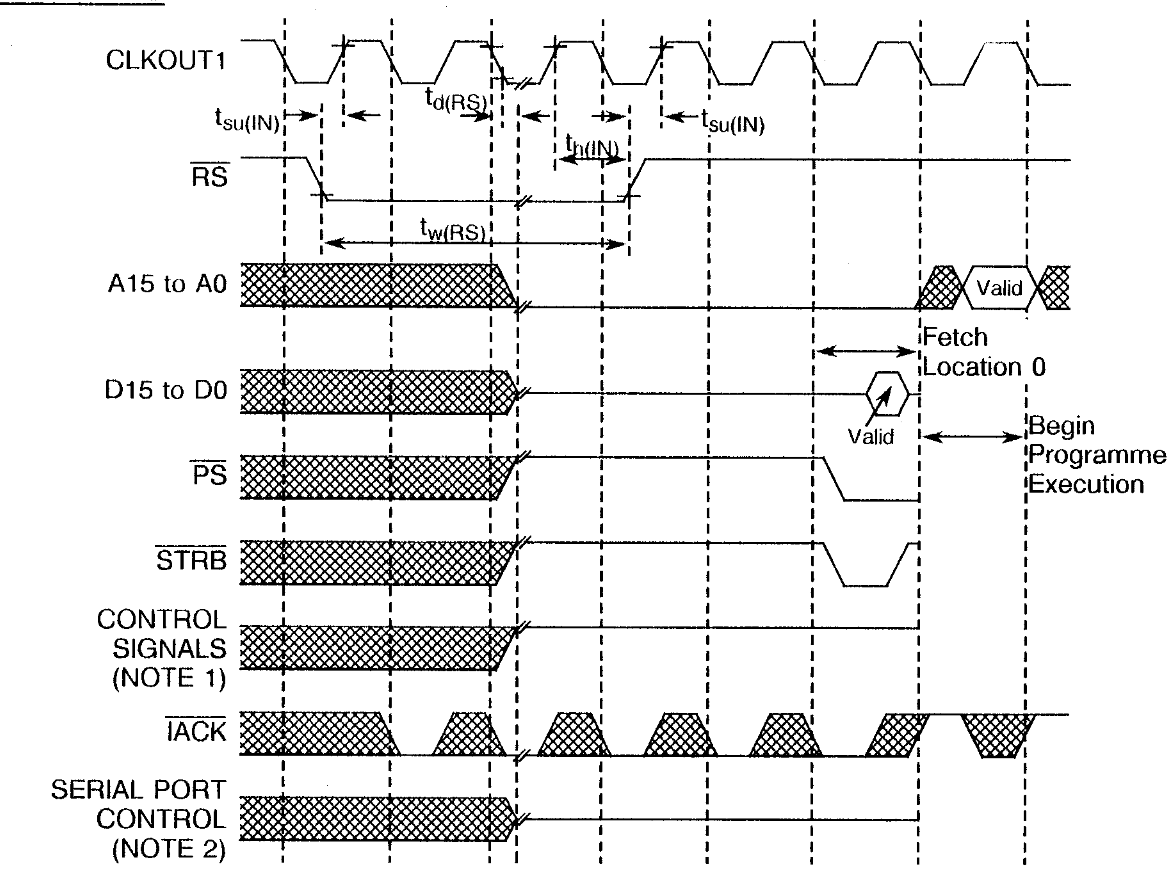


**FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)**

TIMING DIAGRAMS (CONTINUED)

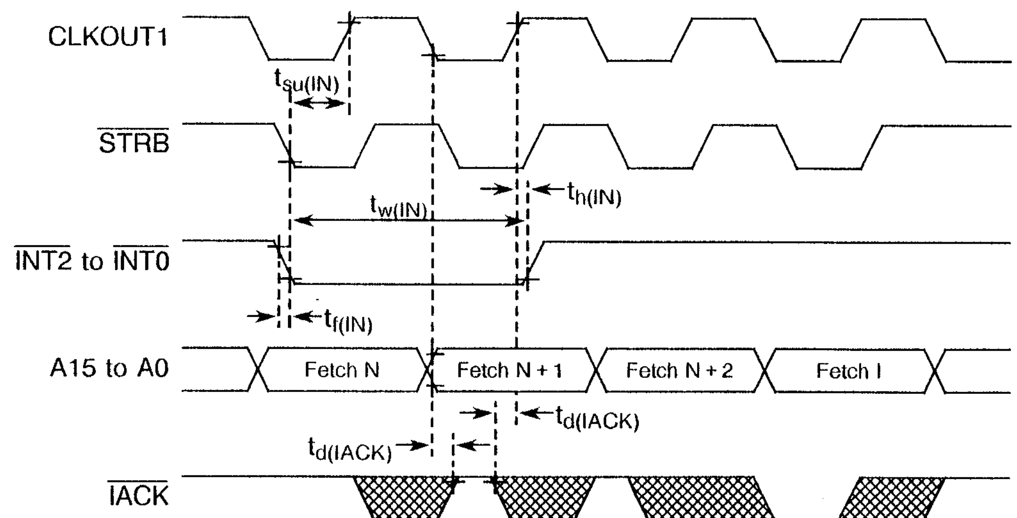
RESET TIMING




**NOTES**

1. Control signals are $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$ and XF.
2. Serial port controls are DX and FSX.

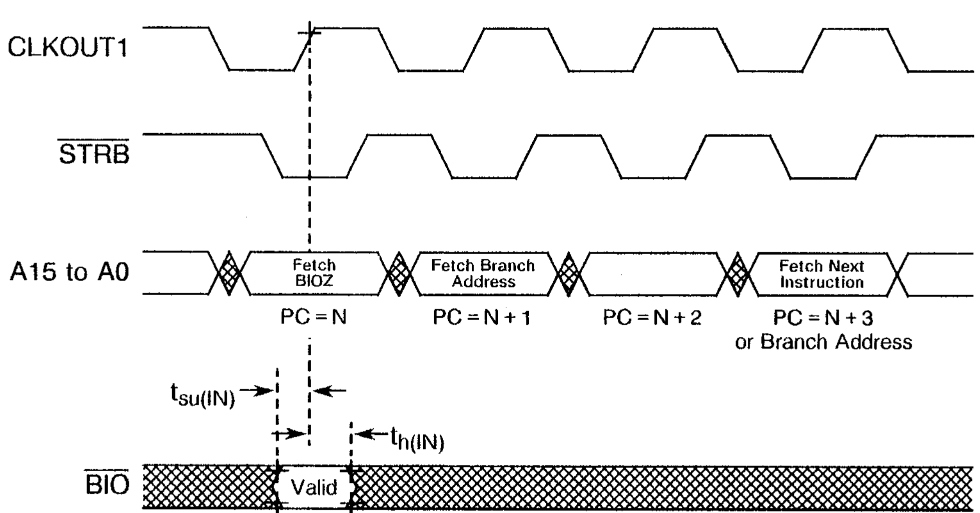
INTERRUPT TIMING



## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

$\overline{BIO}$ TIMING




EXTERNAL FLAG TIMING

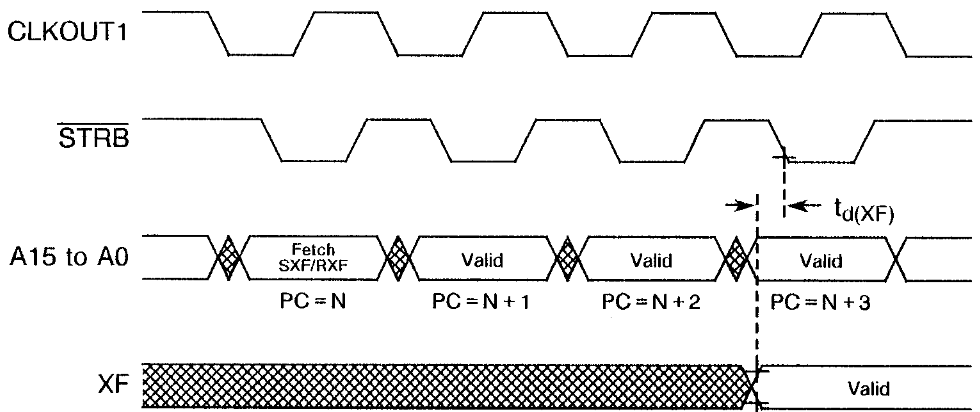
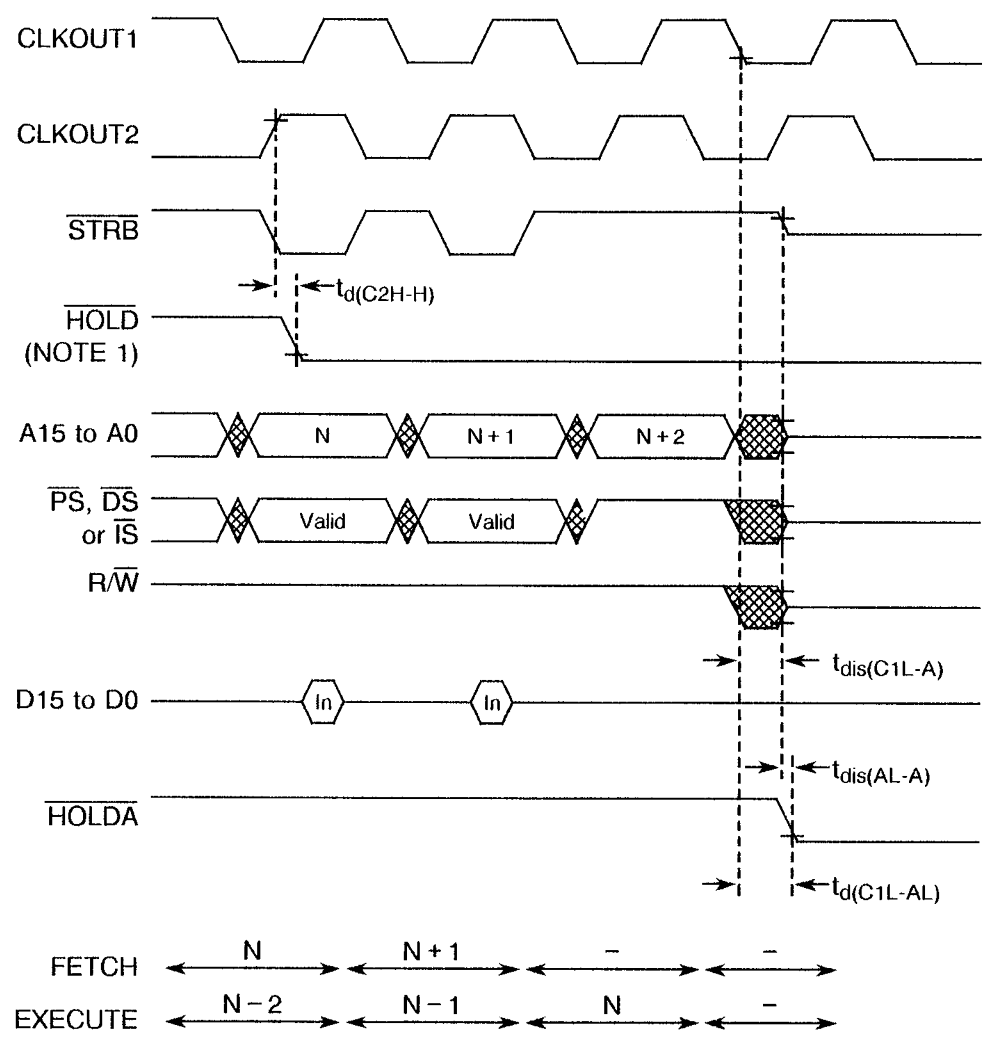


**FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)**

TIMING DIAGRAMS (CONTINUED)

$\overline{\text{HOLD}}$ TIMING (PART A)



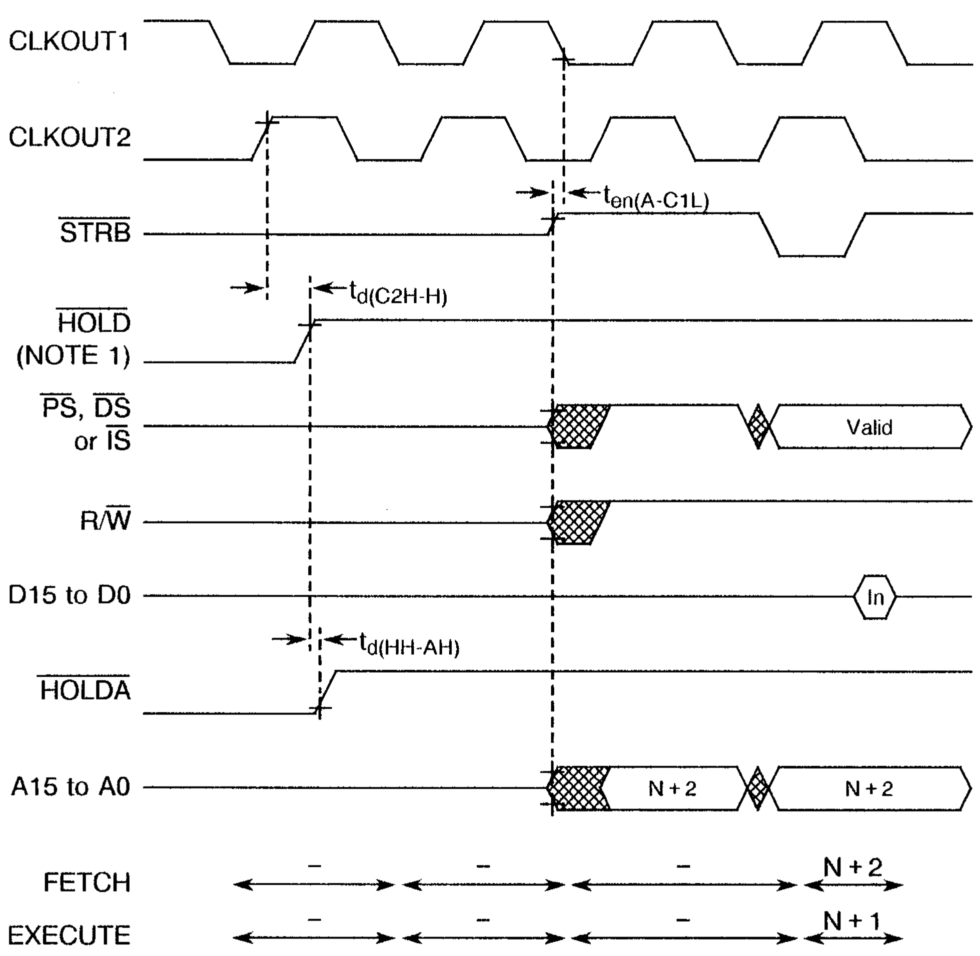

**NOTES**

1. $\overline{\text{HOLD}}$ is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLCKOUT2 cycle will occur.

## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

HOLD TIMING (PART B)



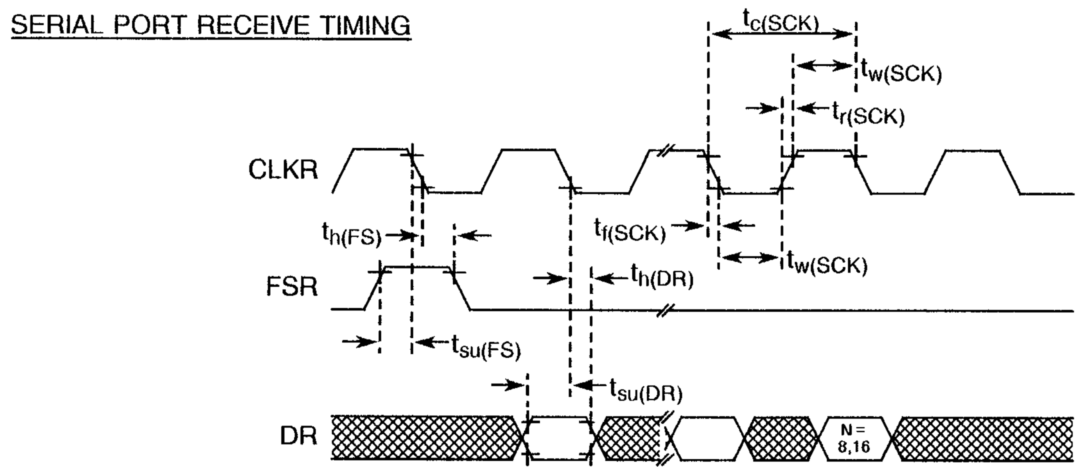

**NOTES**

1. HOLD is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLCKOUT2 cycle will occur.

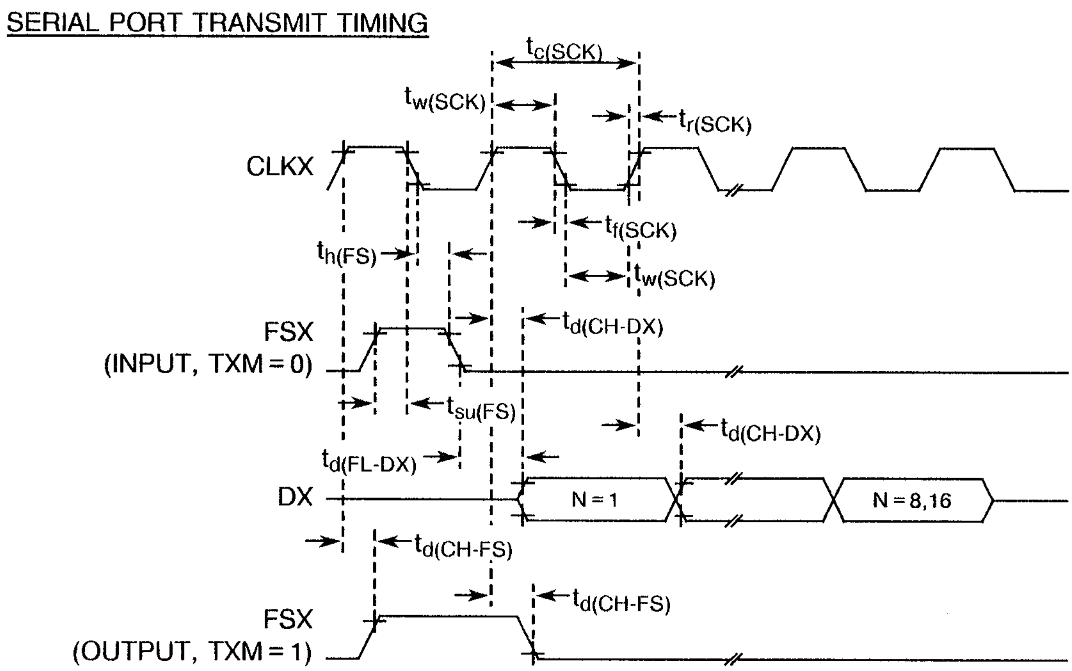
## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

TIMING DIAGRAMS (CONTINUED)

SERIAL PORT RECEIVE TIMING




SERIAL PORT TRANSMIT TIMING



## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

DESCRIPTION OF INSTRUCTIONS

ACCUMULATOR MEMORY REFERENCE

| Mnemonic | Description | Words | 16 Bit OpCode MSB | | | LSB |
|---|---|---|---|---|---|---|
| ABS | Absolute value of accumulator | 1 | 1100 | 1110 | 0001 | 1011 |
| ADD | Add to accumulator with shift | 1 | 0000 | SSSS | IDDD | DDDD |
| ADDC | Add to accumulator with carry | 1 | 0100 | 0011 | IDDD | DDDD |
| ADDH | Add to high accumulator | 1 | 0100 | 1000 | IDDD | DDDD |
| ADDK | Add to accumulator short immediate | 1 | 1100 | 1100 | KKKK | KKKK |
| ADDS | Add to low accumulator with sign-extension suppressed | 1 | 0100 | 1001 | IDDD | DDDD |
| ADDT | Add to accumulator with shift specified by T register | 1 | 0100 | 1010 | IDDD | DDDD |
| ADLK | Add to accumulator long immediate with shift | 2 | 1101 | SSSS | 0000 | 0010 |
| AND | AND with accumulator | 1 | 0100 | 1110 | IDDD | DDDD |
| ANDK | AND immediate with accumulator with shift | 2 | 1101 | SSSS | 0000 | 0100 |
| CMPL | Complement accumulator | 1 | 1100 | 1110 | 0010 | 0111 |
| LAC | Load accumulator with shift | 1 | 0010 | SSSS | IDDD | DDDD |
| LACK | Load accumulator immediate short | 1 | 1100 | 1010 | KKKK | KKKK |
| LACT | Load accumulator with shift specified by T register | 1 | 0100 | 0010 | IDDD | DDDD |
| LALK | Load accumulator long immediate with shift | 2 | 1101 | SSSS | 0000 | 0001 |
| NEG | Negate accumulator | 1 | 1100 | 1110 | 0010 | 0011 |
| NORM | Normalise contents of accumulator | 1 | 1100 | 1110 | 1010 | 0010 |
| OR | OR with accumulator | 1 | 0100 | 1101 | IDDD | DDDD |
| ORK | OR immediate with accumulator with shift | 2 | 1101 | SSSS | 0000 | 0101 |
| ROL | Rotate accumulator left | 1 | 1100 | 1110 | 0010 | 0100 |
| ROR | Rotate accumulator right | 1 | 1100 | 1110 | 0010 | 0101 |
| SACH | Store high accumulator with shift | 1 | 0110 | 1XXX | IDDD | DDDD |
| SACL | Store low accumulator with shift | 1 | 0110 | 0XXX | IDDD | DDDD |
| SBLK | Subtract from accumulator long immediate with shift | 2 | 1101 | SSSS | 0000 | 0011 |
| SFL | Shift accumulator left | 1 | 1100 | 1110 | 0001 | 1000 |
| SFR | Shift accumulator right | 1 | 1100 | 1110 | 0001 | 1001 |
| SUB | Subtract from accumulator with shift | 1 | 0001 | SSSS | IDDD | DDDD |
| SUBB | Subtract from accumulator with borrow | 1 | 0100 | 1111 | IDDD | DDDD |
| SUBC | Conditional subtract | 1 | 0100 | 0111 | IDDD | DDDD |
| SUBH | Subtract from high accumulator | 1 | 0100 | 0111 | IDDD | DDDD |
| SUBK | Subtract from accumulator short immediate | 1 | 1100 | 1101 | KKKK | KKKK |
| SUBS | Subtract from low accumulator with sign extension suppressed | 1 | 0100 | 0101 | IDDD | DDDD |
| SUBT | Subtract from accumulator with shift specified by T register | 1 | 0100 | 0110 | IDDD | DDDD |
| XOR | Exclusive OR with accumulator | 1 | 0100 | 1100 | IDDD | DDDD |
| XORK | Exclusive OR immediate with accumulator with shift | 2 | 1101 | SSSS | 0000 | 0110 |
| ZAC | Zero accumulator | 1 | 1100 | 1010 | 0000 | 0000 |
| ZALH | Zero low accumulator and load high accumulator | 1 | 0100 | 0000 | IDDD | DDDD |
| ZALR | Zero low accumulator and load high accumulator with rounding | 1 | 0111 | 1011 | IDDD | DDDD |
| ZALS | Zero accumulator and load low accumulator with sign extension suppressed | 1 | 0100 | 0001 | IDDD | DDDD |

**NOTES**: For Instruction Symbols, see Page 21.

**FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)**

DESCRIPTION OF INSTRUCTIONS (CONTINUED)

AUXILIARY REGISTERS AND DATA PAGE POINTER

| Mnemonic | Description | Words | 16 Bit OpCode MSB | | | LSB |
|---|---|---|---|---|---|---|
| ADRK | Add to auxiliary register short immediate | 1 | 0111 | 1110 | KKKK | KKKK |
| CMPR | Compare auxiliary register with auxiliary register AR0 | 1 | 1100 | 1110 | 0101 | 00KK |
| LAR | Load auxiliary register | 1 | 0011 | 0RRR | IDDD | DDDD |
| LARK | Load auxiliary register short immediate | 1 | 1100 | 0RRR | KKKK | KKKK |
| LARP | Load auxiliary register pointer | 1 | 0101 | 0101 | 1000 | 1RRR |
| LDP | Load data memory page pointer | 1 | 0101 | 0010 | IDDD | DDDD |
| LDPK | Load data memory page pointer immediate | 1 | 1100 | 100K | KKKK | KKKK |
| LRLK | Load auxiliary register long immediate | 2 | 1101 | 0RRR | 0000 | 0000 |
| MAR | Modify auxiliary register | 1 | 0101 | 0101 | IDDD | DDDD |
| SAR | Store auxiliary register | 1 | 0111 | 0RRR | IDDD | DDDD |
| SBRK | Subtract from auxiliary register short immediate | 1 | 0111 | 1111 | KKKK | KKKK |

T REGISTER, P REGISTER, AND MULTIPLY

| Mnemonic | Description | Words | 16 Bit OpCode MSB | | | LSB |
|---|---|---|---|---|---|---|
| APAC | Add P register to accumulator | 1 | 1100 | 1110 | 0001 | 0101 |
| LPH | Load high P register to accumulator | 1 | 0101 | 0011 | IDDD | DDDD |
| LT | Load T register | 1 | 0011 | 1100 | IDDD | DDDD |
| LTA | Load T register and accumulate previous product | 1 | 0011 | 1101 | IDDD | DDDD |
| LRD | Load T register, accumulate previous product and move data | 1 | 0011 | 1111 | IDDD | DDDD |
| LTP | Load T register and store P register in accumulator | 1 | 0011 | 1110 | IDDD | DDDD |
| LTS | Load T register and subtract previous product | 1 | 0101 | 1011 | IDDD | DDDD |
| MAC | Multiply and accumulate | 2 | 0101 | 1101 | IDDD | DDDD |
| MACD | Multiply and accumulate with data move | 2 | 0101 | 1100 | IDDD | DDDD |
| MPY | Multiply (with T register, store produce in P register) | 1 | 0011 | 1000 | IDDD | DDDD |
| MPYA | Multiply and accumulate previous product | 1 | 0011 | 1010 | IDDD | DDDD |
| MPYK | Multiply immediate | 1 | 101K | KKKK | KKKK | KKKK |
| MPYS | Multuply and subtract previous product | 1 | 0011 | 1011 | IDDD | DDDD |
| MPYU | Multiply unsigned | 1 | 1100 | 1111 | IDDD | DDDD |
| PAC | Load accumulator with P register | 1 | 1100 | 1110 | 0001 | 0100 |
| SPAC | Subtract P register from accumulator | 1 | 1100 | 1110 | 0001 | 0110 |
| SPH | Store high P register | 1 | 0111 | 1101 | IDDD | DDDD |
| SPL | Store low P register | 1 | 0111 | 1100 | IDDD | DDDD |
| SPM | Set P register output mode | 1 | 1100 | 1110 | 0000 | 10KK |
| SQRA | Square and accumulate | 1 | 0011 | 1010 | IDDD | DDDD |
| SQRS | Square and subtract previous product | 1 | 0101 | 1010 | IDDD | DDDD |

**NOTES**: For Instruction Symbols, see Page 21.

**FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)**

DESCRIPTION OF INSTRUCTIONS (CONTINUED)

BRANCH/CALL

| | | | 16 Bit OpCode | | | |
|---|---|---|---|---|---|---|
| **Mnemonic** | **Description** | **Words** | **MSB** | | | **LSB** |
| B | Branch unconditionally | 2 | 1111 | 1111 | 1DDD | DDDD |
| BACC | Branch to address specified by accumulator | 1 | 1100 | 1110 | 0010 | 0101 |
| BANZ | Branch on auxiliary register not zero | 2 | 1111 | 1011 | 1DDD | DDDD |
| BBNZ | Branch if TC bit < > 0 | 2 | 1111 | 1001 | 1DDD | DDDD |
| BBZ | Branch if TC bit = 0 | 2 | 1111 | 1000 | 1DDD | DDDD |
| BC | Branch on carry | 2 | 0101 | 1110 | 1DDD | DDDD |
| BGEZ | Branch if accumulator ≥ 0 | 2 | 1111 | 0100 | 1DDD | DDDD |
| BGZ | Branch if accumulator > 0 | 2 | 1111 | 0001 | 1DDD | DDDD |
| BIOZ | Branch on I/O status = 0 | 2 | 1111 | 0010 | 1DDD | DDDD |
| BLEZ | Branch if accumulator ≤ 0 | 2 | 1111 | 0010 | 1DDD | DDDD |
| BLZ | Branch if accumulator < 0 | 2 | 1111 | 0011 | 1DDD | DDDD |
| BNC | Branch on no carry | 2 | 0101 | 1111 | 1DDD | DDDD |
| BNV | Branch if no overflow | 2 | 1111 | 0111 | 1DDD | DDDD |
| BNZ | Branch if accumulator < > 0 | 2 | 1111 | 0101 | 1DDD | DDDD |
| BV | Branch on overflow | 2 | 1111 | 0000 | 1DDD | DDDD |
| BZ | Branch if accumulator = 0 | 2 | 1111 | 0110 | 1DDD | DDDD |
| CALA | Call subroutine indirect | 1 | 1100 | 1110 | 0010 | 0100 |
| CALL | Call subroutine | 2 | 1111 | 1110 | 1DDD | DDDD |
| RET | Return from subroutine | 1 | 1100 | 1110 | 0001 | 1110 |
| TRAP | Software interrupt | 1 | 1100 | 1110 | 0001 | 1110 |

I/O AND DATA MEMORY OPERATIONS

| | | | 16 Bit OpCode | | | |
|---|---|---|---|---|---|---|
| **Mnemonic** | **Description** | **Words** | **MSB** | | | **LSB** |
| BLKD | Block move from data memory to data memory | 2 | 1111 | 1101 | IDDD | DDDD |
| BLKP | Block move from programme memory to data memory | 2 | 1111 | 1100 | IDDD | DDDD |
| DMOV | Data move in data memory | 1 | 0101 | 0110 | IDDD | DDDD |
| FORT | Format serial port register | 1 | 1100 | 1110 | 0000 | 111K |
| IN | Input data from port | 1 | 1000 | AAAA | IDDD | DDDD |
| OUT | Output data to port | 1 | 1110 | AAAA | IDDD | DDDD |
| RFSM | Reset serial port frame synchronisation mode | 1 | 1100 | 1110 | 0011 | 0110 |
| RTXM | Reset serial port transmit mode | 1 | 1100 | 1110 | 0010 | 0000 |
| RXF | Reset external flag | 1 | 1100 | 1110 | 0000 | 1100 |
| SFSM | Set serial port frame synchronisation mode | 1 | 1100 | 1110 | 0011 | 0111 |
| STXM | Set serial port transmit mode | 1 | 1100 | 1110 | 0010 | 0001 |
| SXF | Set external flag | 1 | 1100 | 1110 | 0000 | 1101 |
| TBLR | Table read | 1 | 0101 | 1000 | IDDD | DDDD |
| TBLW | Table write | 1 | 0101 | 1001 | IDDD | DDDD |

**NOTES**: For Instruction Symbols, see Page 21.

## FIGURE 3(b) - TRUTH TABLE/INSTRUCTION SET (CONTINUED)

DESCRIPTION OF INSTRUCTIONS (CONTINUED)

ACCUMULATOR MEMORY REFERENCE

| Mnemonic | Description | Words | 16 Bit OpCode MSB | | | LSB |
|---|---|---|---|---|---|---|
| BIT | Test bit | 1 | 1001 | BBBB | IDDD | DDDD |
| BITT | Test bit specified by T register | 1 | 0101 | 0111 | IDDD | DDDD |
| CNFD | Configure block as data memory | 1 | 1100 | 1110 | 0000 | 0100 |
| CNFP | Configure block as programme memory | 1 | 1100 | 1110 | 0000 | 0101 |
| DINT | Disable interrupt | 1 | 1100 | 1110 | 0000 | 0001 |
| EINT | Enable interrupt | 1 | 1100 | 1110 | 0000 | 0000 |
| IDLE | Idle until interrupt | 1 | 1100 | 1110 | 0001 | 1111 |
| LST | Load status register ST0 | 1 | 0101 | 0000 | IDDD | DDDD |
| LST1 | Load status register ST1 | 1 | 0101 | 0001 | IDDD | DDDD |
| NOP | No operation | 1 | 0101 | 0101 | 0000 | 0000 |
| POP | Pop top of stack to low accumulator | 1 | 1100 | 1110 | 0001 | 1101 |
| POPD | Pop top of stack to data memory | 1 | 0111 | 1010 | IDDD | DDDD |
| PSHD | Push data memory value onto stack | 1 | 0101 | 0100 | IDDD | DDDD |
| PUSH | Push low accumulator onto stack | 1 | 1100 | 1110 | 0001 | 1100 |
| RC | Reset carry bit | 1 | 1100 | 1110 | 0011 | 0000 |
| RHM | Reset hold mode | 1 | 1100 | 1110 | 0011 | 1000 |
| ROVM | Reset overflow mode | 1 | 1100 | 1110 | 0000 | 0010 |
| RPT | Repeat instruction as specified by data memory value | 1 | 0100 | 1011 | IDDD | DDDD |
| RPTK | Repeat instruction as specified by immediate value | 1 | 1100 | 1011 | KKKK | KKKK |
| RSXM | Reset sign extension mode | 1 | 1100 | 1110 | 0000 | 0110 |
| RTC | Reset test/control flag | 1 | 1100 | 1110 | 0011 | 0010 |
| SC | Set carry bit | 1 | 1100 | 1110 | 0011 | 0001 |
| SHM | Set hold mode | 1 | 1100 | 1110 | 0011 | 1001 |
| SOVM | Set overflow mode | 1 | 1100 | 1110 | 0000 | 0011 |
| SST | Store status register ST0 | 1 | 0111 | 1000 | IDDD | DDDD |
| SST1 | Store status register ST1 | 1 | 0111 | 1001 | IDDD | DDDD |
| SSXM | Set sign extension mode | 1 | 1100 | 1110 | 0000 | 0111 |
| STC | Set test/control flag | 1 | 1100 | 1110 | 0011 | 0011 |

INSTRUCTION SYMBOLS

| SYMBOL | MEANING |
|---|---|
| B | 4-bit field specifying a bit code |
| CM | 2-bit field specifying compare mode |
| D | Data memory address field |
| FO | Format status bit |
| I | Addressing mode bit |
| K | Immediate operand bit |
| PA | Port address |
| PM | 2-bit field specifying P register output shift code |
| R | 3-bit operand field specifying auxiliary register |
| S | 4-bit left-shift code |
| X | 3-bit accumulator left-shift field |

## FIGURE 3(c) - CIRCUIT DESCRIPTION

X1 - Output from internal oscillator for crystal. If a crystal is not used, this pin should be left unconnected.

X2/CLKIN - Input to internal oscillator from crystal or external clock.

CLKOUT1 - Master clock output signal (crystal or CLKIN frequency/4).

CLKOUT2 - A second clock output signal.

D15 to D0 - 16-bit parallel data bus D15 (MSB) to D0 (LSB). Multiplexed to transfer data between signal processor and external programme/data memory or I/O devices. Placed in high-impedance state when no outputting or when $\overline{RS}$ or $\overline{HOLD}$ is activated.

A15 to A0 - 16-bit parallel address bus A15 (MSB) to A0 (LSB). Multiplexed to address external programme/data memory or I/O. Placed in high-impedance state in the hold mode.

$\overline{PS}$, $\overline{DS}$, $\overline{IS}$ - Programme, data and I/O space select signals. Always high unless low level activated for communicating to a particular external space. Placed in high-impedance state in the hold mode.

R/$\overline{W}$ - Read/write signal. Indicates transfer direction when communicating to a particular external space. Placed in high-impedance state in the hold mode.

$\overline{STRB}$ - Strobe signal. Always high unless activated low to indicate an external bus cycle. Placed in high-impedance state in the hold mode.

$\overline{RS}$ - Reset input. Causes the signal processor to terminate execution and forces the programme counter to zero. When brought to a high level, execution begins at location zero of programme memory.

$\overline{INT2}$ to $\overline{INT0}$ - 3 external user interrupt inputs. Prioritised and maskable by the interrupt mask register and the interrupt mode bit.

MP/$\overline{MC}$ - Microprocessor/microcomputer mode select pin. When activated low (microcomputer mode), the pin causes the internal ROM to be mapped into the lower 4k words of the programme memory map. In the microprocessor mode, the lower 4k words of programme memory are external.

$\overline{MSC}$ - Microstate complete signal, activated low and valid only during CLKOUT1 low when the signal processor has just completed a memory operation such as an instruction fetch or a data memory read/write.

$\overline{IACK}$ - Interrupt acknowledge signal. Output is only valid while CLKOUT1 is low. Indicates receipt of an interrupt and that the programme is branching to the interrupt-vector location indicated by A15 to A0.

READY - Data ready input. Indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY=0), the signal processor waits 1 cycle and checks READY again.

$\overline{BR}$ - Bus request signal. Activated when the signal processor requires access to an external global data memory space.

## FIGURE 3(c) - CIRCUIT DESCRIPTION (CONTINUED)

| | | |
|---|---|---|
| XF | - | External Flag output. |
| $\overline{\text{HOLD}}$ | - | Hold input. When activated, the signal processor places the data, address and control lines in the high-impedance state. |
| $\overline{\text{HOLDA}}$ | - | Hold acknowledge signal. Indicates that the signal processor has gone in the hold mode and that an external processor may access the local external memory of the signal processor. |
| $\overline{\text{SYNC}}$ | - | Synchronisation input. Allow clock synchronisation of 2 or more signal processors. SYNC is an active-low signal and must be activated on the rising edge of the CLKIN. |
| $\overline{\text{BIO}}$ | - | Branch control input. Polled by BIOZ instruction. If low the signal processor executes a branch. |
| DR | - | Serial data receive input. |
| CLKR | - | Clock for receive input for serial port. |
| FSR | - | Frame synchronisation pulse for receive input. |
| DX | - | Serial data transmit output. |
| CLKR | - | Clock for transmit output for serial port. |
| FSX | - | Frame synchronisation pulse for transmit. Configurable as either an input or an output. |

## FIGURE 3(d) - FUNCTIONAL DIAGRAM

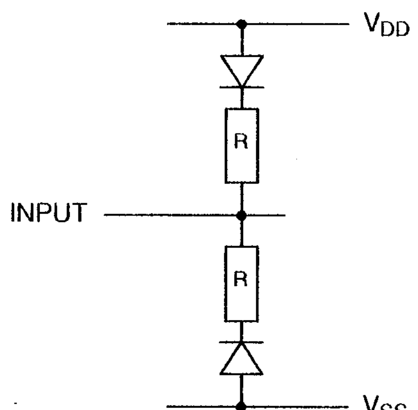
SYNC
IS
DS
PS
X1
X2/CLKIN
CLKOUT1
CLKOUT2
R/W
STRB
READY
BR
XF
HOLD
HOLDA
MSC
BIO
RS
IACK
CONTROLLER
MP/MC
INT(2 to 0)
3
PROGRAMME BUS
16
PFC(16)
MUX
PC(16)
MCS(16)
ADDRESS
PROGRAMME ROM (4096 × 16)
INSTRUCTION
STACK (8 × 16)
A15 to A0
D15 to D0
MUX
QIR(16)
IR(16)
ST0(16)
ST1(16)
RPTC(8)
IFR(6)
DR
CLKR
FSR
DX
CLKX
FSX
RSR(16)
XSR(16)
DRR(16)
DXR(16)
TIM(16)
PRD(16)
IMR(6)
GREG(8)
6
8
PROGRAMME BUS
DATA BUS
ARP(3)
ARB(3)
AR0(16)
AR1(16)
AR2(16)
AR3(16)
AR4(16)
AR5(16)
AR6(16)
AR7(16)
ARAU(16)
DP(9)
9
7 LSB FROM IR
SHIFTER(0-16)
TR(16)
MULTIPLIER
PR(32)
32
SHIFTER(-6,0,1,4)
MUX
ALU(32)
C
ACCH(16)
ACCL(16)
SHIFTER(0-7)
BLOCK B2 (32 × 16)
DATA RAM BLOCK B1 (256 × 16)
DATA/PROG RAM (256 × 16) BLOCK B0
DATA BUS

**FIGURE 3(d) - FUNCTIONAL DIAGRAM (CONTINUED)**

**LEGEND**

| | | |
|---|---|---|
| ACCH | = | Accumulator High. |
| ACCL | = | Accumulator Low. |
| ALU | = | Arithmetic Logic Unit. |
| ARAU | = | Auxiliary Register Arithmetic Unit. |
| ARB | = | Auxiliary Register Pointer Buffer. |
| ARP | = | Auxiliary Register Pointer. |
| DP | = | Data Memory Page Pointer. |
| DRR | = | Serial Port Data Receive Register. |
| DXR | = | Serial Port Data Transmit Register. |
| IFR | = | Interrupt Flag Register. |
| IMR | = | Interrupt Mask Register. |
| IR | = | Instruction Register. |
| MCS | = | Microcall Stack. |
| QIR | = | Queue Instruction Register. |
| PR | = | Product Register. |
| PRD | = | Period Register for Timer. |
| TIM | = | Timer. |
| TR | = | Temporary Register. |
| PC | = | Programme Counter. |
| PFC | = | Prefetch Counter. |
| RPTC | = | Repeat Instruction Counter. |
| GREG | = | Global Memory Allocation Register. |
| RSR | = | Serial Port Receive Shift Register. |
| XSR | = | Serial Port Transmit Shift Register. |
| AR0 to AR7 | = | Auxiliary Registers. |
| ST0 to ST1 | = | Status Registers. |
| C | = | Carry Bit. |

**FIGURE 3(e) - INPUT PROTECTION NETWORK**




**NOTES**

1. R = Diffused resistor of 300Ω.

## 2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:-

(a) ESA/SCC Generic Specification No. 9000 for Integrated Circuits.

(b) MIL-STD-883, Test Methods and Procedures for Micro-electronics.

## 3. TERMS, DEFINITIONS, ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESA/SCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:-

- $I_{DD}$ = Supply Current.
- $V_{IC}$ = Input Clamp Voltage.
- $t_{d(CIH-C)}$ = CLKIN High to CLKOUT1, CLKOUT2, $\overline{STRB}$ High/Low.
- $t_{r(C)}$ = CLKOUT1/CLKOUT2 $\overline{STRB}$ Rise Time.
- $t_{f(C)}$ = CLKOUT1/CLKOUT2 $\overline{STRB}$ Fall Time.
- $t_{w(CL)}$ = CLKOUT1/CLKOUT2 Low Pulse Duration.
- $t_{w(CH)}$ = CLKOUT1/CLKOUT2 High Pulse Duration.
- $t_{d(C1-C2)}$ = CLKOUT1 Low to CLKOUT2 High Delay Time.
- $t_{d(C1-S)}$ = CLKOUT1 to $\overline{STRB}$ Delay Time.
- $t_{d(C2-S)}$ = CLKOUT2 to $\overline{STRB}$ Delay Time.
- $t_{w(SL)}$ = $\overline{STRB}$ Low Pulse Duration (no wait state).
- $t_{su(IN)}$ = $\overline{INT}$/$\overline{BIO}$/$\overline{RS}$ Setup before CLKOUT1 High.
- $t_{h(IN)}$ = $\overline{INT}$/$\overline{BIO}$/$\overline{RS}$ Hold after CLKOUT1 High.
- $t_{w(IN)}$ = $\overline{INT}$/$\overline{BIO}$ Low Pulse Duration.
- $t_{w(RS)}$ = $\overline{RS}$ Low Pulse Duration.
- $t_{d(C1L-AL)}$ = CLKOUT1 Low to $\overline{HOLDA}$ Low Delay Time.
- $t_{d(HH-AH)}$ = $\overline{HOLD}$ High to $\overline{HOLDA}$ High Delay Time.
- $t_{d(C2H-H)}$ = $\overline{HOLD}$ Valid after CLKOUT2 High.
- $t_{su(FS)}$ = FSX/FSR Setup Time before CLKX/CLKR Falling Edge (TXM = 0).
- $t_{h(FS)}$ = FSX/FSR Hold Time after CLKX/CLKR Falling Edge (TXM = 0).
- $t_{su(DR)}$ = DR Setup Time before CLKR Falling Edge.
- $t_{h(DR)}$ = DR Hold Time after CLKR Falling Edge.
- $t_{d(CH-DX)}$ = DX Valid after CLKX Rising Edge.
- $t_{d(FL-DX)}$ = DX Valid after FSX Falling Edge (TXM = 0).
- $t_{d(CH-FS)}$ = FSXX Valid after CLKX Rising Edge (TXM = 1).
- $t_{su(A)}$ = Address Setup Time before $\overline{STRB}$ Low.
- $t_{h(A)}$ = Address Hold Time after $\overline{STRB}$ High.
- $t_{su(D)W}$ = Data Write Setup Time before $\overline{STRB}$ High.
- $t_{h(D)W}$ = Data Write Hold Time from $\overline{STRB}$ High.
- $t_{su(D)S}$ = Data Read Setup Time before $\overline{STRB}$ High.
- $t_{h(D)S}$ = Data Read Hold Time from $\overline{STRB}$ High.
- $t_{a(A)}$ = Read Data Access Time from Address Time.
- $t_{d(SL-R)}$ = READY Valid after STRB Low.
- $t_{h(SL-R)}$ = READY Hold Time after STRB Low (no wait state).
- $t_{d(C2H-R)}$ = READY Valid after CLKOUT2 High.
- $t_{h(C2h-R)}$ = READY Hold after CLKOUT2 Low.
- $t_{d(MSC)}$ = MSC Valid from CLKOUT1.
- $t_{d(M-R)}$ = READY Valid after MSC Valid.
- $t_{h(M-R)}$ = READY Hold Time after MSC Valid.
- $t_{d(IACK)}$ = CLKOUT1 to IACK Valid.
- $t_{d(XF)}$ = XF Valid before Falling Edge of $\overline{STRB}$.

## 4. REQUIREMENTS

### 4.1 GENERAL

The complete requirements for procurement of the integrated circuits specified herein are stated in this specification and ESA/SCC Generic Specification No. 9000 for Integrated Circuits. Deviations from the Generic Specification, applicable to this specification only, are listed in Para. 4.2.

Deviations from the applicable Generic Specification and this Detail Specification, formally agreed with specific Manufacturers on the basis that the alternative requirements are equivalent to the ESA/SCC requirements and do not affect the components' reliability, are listed in the appendices attached to this specification.

### 4.2 DEVIATIONS FROM GENERIC SPECIFICATION

#### 4.2.1 Deviations from Special In-process Controls

(a) Para. 5.2.2, Total Dose Irradiation Testing: Shall be performed during qualification and maintenance of qualification.

(b) Para. 5.2.2, Total Dose Irradiation Testing: If specified in a Purchase Order, shall be performed during procurement on a lot acceptance basis at the total dose irradiation level specified in the Purchase Order.

#### 4.2.2 Deviations from Final Production Tests (Chart II)

None.

#### 4.2.3 Deviations from Burn-in and Electrical Measurements (Chart III)

(a) Para. 7.1.1(a), "High Temperature Reverse Bias" test and subsequent electrical measurements related to this test shall be omitted.

#### 4.2.4 Deviations from Qualification Tests (Chart IV)

None.

#### 4.2.5 Deviations from Lot Acceptance Tests (Chart V)

None.

### 4.3 MECHANICAL REQUIREMENTS

#### 4.3.1 Dimension Check

The dimensions of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 2.

#### 4.3.2 Weight

The maximum weight of the integrated circuits specified herein shall be 5.0 grammes for chip carrier packages and 5.0 grammes for QFP package.

## 4.4 MATERIALS AND FINISHES

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the integrated circuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.

### 4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and the lids shall be pre-form soldered.

### 4.4.2 Lead Material and Finish

For leaded chip carrier and flat packages, the lead material shall be Type 'G' with either Type '4' or Type '7' finish in accordance with the requirements of ESA/SCC Basic Specification No. 23500. For leadless chip carrier packages, the finish shall be Type '4' or Type '7' in accordance with the requirements of ESA/SCC Basic Specification No. 23500. (See Table 1(a) for Type Variants).

## 4.5 MARKING

### 4.5.1 General

The marking of all components delivered to this specification shall be in accordance with the requirements of ESA/SCC Basic Specification No. 21700. Each component shall be marked in respect of:-

(a) Lead Identification.

(b) The SCC Component Number.

(c) Traceability Information.

### 4.5.2 Lead Identification

For each package variant, an index shall be located at one corner of the package in the position defined in Figure 2.

### 4.5.3 The SCC Component Number

Each component shall bear the SCC Component Number which shall be constituted and marked as follows:

951200101BF

- Detail Specification Number → 9512
- Type Variant (see Table 1(a)) → 001
- Testing Level (B or C, as applicable) → 01B... B
- Total Dose Irradiation Level (if applicable) → F

The Total Dose Irradiation Level designation shall be added for those devices for which a sample has been successfully tested to the level in question. For these devices, a code shall be added in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

### 4.5.4 Traceability Information

Each component shall be marked in respect of traceability information in accordance with the requirements of ESA/SCC Basic Specification No. 21700.

## 4.6 ELECTRICAL MEASUREMENTS

### 4.6.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 2. Unless otherwise specified, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

### 4.6.2 Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Table 3. The measurements shall be performed at $T_{amb} = +125(+0-5)$ °C and $-55(+5-0)$ °C respectively.

### 4.6.3 Circuits for Electrical Measurements

Circuits for use in performing electrical measurements listed in Tables 2 and 3 of this specification are shown in Figure 4.

## 4.7 BURN-IN TESTS

### 4.7.1 Parameter Drift Values

The parameter drift values applicable to burn-in are specified in Table 4 of this specification. Unless otherwise stated, measurements shall be performed at $T_{amb} = +22 \pm 3$ °C. The parameter drift values ($\Delta$) applicable to the parameters scheduled, shall not be exceeded. In addition to these drift value requirements, the appropriate limit value specified for a given parameter in Table 2 shall not be exceeded.

### 4.7.2 Conditions for H.T.R.B. Burn-in (Table 5(a))

Not applicable.

### 4.7.3 Conditions for Power Burn-in

The requirements for Power Burn-in are specified in Section 7 of ESA/SCC Generic Specification No. 9000. The conditions for Power Burn-in shall be as specified in Table 5(b) of this specification.

### 4.7.4 Electrical Circuits for H.T.R.B. Burn-in (Figure 5(a))

Not applicable.

### 4.7.5 Electrical Circuits for Power Burn-in

Circuits for use in performing the Power Burn-in test is shown in Figure 5(b) of this specification.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 1 | Functional Test 1 | - | - | 4(a) | Verify Truth Table with Load.<br>$V_{IL}$ = 0V, $V_{IH}$ = 4.5V<br>$I_{OL}$ = 2.4mA, $I_{OH}$ = 300μA<br>$V_{DD}$ = 4.5V, $V_{SS}$ = 0V<br>Test Programme 320C25S1<br>Note 1 | - | - | - |
| 2 | Functional Test 2 | - | - | 4(a) | Verify Truth Table with Load.<br>$V_{IL}$ = 0V, $V_{IH}$ = 5.5V<br>$I_{OL}$ = 2.4mA, $I_{OH}$ = 300μA<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Test Programme 320C25S1<br>Note 1 | - | - | - |
| 3 | Supply Current Idle/Hold | $I_{DD(S1)}$ | 3005 | - | f = 40MHz<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>(Pins 23 + 35 + 61 + 62) | - | 100 | mA |
| 4 | Supply Current Normal Mode | $I_{DD(S2)}$ | 3005 | - | f = 40MHz<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>(Pins 23 + 35 + 61 + 62) | - | 185 | mA |
| 5 to 18 | Input Current Low Level | $I_{IL}$ | 3009 | 4(b) | $V_{IN}$ (Under Test) = 0V<br>$V_{IN}$ (Remaining Inputs) = 5.5V<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | - | −10 | μA |
| 19 to 32 | Input Current High Level | $I_{IH}$ | 3010 | 4(c) | $V_{IN}$ (Under Test) = 5.5V<br>$V_{IN}$ (Remaining Inputs) = 0V<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | - | 10 | μA |
| 33 to 47 | Output Voltage Low Level | $V_{OL}$ | 3007 | 4(d) | $V_{IL}$ = Note 2, $V_{IH}$ = Note 2<br>$I_{OL}$ = 2.0mA<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 3<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-50-53-54-55-56-57-58-59-60) | - | 0.6 | V |

**NOTES**: See Page 36.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - d.c. PARAMETERS (CONT'D)**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 48 to 62 | Output Voltage High Level | $V_{OH}$ | 3006 | 4(e) | $V_{IL}$ = Note 2, $V_{IH}$ = Note 2<br>$I_{OH}$ = 300μA<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 3<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-50-53-54-55-56-57-58-59-60) | 2.4 | - | V |
| 63 to 101 | Output Leakage Current Third State (Low Level Applied) | $I_{OZL}$ | 3006 | 4(f) | $V_{OUT}$ = 0V<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 4<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-53-54) | - | −20 | μA |
| 102 to 140 | Output Leakage Current Third State (High Level Applied) | $I_{OZH}$ | 3006 | 4(f) | $V_{OUT}$ = 5.5V<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 4<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-53-54) | - | 20 | μA |
| 141 to 154 | Input Clamp Voltage (to $V_{SS}$) | $V_{IC1}$ | 3022 | 4(g) | $I_{IN}$ (Under Test) = −0.1mA<br>$V_{DD}$ = Open, $V_{SS}$ = 0V<br>All Other Pins Open<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | −0.4 | −0.9 | V |
| 155 to 168 | Input Clamp Voltage (to $V_{DD}$) | $V_{IC1}$ | 3022 | 4(g) | $I_{IN}$ (Under Test) = 0.1mA<br>$V_{DD}$ = 0V, $V_{SS}$ = Open<br>All Other Pins Open<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | 0.4 | 0.9 | V |

**NOTES**: See Page 36.

TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 169 to 182 | Input Capacitance | $C_{IN}$ | 3012 | 4(h) | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD} = V_{SS} = 0V$<br>Note 5<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | 10 | 20 | pF |
| 183 to 221 | Input/Output Capacitance | $C_{IN/OUT}$ | 3012 | 4(h) | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD} = V_{SS} = 0V$<br>Note 5<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-53-54) | 10 | 20 | pF |
| 222 | CLKIN High to CLKOUT1/2, $\overline{STRB}$ High/Low | $t_{d(CIH-C)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 58) | 5.0 | 30 | ns |
| 223 | CLKOUT1/2, $\overline{STRB}$ Rise Time | $t_{r(C)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 58) | - | 5.0 | ns |
| 224 | CLKOUT1/2, $\overline{STRB}$ Fall Time | $t_{f(C)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 58) | - | 5.0 | ns |
| 225 | CLKOUT1/2, Low Pulse Duration | $t_{w(CL)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 58) | 42 | 58 | ns |
| 226 | CLKOUT1/2, High Pulse Duration | $t_{w(CH)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 58) | 42 | 58 | ns |
| 227 | CLKOUT1 to CLKOUT2 High Delay Time | $t_{d(C1-C2)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 57) | 19 | 31 | ns |
| 228 | CLKOUT1 to $\overline{STRB}$ | $t_{d(C1-S)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 49) | 19 | 31 | ns |
| 229 | CLKOUT2 to $\overline{STRB}$ | $t_{d(C2-S)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 49) | −6.0 | 6.0 | ns |
| 230 | $\overline{STRB}$ Low Pulse Duration | $t_{w(SL)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 6<br>(Pin 49) | 45 | 55 | ns |

**NOTES**: See Page 36.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 231 | $\overline{HOLDA}$ Low after CLKOUT1 Low | $t_{d(C1L-AL)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 55) | 0 | 10 | ns |
| 232 | $\overline{HOLD}$ High to $\overline{HOLDA}$ High | $t_{d(HH-AH)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 55) | - | 25 | ns |
| 233 | DX Valid after CLKX Rising Edge | $t_{d(C\overline{H}-DX)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 9 and 10 (Pin 64) | - | 80 | ns |
| 234 | DX Valid after FSX Falling Edge | $t_{d(FL-DX)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 7, 9 and 10 (Pin 54) | - | 45 | ns |
| 235 | FSX Valid after CLKX Rising Edge | $t_{d(CH-FS)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 8 and 9 (Pin 53) | - | 45 | ns |
| 236 | Address Setup before $\overline{STRB}$ Low | $t_{su(A)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 6 and 11 (Pin 49) | 13 | - | ns |
| 237 | Address Hold after $\overline{STRB}$ Low | $t_{h(A)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 6 and 11 (Pin 49) | 17 | - | ns |
| 238 | Data Write Setup before $\overline{STRB}$ High | $t_{su(D)W}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 49) | 30 | - | ns |
| 239 | Data Write Hold after $\overline{STRB}$ High | $t_{h(D)W}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 49) | 15 | - | ns |
| 240 | MSC Valid from CLKOUT1 | $t_{d(MSC)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 58) | −10 | 10 | ns |
| 241 | CLKOUT1 to IACK Valid | $t_{d(IACK)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 60) | −8.0 | 8.0 | ns |
| 242 | XF Valid before $\overline{STRB}$ Falling Edge | $t_{d(XF)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 49) | 13 | - | ns |

**NOTES**: See Page 36.

## TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 243 | $\overline{INT}$/$\overline{BIO}$/$\overline{RS}$ Setup before CLKOUT1 High | $t_{su(IN)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 58) | 32 | - | ns |
| 244 | $\overline{INT}$/$\overline{BIO}$/$\overline{RS}$ Hold after CLKOUT1 High | $t_{h(IN)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 58) | 0 | - | ns |
| 245 to 248 | $\overline{INT}$/$\overline{BIO}$ Low Pulse Duration | $t_{w(IN)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pins 20-21-22-68) | 100 | - | ns |
| 249 | $\overline{RS}$ Low Pulse Duration | $t_{w(\overline{RS})}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 65) | 300 | - | ns |
| 250 | $\overline{HOLD}$ Valid after CLKOUT2 High | $t_{d(C2H-H)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 57) | - | 1.0 | ns |
| 251 | FSX/FSR before CLKX/CLKR Falling Edge | $t_{su(FS)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Notes 7 and 12<br>(Pin 64) | 18 | - | ns |
| 252 | FSX/FSR after CLKX/CLKR Falling Edge | $t_{h(FS)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Notes 7 and 12<br>(Pin 64) | 20 | - | ns |
| 253 | DR Setup before CLKR Falling Edge | $t_{su(DR)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 64) | 10 | - | ns |
| 254 | DR Hold after CLKR Falling Edge | $t_{h(DR)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 64) | 20 | - | ns |
| 255 | Data Read Setup before $\overline{STRB}$ High | $t_{su(D)S}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 49) | 23 | - | ns |
| 256 | Data Read Setup after $\overline{STRB}$ High | $t_{h(D)S}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 49) | 0 | - | ns |
| 257 to 258 | Read Data Access from Address Time | $t_{a(A)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pins 2 to 9, 11 to 18) | - | 35 | ns |
| 259 | Ready Valid after $\overline{STRB}$ Low | $t_{d(SL-R)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 12<br>(Pin 49) | - | 5.0 | ns |

**NOTES**: See Page 36.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE - a.c. PARAMETERS (CONT'D)**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 260 | Ready Hold after $\overline{\text{STRB}}$ Low | $t_{h(SL-R)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 12<br>(Pin 49) | 28 | - | ns |
| 261 | Ready Valid after CLKOUT2 High | $t_{d(C2H-R)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 12<br>(Pin 57) | - | 5.0 | ns |
| 262 | Ready Hold after CLKOUT2 High | $t_{h(C2H-R)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 12<br>(Pin 57) | 28 | - | ns |
| 263 | Ready Valid after MSC Valid | $t_{d(M-R)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 12<br>(Pin 59) | - | 25 | ns |
| 264 | Ready Hold after MSC Valid | $t_{h(M-R)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$<br>Note 12<br>(Pin 59) | 0 | - | ns |

**NOTES**: See Page 36.

**TABLE 2 - ELECTRICAL MEASUREMENTS AT ROOM TEMPERATURE (CONT'D)**

**NOTES**

1. Functional test go-no-go with timings at specification limits and trip point = 1.8V.
2. Dynamic measurement with $f_{(CL)}$ = 40MHz and the following input conditions:-
   - Pins 1, 19, 20, 21, 22, 24, 25, 65, 66, 67, 68 : $V_{IL}$ = 0.7V, $V_{IH}$ = 3.0V.
   - Pins 2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18, 52, 53, 63, 64 : $V_{IL}$ = 0.8V.
   - Pins 2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18, 53 : $V_{IH}$ = 2.2V.
   - Pins 52, 63, 64 : $V_{IH}$ = 3.5V.
3. Data Bus Pins 2, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 17, 18 are gathered in 1 test with the worst case recorded.
   Address Bus Pins 26, 28, 29, 30, 31, 32, 33, 34, 36, 37, 38, 39, 40, 41, 42, 43 are gathered in 1 test with the worst case recorded.
   Output Clock Pins 57, 58 are gathered in 1 test with the worst case recorded.
   All remaining pins are measured separately.
4. For I/Os, the measurement includes the Input Currents $I_{IL}$ and $I_{IH}$.
5. Guaranteed but not tested. Characterised at initial design and after major process changes.
6. Switching characteristic measured during Functional Test 2 with $f_{(CL)}$ = 40MHz, Duty Cycle 50%.
7. TXM bit must be set to "0" for this test.
8. TXM bit must be set to "1" for this test.
9. Switching characteristic measured during Functional Test 2 with Serial Port Clock (CLKX/CLKR) cycle time = 600ns.
10. Last occurance of FSX falling and CLKX rising.
11. A15 to A0, PS, DS, IS, R/W and BR timings are all included in timings referenced as "Address".
12. This parameter is tested but not recorded.

## TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 1 | Functional Test 1 | - | - | 4(a) | Verify Truth Table with Load.<br>$V_{IL}=0V$, $V_{IH}=4.5V$<br>$I_{OL}=2.4mA$, $I_{OH}=300\mu A$<br>$V_{DD}=4.5V$, $V_{SS}=0V$<br>Test Programme 320C25S1<br>Note 1 | - | - | - |
| 2 | Functional Test 2 | - | - | 4(a) | Verify Truth Table with Load.<br>$V_{IL}=0V$, $V_{IH}=5.5V$<br>$I_{OL}=2.4mA$, $I_{OH}=300\mu A$<br>$V_{DD}=5.5V$, $V_{SS}=0V$<br>Test Programme 320C25S1<br>Note 1 | - | - | - |
| 3 | Supply Current Idle/Hold | $I_{DD(S1)}$ | 3005 | - | f = 40MHz<br>$V_{DD}=5.5V$, $V_{SS}=0V$<br>(Pins 23 + 35 + 61 + 62) | - | 100 | mA |
| 4 | Supply Current Normal Mode | $I_{DD(S2)}$ | 3005 | - | f = 40MHz<br>$V_{DD}=5.5V$, $V_{SS}=0V$<br>(Pins 23 + 35 + 61 + 62) | - | 185 | mA |
| 5 to 18 | Input Current Low Level | $I_{IL}$ | 3009 | 4(b) | $V_{IN}$ (Under Test) = 0V<br>$V_{IN}$ (Remaining Inputs) = 5.5V<br>$V_{DD}=5.5V$, $V_{SS}=0V$<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | - | −10 | µA |
| 19 to 32 | Input Current High Level | $I_{IH}$ | 3010 | 4(c) | $V_{IN}$ (Under Test) = 5.5V<br>$V_{IN}$ (Remaining Inputs) = 0V<br>$V_{DD}=5.5V$, $V_{SS}=0V$<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | - | 10 | µA |
| 33 to 47 | Output Voltage Low Level | $V_{OL}$ | 3007 | 4(d) | $V_{IL}$ = Note 2, $V_{IH}$ = Note 2<br>$I_{OL}=2.0mA$<br>$V_{DD}=5.5V$, $V_{SS}=0V$<br>Note 3<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-50-53-54-55-56-57-58-59-60) | - | 0.6 | V |

**NOTES**: See Page 36.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - d.c. PARAMETERS (CONT'D)**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 48 to 62 | Output Voltage High Level | $V_{OH}$ | 3006 | 4(e) | $V_{IL}$ = Note 2, $V_{IH}$ = Note 2<br>$I_{OH}$ = 300μA<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 3<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-50-53-54-55-56-57-58-59-60) | 2.4 | - | V |
| 63 to 101 | Output Leakage Current Third State (Low Level Applied) | $I_{OZL}$ | 3006 | 4(f) | $V_{OUT}$ = 0V<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 4<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-53-54) | - | −20 | μA |
| 102 to 140 | Output Leakage Current Third State (High Level Applied) | $I_{OZH}$ | 3006 | 4(f) | $V_{OUT}$ = 5.5V<br>$V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 4<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-53-54) | - | 20 | μA |
| 141 to 154 | Input Clamp Voltage (to $V_{SS}$) | $V_{IC1}$ | 3022 | 4(g) | $I_{IN}$ (Under Test) = −0.1mA<br>$V_{DD}$ = Open, $V_{SS}$ = 0V<br>All Other Pins Open<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | −0.4 | −0.9 | V |
| 155 to 168 | Input Clamp Voltage (to $V_{DD}$) | $V_{IC1}$ | 3022 | 4(g) | $I_{IN}$ (Under Test) = 0.1mA<br>$V_{DD}$ = 0V, $V_{SS}$ = Open<br>All Other Pins Open<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | 0.4 | 0.9 | V |

**NOTES**: See Page 36.

## TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 169 to 182 | Input Capacitance | $C_{IN}$ | 3012 | 4(h) | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD} = V_{SS} = 0V$<br>Note 5<br>(Pins 1-19-20-21-22-24-25-52-63-64-65-66-67-68) | 10 | 20 | pF |
| 183 to 221 | Input/Output Capacitance | $C_{IN/OUT}$ | 3012 | 4(h) | $V_{IN}$ (Not Under Test) = 0V<br>$V_{DD} = V_{SS} = 0V$<br>Note 5<br>(Pins 2-3-4-5-6-7-8-9-11-12-13-14-15-16-17-18-26-28-29-30-31-32-33-34-36-37-38-39-40-41-42-43-45-46-47-48-49-53-54) | 10 | 20 | pF |
| 222 | CLKIN High to CLKOUT1/2, $\overline{STRB}$ High/Low | $t_{d(CIH-C)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 58) | 5.0 | 30 | ns |
| 223 | CLKOUT1/2, $\overline{STRB}$ Rise Time | $t_{r(C)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 58) | - | 5.0 | ns |
| 224 | CLKOUT1/2, $\overline{STRB}$ Fall Time | $t_{f(C)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 58) | - | 5.0 | ns |
| 225 | CLKOUT1/2, Low Pulse Duration | $t_{w(CL)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 58) | 42 | 58 | ns |
| 226 | CLKOUT1/2, High Pulse Duration | $t_{w(CH)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 58) | 42 | 58 | ns |
| 227 | CLKOUT1 to CLKOUT2 High Delay Time | $t_{d(C1-C2)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 57) | 19 | 31 | ns |
| 228 | CLKOUT1 to $\overline{STRB}$ | $t_{d(C1-S)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 49) | 19 | 31 | ns |
| 229 | CLKOUT2 to $\overline{STRB}$ | $t_{d(C2-S)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 49) | −6.0 | 6.0 | ns |
| 230 | $\overline{STRB}$ Low Pulse Duration | $t_{w(SL)}$ | - | 4(i) | $V_{DD}$ = 5.5V, $V_{SS}$ = 0V<br>Note 6<br>(Pin 49) | 45 | 55 | ns |

**NOTES**: See Page 36.

## TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 231 | $\overline{HOLDA}$ Low after CLKOUT1 Low | $t_{d(C1L-AL)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 55) | 0 | 10 | ns |
| 232 | $\overline{HOLD}$ High to $\overline{HOLDA}$ High | $t_{d(HH-AH)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 55) | - | 25 | ns |
| 233 | DX Valid after CLKX Rising Edge | $t_{d(CH-DX)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 9 and 10 (Pin 64) | - | 80 | ns |
| 234 | DX Valid after FSX Falling Edge | $t_{d(FL-DX)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 7, 9 and 10 (Pin 54) | - | 45 | ns |
| 235 | FSX Valid after CLKX Rising Edge | $t_{d(CH-FS)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 8 and 9 (Pin 53) | - | 45 | ns |
| 236 | Address Setup before $\overline{STRB}$ Low | $t_{su(A)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 6 and 11 (Pin 49) | 13 | - | ns |
| 237 | Address Hold after $\overline{STRB}$ Low | $t_{h(A)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 6 and 11 (Pin 49) | 17 | - | ns |
| 238 | Data Write Setup before $\overline{STRB}$ High | $t_{su(D)W}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 49) | 30 | - | ns |
| 239 | Data Write Hold after $\overline{STRB}$ High | $t_{h(D)W}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 49) | 15 | - | ns |
| 240 | MSC Valid from CLKOUT1 | $t_{d(MSC)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 58) | −10 | 10 | ns |
| 241 | CLKOUT1 to IACK Valid | $t_{d(IACK)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 60) | −8.0 | 8.0 | ns |
| 242 | XF Valid before $\overline{STRB}$ Falling Edge | $t_{d(XF)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 6 (Pin 49) | 13 | - | ns |

**NOTES:** See Page 36.

**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES**
**- a.c. PARAMETERS (CONT'D)**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 243 | $\overline{INT}/\overline{BIO}/\overline{RS}$ Setup before CLKOUT1 High | $t_{su(IN)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 58) | 32 | - | ns |
| 244 | $\overline{INT}/\overline{BIO}/\overline{RS}$ Hold after CLKOUT1 High | $t_{h(IN)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 58) | 0 | - | ns |
| 245 to 248 | $\overline{INT}/\overline{BIO}$ Low Pulse Duration | $t_{w(IN)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pins 20-21-22-68) | 100 | - | ns |
| 249 | $\overline{RS}$ Low Pulse Duration | $t_{w(\overline{RS})}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 65) | 300 | - | ns |
| 250 | $\overline{HOLD}$ Valid after CLKOUT2 High | $t_{d(C2H-H)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 57) | - | 1.0 | ns |
| 251 | FSX/FSR before CLKX/CLKR Falling Edge | $t_{su(FS)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 7 and 12 (Pin 64) | 18 | - | ns |
| 252 | FSX/FSR after CLKX/CLKR Falling Edge | $t_{h(FS)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Notes 7 and 12 (Pin 64) | 20 | - | ns |
| 253 | DR Setup before CLKR Falling Edge | $t_{su(DR)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 64) | 10 | - | ns |
| 254 | DR Hold after CLKR Falling Edge | $t_{h(DR)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 64) | 20 | - | ns |
| 255 | Data Read Setup before $\overline{STRB}$ High | $t_{su(D)S}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 49) | 23 | - | ns |
| 256 | Data $\overline{Read}$ Setup after $\overline{STRB}$ High | $t_{h(D)S}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 49) | 0 | - | ns |
| 257 to 258 | Read Data Access from Address Time | $t_{a(A)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pins 2 to 9, 11 to 18) | - | 35 | ns |
| 259 | Ready Valid after $\overline{STRB}$ Low | $t_{d(SL-R)}$ | - | 4(i) | $V_{DD} = 5.5V$, $V_{SS} = 0V$ Note 12 (Pin 49) | - | 5.0 | ns |

**NOTES**: See Page 36.

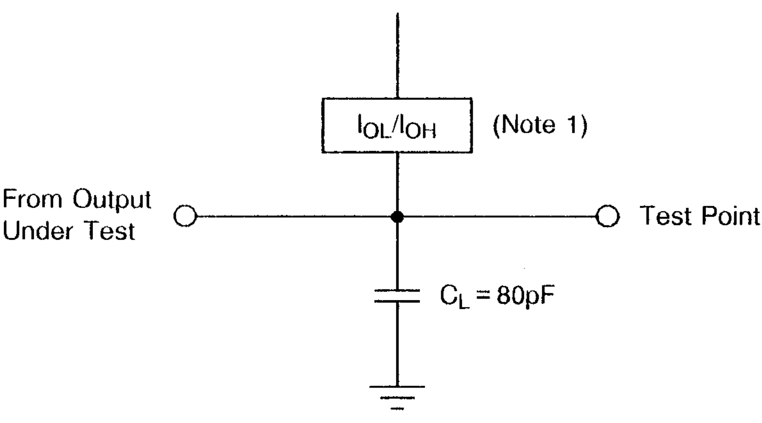
**TABLE 3 - ELECTRICAL MEASUREMENTS AT HIGH AND LOW TEMPERATURES - a.c. PARAMETERS (CONT'D)**

| No. | CHARACTERISTICS | SYMBOL | TEST METHOD MIL-STD 883 | TEST FIG. | TEST CONDITIONS (PINS UNDER TEST) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | MAX | |
| 260 | Ready Hold after $\overline{STRB}$ Low | $t_{h(SL-R)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$ Note 12 (Pin 49) | 28 | - | ns |
| 261 | Ready Valid after CLKOUT2 High | $t_{d(C2H-R)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$ Note 12 (Pin 57) | - | 5.0 | ns |
| 262 | Ready Hold after CLKOUT2 High | $t_{h(C2H-R)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$ Note 12 (Pin 57) | 28 | - | ns |
| 263 | Ready Valid after MSC Valid | $t_{d(M-R)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$ Note 12 (Pin 59) | - | 25 | ns |
| 264 | Ready Hold after MSC Valid | $t_{h(M-R)}$ | - | 4(i) | $V_{DD}=5.5V$, $V_{SS}=0V$ Note 12 (Pin 59) | 0 | - | ns |

**NOTES**: See Page 36.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS

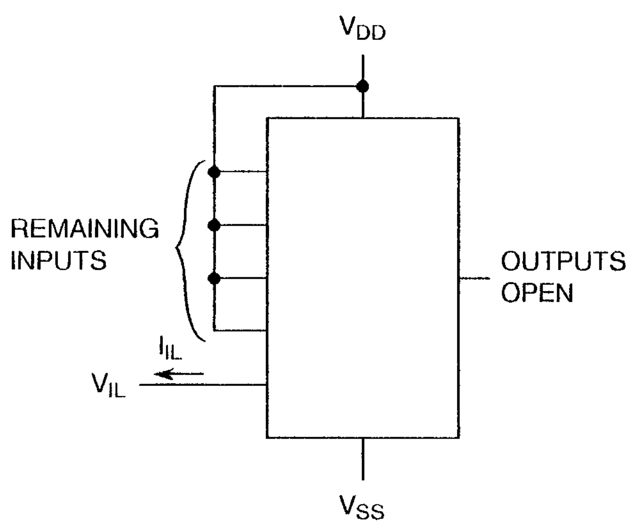
### FIGURE 4(a) - TEST LOAD CIRCUIT




**NOTES**

1. $I_{OL}/I_{OH}$ shall be a current source.

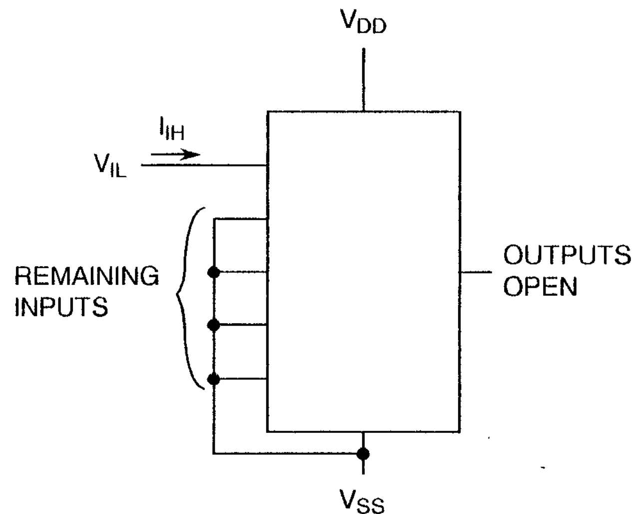
### FIGURE 4(b) - INPUT CURRENT LOW LEVEL




**NOTES**

1. Each input to be tested separately.

### FIGURE 4(c) - INPUT CURRENT HIGH LEVEL



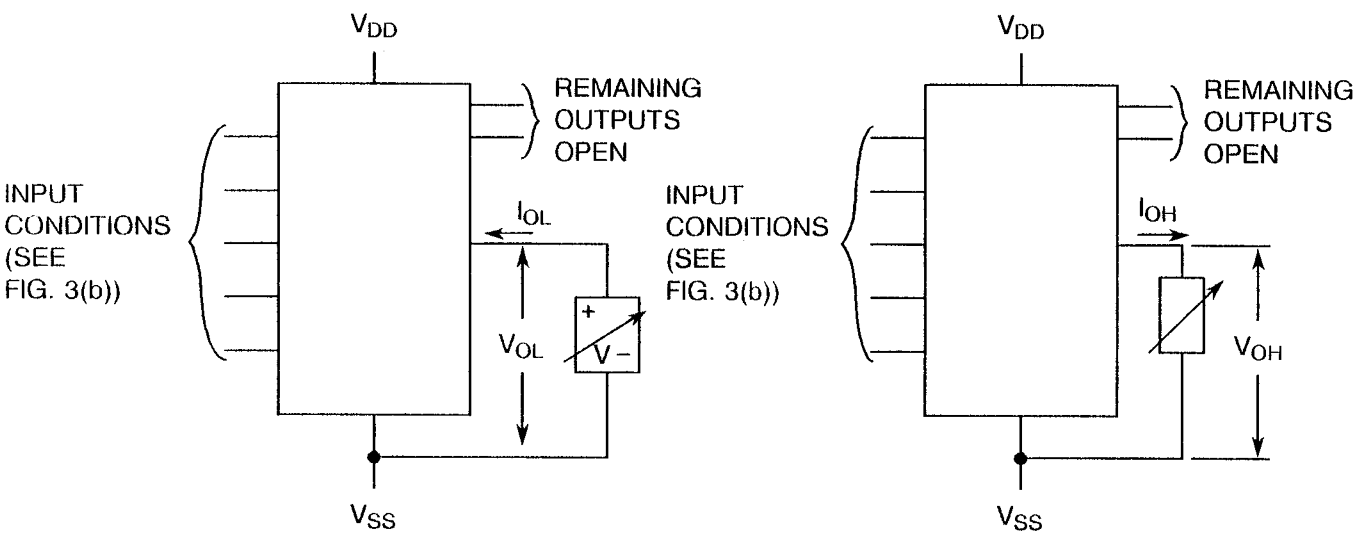

**NOTES**

1. Each input to be tested separately.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

FIGURE 4(d) - OUTPUT VOLTAGE LOW LEVEL

FIGURE 4(e) - OUTPUT VOLTAGE HIGH LEVEL



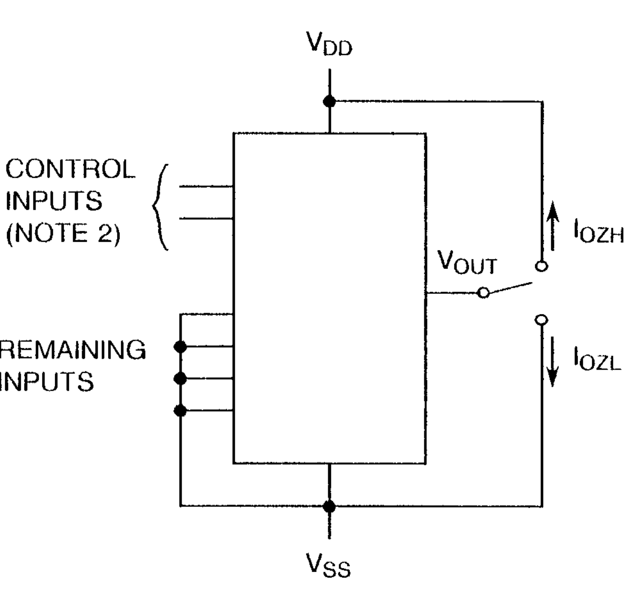

**NOTES**

1. Each output to be tested separately.

**NOTES**

1. Each output to be tested separately.

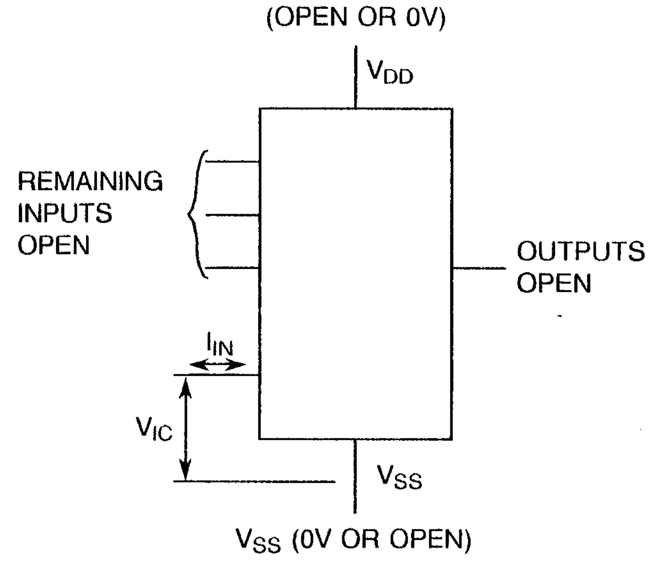
FIGURE 4(f) - OUTPUT LEAKAGE CURRENT THIRD STATE




**NOTES**

1. Each input to be tested separately.
2. Control inputs as per test programme.

FIGURE 4(g) - INPUT CLAMP VOLTAGE

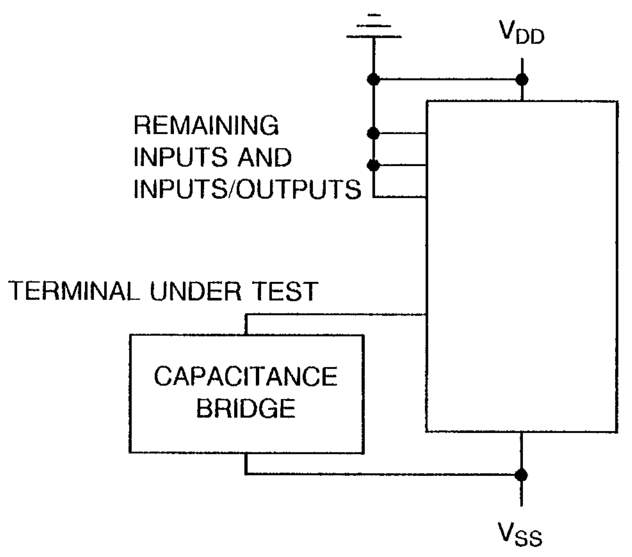



**NOTES**

1. Each input to be tested separately.

## FIGURE 4 - CIRCUITS FOR ELECTRICAL MEASUREMENTS (CONTINUED)

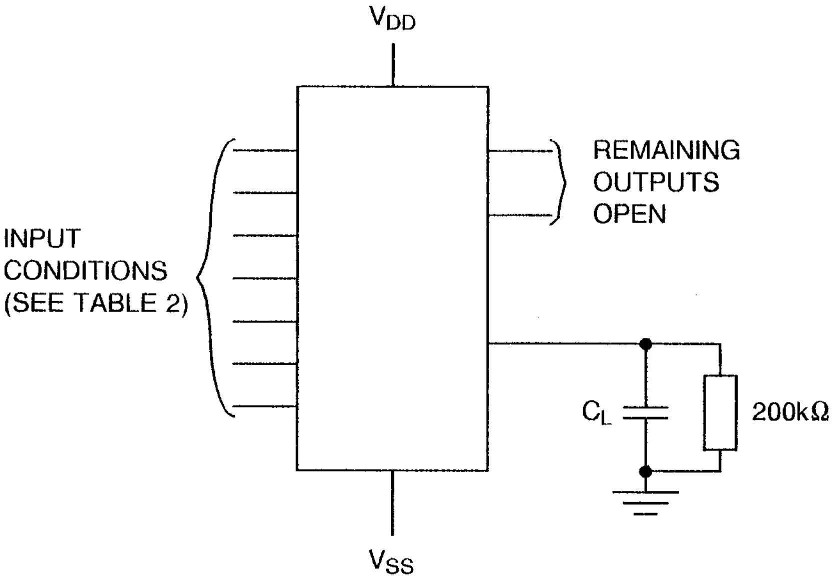
FIGURE 4(i) - INPUT AND INPUT/OUTPUT CAPACITANCE




**NOTES**

1. Test frequency = 1.0MHz.
2. Each input and input/output to be tested separately.

FIGURE 4(j) - PROPAGATION DELAY




**NOTES**

1. Pulse Generator: $V_P = 0V$ to $V_{DD}$, $t_r$ and $t_f \leq 6.0ns$, $f = 1.0MHz$ minimum, 50% Duty Cycle, $Z_{OUT} = 50\Omega$.
2. $C_L = 50pF \pm 5\%$ including scope, wiring and stray capacitance without package in test fixture.
3. For test waveforms see Figure 3(b).

## TABLE 4 - PARAMETER DRIFT VALUES

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS (Δ) | UNIT |
|---|---|---|---|---|---|---|
| 3 | Supply Current Idle/$\overline{\text{Hold}}$ | $I_{DD(S1)}$ | As per Table 2 | As per Table 2 | ±10 | mA |
| 4 | Supply Current Normal Mode | $I_{DD(S2)}$ | As per Table 2 | As per Table 2 | ±18 | mA |
| 5 to 18 | Input Current Low Level | $I_{IL}$ | As per Table 2 | As per Table 2 | ±0.5 | μA |
| 19 to 32 | Input Current High Level | $I_{IH}$ | As per Table 2 | As per Table 2 | ±0.5 | μA |
| 33 to 47 | Output Voltage Low Level | $V_{OL}$ | As per Table 2 | As per Table 2 | ±60 | mV |
| 48 to 62 | Output Voltage High Level | $V_{OH}$ | As per Table 2 | As per Table 2 | ±240 | mV |
| 63 to 101 | Output Leakage Current Third State (Low Level Applied) | $I_{OZL}$ | As per Table 2 | As per Table 2 | ±0.5 | μA |
| 102 to 140 | Output Leakage Current Third State (High Level Applied) | $I_{OZH}$ | As per Table 2 | As per Table 2 | ±0.5 | μA |
| 222 | CLKIN High to CLKOUT1/2, $\overline{\text{STRB}}$ High/Low | $t_{d(CIH-C)}$ | As per Table 2 | As per Table 2 | ±5.0 | ns |
| 236 | Address Setup before $\overline{\text{STRB}}$ Low | $t_{su(A)}$ | As per Table 2 | As per Table 2 | ±5.0 | ns |
| 237 | Address Hold after $\overline{\text{STRB}}$ Low | $t_{h(A)}$ | As per Table 2 | As per Table 2 | ±5.0 | ns |

**TABLE 5(a) - CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN**

Not applicable.

**TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS**

| No. | CHARACTERISTICS | SYMBOL | CONDITION | UNIT |
|---|---|---|---|---|
| 1 | Ambient Temperature | $T_{amb}$ | +125(+0−3) | °C |
| 2 | Frequency | F | 2.2 ± 0.3 | MHz |
| 3 | Pulse Voltage | $V_{GEN}$ | 0 to 0.4 max.<br>to<br>min. 3.0 to 5.0 | V |
| 4 | Duty Cycle | - | 50 ± 20 | % |
| 5 | Positive Supply Voltage | $V_{DD}$ | 5.0 ± 0.5 | V |
| 6 | Negative Supply Voltage | $V_{SS}$ | GND | V |
| 7 | Output Load Voltage | $V_{OUT}$ | 3.5 ± 0.5 | V |
| 8 | Activation Programme | | Note 1 | |

**NOTES**: See Page 46

**TABLE 5(b) - CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS (CONT'D)**

**NOTES**

1. Burn-in activation programme is written in 320C25 Assembler language and object codes can be stored in either pattern generator or memory.

| LINE | ADDRESS | OPCODE | INSTRUCTIONS | | | COMMENTS |
|---|---|---|---|---|---|---|
| 0001 | | | | IDT | 'LIFETEST' | |
| 0002 | | | * | | | * D6 IS GROUNDED ON THE LIFETEST BOARD |
| 0004 | | | * | | | |
| 0005 | | 0001 | DXR | EQU | 1 | |
| 0006 | | 0002 | TIMER | EQU | 2 | |
| 0007 | | 0003 | PERIOD | EQU | 3 | |
| 0008 | | 0004 | IMR | EQU | 4 | |
| 0009 | | 0005 | GREG | EQU | 5 | |
| 0010 | | | * | | | |
| 0011 | | | * R10 TOP | RESET | | |
| 0012 | 0000 | C800 | R5 | LDPK | 0 | |
| 0013 | 0001 | 5588 | | LARP | AR0 | |
| 0014 | 0002 | D000 | | LLRK | AR0, >0300 | |
| | 0003 | 0300 | | | | |
| 0015 | 0004 | D100 | | LLRK | AR1, >0800 | |
| | 0005 | 0800 | | | | |
| 0016 | 0006 | 7002 | | SAR | 0,TIMER | |
| 0017 | 0007 | 7103 | | SAR | 1,PERIOD | |
| 0018 | 0008 | 7201 | | SAR | 2,DXR | |
| 0019 | 0009 | 7305 | | SAR | 3,GREG | |
| 0020 | 000A | 7404 | | SAR | 4,IMR | |
| 0021 | 000B | 4780 | | SUBC | * | |
| 0022 | 000C | CE0C | | RXF | | |
| 0023 | 000D | CB05 | | RPTK | >05 | |
| 0024 | 000E | 3B80 | R6 | MACD | * | |
| 0025 | 000F | 5780 | | BITT | * | |
| 0026 | 0010 | CE0F | | FORT | 1 | |
| 0027 | 0011 | FB89 | | BANZ | >7FBF,*,1 | |
| | 0012 | 7FBF | | | | |
| 0028 | 0013 | 5480 | | PSHD | * | |
| 0029 | 0014 | 0000 | | DATA | >0000 | |
| 0030 | 0015 | CE0D | | SXF | | |
| 0031 | 0016 | 7A80 | | POPD | * | |
| 0032 | 0017 | 0000 | | DATA | >0000 | *. DATA WRITE CYCLE |
| 0033 | 0018 | CE0C | | RXF | | |
| 0034 | 0019 | 4080 | | ZALH | * | |
| 0035 | 001A | FFFF | | DATA | >FFFF | |
| 0036 | 001B | CE07 | | SSXM | | |
| 0037 | 001C | 6880 | | SACH | * | |
| 0038 | 001D | 0000 | | DATA | >5500 | *. DEAD CYCLE = NOP |
| 0039 | 001E | FFFF | | DATA | >5500 | *. DATA WRITE CYCLE |
| 0040 | | | * | GOTO TOP | | |

**FIGURE 5(a) - ELECTRICAL CIRCUIT FOR HIGH TEMPERATURE REVERSE BIAS BURN-IN**

Not applicable.

**FIGURE 5(b) - ELECTRICAL CIRCUIT FOR POWER BURN-IN AND OPERATING LIFE TESTS**



LID UP VIEW, TOP VIEW OF BOARD

**NOTES**

1. Resistors = 1.5kΩ, 5.0%, 1/4 Watt.

4.8 ENVIRONMENTAL AND ENDURANCE TESTS (CHARTS IV AND V OF ESA/SCC GENERIC SPECIFICATION NO. 9000)

4.8.1 Electrical Measurements on Completion of Environmental Tests

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.2 Electrical Measurements at Intermediate Points during Endurance Tests

The parameters to be measured at intermediate points during endurance tests are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.3 Electrical Measurements on Completion of Endurance Tests

The parameters to be measured on completion of endurance testing are as scheduled in Table 6 of this specification. Unless otherwise stated, the measurements shall be performed at $T_{amb} = +22 \pm 3$ °C.

4.8.4 Conditions for Operating Life Tests

The requirements for operating life testing are specified in Section 9 of ESA/SCC Generic Specification No. 9000. The conditions for operating life testing shall be as specified in Table 5(b) of this specification.

4.8.5 Electrical Circuits for Operating Life Tests

Circuits for use in performing the operating life tests are shown in Figure 5(b) of this specification.

4.8.6 Conditions for High Temperature Storage Test

The requirements for the high temperature storage test are specified in ESA/SCC Generic Specification No. 9000. The temperature to be applied shall be the maximum storage temperature specified in Table 1(b) of this specification.

4.9 TOTAL DOSE IRRADIATION TESTING

4.9.1 Application

If specified in Para. 4.2.1 of this specification, total dose irradiation testing shall be performed in accordance with the requirements of ESA/SCC Basic Specification No. 22900.

4.9.2 Bias Conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6.

4.9.3 Electrical Measurements

The parameters to be measured prior to irradiation exposure are scheduled in Table 2 of this specification. Only devices which meet the requirements of Table 2 shall be scheduled in the test sample.

The parameters to be measured during and on completion of irradiation testing are scheduled in Table 7 of this specification.

## TABLE 6 - ELECTRICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | CHANGE LIMITS (Δ) | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN. | MAX. | |
| 1 | Functional Test 1 | - | As per Table 2 | As per Table 2 | - | - | - | - |
| 3 | Supply Current Idle/Hold | $I_{DD(S1)}$ | As per Table 2 | As per Table 2 | ± 10 | - | 100 | mA |
| 4 | Supply Current Normal Mode | $I_{DD(S2)}$ | As per Table 2 | As per Table 2 | ± 18 | - | 185 | mA |
| 5 to 18 | Input Current Low Level | $I_{IL}$ | As per Table 2 | As per Table 2 | ± 0.5 | - | − 10 | μA |
| 19 to 32 | Input Current High Level | $I_{IH}$ | As per Table 2 | As per Table 2 | ± 0.5 | - | 10 | μA |
| 33 to 47 | Output Voltage Low Level | $V_{OL}$ | As per Table 2 | As per Table 2 | ± 0.06 | - | 0.6 | V |
| 48 to 62 | Output Voltage High Level | $V_{OH}$ | As per Table 2 | As per Table 2 | ± 0.24 | 2.4 | - | V |
| 63 to 101 | Output Leakage Current Third State (Low Level Applied) | $I_{OZL}$ | As per Table 2 | As per Table 2 | ± 0.5 | - | − 20 | μA |
| 102 to 140 | Output Leakage Current Third State (High Level Applied) | $I_{OZH}$ | As per Table 2 | As per Table 2 | ± 0.5 | - | 20 | μA |

**FIGURE 6 - BIAS CONDITIONS FOR IRRADIATION TESTING**

320C25

$V_{OUT}$

0V

5.0 ± 0.5V

LID UP VIEW, TOP VIEW OF BOARD

**NOTES**

1. Resistors = 1.5kΩ, 5.0%, 1/4 Watt.

**TABLE 7 - ELECTRICAL MEASUREMENTS DURING AND ON COMPLETION OF IRRADIATION TESTING**

| No. | CHARACTERISTICS | SYMBOL | SPEC. AND/OR TEST METHOD | TEST CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| 3 | Supply Current Idle/Hold | $I_{DD(S1)}$ | As per Table 2 | As per Table 2 | - | 100 | mA |
| 4 | Supply Current Normal Mode | $I_{DD(S2)}$ | As per Table 2 | As per Table 2 | - | 185 | mA |

**APPENDIX 'A'**



AGREED DEVIATIONS FOR TEXAS INSTRUMENTS (F)

| ITEMS AFFECTED | DESCRIPTION OF DEVIATIONS |
|---|---|
| Para. 4.2.2 | Precap Inspection may be performed using TIF documents "PRECAP INSPECTION MIL-STD-883, METHOD 2010, CONDITION 'A', SPEC No. 50.22-1068".<br><br>Prior to Die Shear Test, TIF may perform a Radiographic Inspection on the randomly chosen samples to be subjected to this test using TIF document TIF 50.42-3002. |
| Para. 4.2.3 | Radiographic Inspection may be performed using TIF document TIF 50.42-3002. |

FUNCTIONAL TEST OVERVIEW

The Functional Tests contain patterns for the following tests:-

3-State, $I_{DD}$ Hold Mode, $I_{DD}$ Normal Mode, Hold Mode, Hold RAM Mode, RAM, Global Memory Allocation, Input/Output, Multiplier, Programme Counter, Prefetch Counter, Hold/Idle Mode, Arithmetic Logic Unit, Auxiliary Registers, Programme Counter/Stack, Repeat Instructions, Status Registers, Timer.