ESA Capability Assessment : CCD Evaluation Programme

Project Completion and Final Review Presentation

Held at ESA Estec, Noordwijk, The Netherlands 16th March 2004

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Overview of the Presentation



- Aims and Objectives of the Programme
- Structure of the Programme
- Concept and Definition of "The Capability Domain"
- The Construction of the Samples
- The Evaluation Plan
- Key Results and Observations from the Evaluation
- Conclusions



technology and construction can also be deemed to be covered by the evaluation

Structure of the Programme



Definition Phase

- Define a Draft PID and Detail Specification for each CCD Type
- Manufacture Samples for Evaluation
- Submit Samples for Constructional Analysis by ESA
- ESA to conduct a Manufacturer Survey and Line Audit
- Define the Evaluation Test Plan
- Evaluation Part 1
 - CCD Evaluation Testing to Plan (Excluding Life Test)
- Evaluation Part 2
 - CCD Evaluation Testing to Plan (Accelerated Life Test)
 - Review Results of Evaluation
- Extent of Evaluation Applicability
 - Definition of Capability Domain

Definition of "The Domain"

 A Domain is set of physical attributes which can describe a range of CCDs either by specifying individual parameter conditions or by setting a range with boundary limits for each

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- The two CCD types to be evaluated were, where possible, chosen to represent the boundaries for each domain parameter although some extrapolation and read-across was agreed
- Specific exclusions from The Domain were also defined



Design Parameter	Proposed Domain	CCD55-20	CCD57-10
Silicon CCD, Photosensitive	yes	yes	yes
P-type silicon epitaxy	20mΩcm CZ substrate, 20Ωcm to 1500Ωcm epi 13 to 50 μ m thick	20mΩcm CZ substrate, 100Ωcm 25 <i>°</i> m epi.	20mΩcm CZ substrate, 20Ωcm 20 <i>°</i> m epi
Photo- lithographic stitching	Proprietary e2v technologies technique for defining butted areas of photolith exposure	Two stitched sections	None
Buried n-channel	yes	yes	yes
Illumination type	Front Face or Back face illuminated (on silicon support) -variants of passivation process included	Back-illuminated (on silicon support) ⊮Enhanced QE Process	Front-illuminated
Store shield	yes	yes, on back face	yes, on front face



Design Parameter	Proposed Domain	CCD55-20	CCD57-10
Number of electrode phases	3	3	3
Operating Mode	Standard mode, or Advanced inverted mode(AIMO)	AIMO	Standard
Pixel Size	13 to 27 microns square	22.5 microns square	13 microns square
Output responsivity	0.5 to 6 μV/e-	0.6µV/e-	6μV/e-
Dump drain	Gated or none	gated	gated
Antiblooming	Fixed barrier or none	none	fixed, shielded
Image architecture	full frame, frame transfer or split frame transfer	frame transfer (in this package)	frame transfer but tested in full frame mode
Readout register architecture	single or dual output, split or continuous register	dual output continuous (single output only in this package)	dual output split register



Design Parameter	Proposed Domain	CCD55-20	CCD57-10
Packaging type	Co- fired ceramic, alumina, with optional aluminium nitride substrate/insert, maximum size 40 x 45mm with gold plated contact pads and 36 pins max. of material ASTM F15 (ESA type D) or Alloy 42 (ESA Type G) both with Nickel plate (50 - 350 micro- inch) under Gold plate (50 micro - inch minimum). Adhesive die attach. Ultrasonic aluminium wire bonding.	Co-fired ceramic, alumina, with aluminium nitride substrate/insert, 40 x 45mm with gold plated contact pads and 22 gold on nickel plated ASTM F15 pins. Adhesive die attach. Ultrasonic aluminium wire bonding.	Co-fired ceramic, alumina, 30 x 23mm with gold plated conta ct pads and 24 gold on nickel plated Alloy 42 pins. Adhesive die attach. Ultrasonic aluminium wire bonding.
Window type	with or without glass window, window to be specified to be safe to 1 atmosphere, CTE matched to package material and with or without multilayer AR coating.	without	Broad band AR coated, optical glass window
Active Area	0.1 to 5 cm ²	4.6 cm ²	0.9cm ²

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Design Parameter	Proposed Domain	CCD55-20	CCD57-10
Gate protection circuits	Full back to back zener diodes	Full back to back zener diodes	Full back to back zener diodes
Output amplifier	Two stage FET with Reset transistor	Two stage FET with Reset transistor (two on-chip amplifiers, only one accessible in the package)	Two stage FET with Reset transistor (two on-chip amplifiers).
On-chip Anti- Reflection coating (Back-Illuminated devices only)	Single layer, hafnium oxide, quarter-wavelength coating- various thickness	Single layer, hafnium oxide, ⊮Broadband aR coating	Not Applicable
Operating and Storage Temperature	-55 to +50 ℃* -55 to +125 ℃	-55 to +50 ℃* -55 to +125 ℃	-55 to +50⁼℃* -55 to +125⁼℃

* subject to increased level of Dark Signal

Exclusions from "The Domain"

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- Specific Exclusions from the Domain:
 - CCDs with fibre-optics
 - CCDs with wavelength conversion coatings
 - Temperature sensors/thermistors
 - Use of flow glass technology
 - Use of conventional LOCOS semiconductor processing
 - Plastic encapsulations
 - Flexible circuit interconnections
 - Gold wire bonding

Manufacturer Line Audit

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- Manufacturer Survey and Line Audit:
 - An in-depth audit of e2v technologies' manufacturing facilities was performed by ESA representatives
 - CCD wafer fabrication,
 - Back-thinning
 - Post processing areas
 - Company quality management system
 - Performed over several visits:
 - November 1999
 - July 2000
 - October 2000
 - Close-out May 2001

Manufacturer Line Audit



- Manufacturer Survey and Line Audit:
 - 145 Line items were recorded:
 - All Action Items closed out successfully

Construction of the Samples

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- The Samples for the Evaluation:
 - Assembled at e2v technologies in Chelmsford, UK,
 - Wafers fabricated in the on-site, dedicated CCD wafer fab.
 - Back-thinned, where applicable (CCD55-20), also in house
- Devices assembled:
 - Defined PID documentation (or controlled deviations)
 - Traveller documentation is used to control and record the build state and history of each item
- Typically 50 of each device type:
 - Electrically and Electro-Optically pre-tested
 - Allocated to the appropriate test groups of the Evaluation
 - Non-conformances not to influence the applicability of any test

Construction of the Samples



- The Samples for the Evaluation : CCD57-10-5-B19
 - Front-Illuminated, Shielded Anti-bloomed. Hermetically Sealed Package



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Construction of the Samples



- The Samples for the Evaluation : CCD55-20-5-B18
 - Back-Illuminated, Enhanced QE, AIMO. Open "MERIS style" Package



The Evaluation Plan e2v technologies The Evaluation Plan: Based on generic ESA principles: **ESA/SCC Generic Specification 9020** Charge Coupled Devices, Silicon, Photosensitive ESA/SCC 2269000 Evaluation Test Programme for **Monolithic Integrated Circuits**

The Evaluation Plan



The Evaluation Plan:

- Silicon Die related tests
 - Irradiation
 - Step-Stress
 - Operating Endurance
 - High Temperature Storage
- Device Assembly related tests
 - Thermal
 - Mechanical
 - Assembly-techniques
 - Package
- Constructional Analysis Performed by ESA
- Control Devices

The Evaluation Plan





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Irradiation Tests - Gamma

- 3 devices of each type tested
- Test performed by Raditec, Harwell
- Cobalt60 source, 1.25Mev gamma; Dose rate ~10kRad/hour
- Doses of 3, 6 and 18 krad(si)
- Cumulative 3, 9 and 27 krad(si)
- Post-Irradiation Anneal, 168hours at 100C (Final stage only)
- Devices biased during irradiation and anneal
- Pre and Post testing at e2v technologies, Chelmsford



Irradiation Tests - Gamma

- Threshold Voltage shifts for both device types as expected:
 - 3-3.5V for 27krad(si); ~120mV/krad(si)
- Bias voltages for Post-Irradiation Electro-Optical test increased to compensate after step 3 and post anneal testing
- Dark signal increases observed for unpinned "surface" component – graphs for CCD55-20 (AIMO) shown at +5C





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Key Results and Observations e2v technologies Irradiation Tests - Gamma Devices do not show significant increases after annealing as has been observed previously, but show some reduction



Dark Signal behaviour for Gamma Irradiation : CCD57-10





Irradiation Tests - Gamma

 The apparent setting of Full Well Capacity vs Vabd bias is subject to change due to the effects of threshold shift on Image clock potentials and not drain bias: Shown for CCD57-10



Full Well Capacity vs Vabd — Pre-Irradiation



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Full Well Capacity vs Vabd — 2nd Irradiation — Gamma

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Full Well Capacity vs Vabd — 3rd Irradiation — Gamma



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Full Well Capacity vs Vabd — Anneal — Gamma



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Irradiation Tests - Proton

- 3 devices of each type tested The CCD57-10 devices were fabricated without permanent windows due to the incompatibility of the window with the proton energy
- Test performed by EBIS lotron, Harwell
- 10MeV protons
- Doses of 3×10^9 , 3×10^9 and 6×10^9 protons/cm²
- 3 x10⁹, 6 x10⁹ and 12 x10⁹ protons/cm²
- Post-Irradiation Anneal, 168hours at 100C (Final stage only)
- Devices un-biased during irradiation and anneal
- Pre and Post testing at e2v technologies, Chelmsford



- Irradiation Tests Proton
 - No significant threshold shift observed
 - e.g. for dark signal and Vabd
 - Bias voltages not adjusted in post testing
 - Dark signal increase in pinned region expected "bulk silicon" contribution – data shown for CCD55-20 at 5C
 - Increase of ~1.5pA/cm2/krad(si) at +20C











Full Well Capacity vs Vabd —3rd Irradiation — Proton



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Irradiation Tests - Proton

- Some loss of CTE occurred as shown by increase in Total CTI test figures (CCD55-20 at 5C)
- Partial recovery observed after anneal



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Step-Stress Tests – Power Stress

- 5 devices
- Step 1 125C for 168 hours, standard biases
- Step 2 125C for 168 hours, Amplifier drain biases +2V
- Step 3 125C for 168 hours, Amplifier drain biases +4V

CCD55-20

- Two devices showed unusual and significant increases in cosmetic image defects/dark signal at step 1
- Confirmed by repeating step 1 on samples from the same wafers
- Other samples passed all 3 steps without catastrophic failures
- Some increase in QE at short wavelengths for devices initially lower than average



Quantum Efficiency – Power Stress : CCD55-20



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Step-Stress Tests – Power Stress

- 5 devices
- Step 1 125C for 168 hours, standard biases
- Step 2 125C for 168 hours, Amplifier drain biases +2V
- Step 3 125C for 168 hours, Amplifier drain biases +4V

CCD57-10

 General dark signal increase and some shift in Full Well Capacity but no catastrophic failures



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Step-Stress Tests – Temperature Stress

- 5 devices + 2 additional samples to check for wafer related degradation as seen on power stress
- Step 1 125C for 168 hours, standard biases
- Step 2 150C for 168 hours, standard biases
- Step 3 175C for 168 hours, standard biases
- CCD55-20
 - Two devices showed unusual and significant increases in image defects/dark signal at step 1. One further device showed unusual and significant increases in image defects/dark signal at steps 2 and 3
 - 1 device failure thought to be due to incorrect connection to biases, but this remains unconfirmed
 - Other samples passed all 3 steps without catastrophic failures
 - Some increase in QE at short wavelengths for devices initially lower than average



- Step-Stress Tests Temperature Stress
 - 5 devices
 - Step 1 125C for 168 hours, standard biases
 - Step 2 150C for 168 hours, standard biases
 - Step 3 175C for 168 hours, standard biases
- CCD57-10
 - Temporary window attachment only:
 - Window sealing process is not compatible with temperatures>125C
 - Significant Dark signal Increase at the higher temperatures
 - 4 devices above specification after the test
 - Variation in the Full Well capacity values
 - Typically 10% reduction



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• Full well capacity – Temperature Stress : CCD57-10



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Operating Endurance Test

- 168 hours at 125C, (equivalent to a typical Class C Burn-in)
- Static biases increased by 2V as agreed following the Power Step Stress testing
- Electrical and Electro-Optical testing.
- 72 hours, 240hours cumulative (equivalent to a typical Class B Burn-in) with the same biases
- Electrical and Electro-Optical testing
- 500 hours cumulative, 1000hours and 2000hours with intermediate Electrical and Electro-Optical testing
- 8 Devices of each type
 - CCD55-20 wafers with image defects/dark signal anomaly were omitted



- Operating Endurance Test
 - CCD55-20
 - No catastrophic failures
 - Some increase in QE at short wavelengths for devices initially lower than average. First period only
 - No significant changes in performance
 - CCD57-10
 - No catastrophic failures
 - Dark signal increase reaches stable level
 - Full well capacity / Anti-blooming set points show drift
 - No significant changes in performance of other parameters



Dark Signal for Operating Endurance : CCD57-10







Full Well Capacity for Operating Endurance : CCD57-10







- Operating Endurance Test Acceleration Factors for +125C
 - Assumed activation energy 0.3eV
 - CCD55-20
 - Acceleration Factor for T_{op} +5C = 43.48
 - 2000 hours equivalent ~ 10 years
 - CCD57-10
 - Acceleration Factor for $T_{op} 30C = 263.6$
 - 2000 hours equivalent ~ 60 years

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High Temperature Storage Test

- 168 hours at 150C
- No applied bias
- Electrical and Electro-Optical testing (CCD55-20 only).
- 500 hours cumulative, 1000hours and 2000hours with intermediate Electrical and Electro-Optical testing
- 5 Devices of each type
 - 3 additional CCD55-20s added to identify wafers with defects in darkness anomaly
 - CCD57-10 were fabricated without permanent windows due to the incompatibility of the window sealing process with the temperature of this test

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- High Temperature Storage Test
 - CCD55-20
 - No catastrophic failures
 - Some increase in QE at short wavelengths for devices initially lower than average – as seen previously
 - One further device identified with the image defects/dark signal anomalous behaviour
 - No significant changes in performance for other parameters
 - CCD57-10
 - No catastrophic failures
 - No significant changes in performance



- Thermal Cycling 5 Devices of each type
 - 100 thermal cycles (10 x 10) between 55C and +125C
 - Mil-STD-883, Method 1010-Condition B (Two chamber)
 - DC tests and electrical leakage current upon completion
 - No significant changes or catastrophic failures
- Constant Acceleration of the Thermally Cycled Devices
 - 5000g Y1 axis only.
 - No apparent degradation of the devices upon inspection
 - CCD57-10s passed the Seal Test after the Constant Acceleration
 - The devices passed the post test DPA
 - Mil-STD-883, Method 1010, Condition D, wirebond pull



Mechanical tests – 5 Devices of each type

- 4 lots of 4 minutes in each of three axis for sine vibration using Mil-STD-883, Method 2007.3, condition B, 50g
- 5 shock pulses in each of six axes for shock using Mil-STD-883, Method 2002.3, condition B, 1,500g, 0.5ms
- Sequence performed 5 times
- DC Electrical test and Visual Inspection as intermediate tests, between each shock and vibration

Constant Acceleration of the Shock and Vibration devices

- 5000g, Y1 axis only
- No apparent degradation of the devices upon inspection
- Device post test DPA
 - Mil-STD-883, Method 1010, Condition D, wirebond pull
 - 1 wire failure noted CCD57-10 no obvious cause

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Mechanical tests

- No failures directly attributed to the Mechanical conditioning.
- Two devices suffered apparent ESD damage
 - Failures of certain DC tests.
 - Control of ESD in the mechanical test area is difficult.
- Two devices became detached from the jig during the test.
 - The devices were progressed through the remaining test sequences and showed no further degradation.
- Damage to devices occurred during loading and unloading of the devices from the shock and vibration jigs,
 - e.g. bent pins or bond wires
 - Temporary windows are removed and replaced for the tests.
- Devices generally acquired a lot of particulate contamination from exposure to the mechanical test area.

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Mechanical tests – CCD55-20 during Vibration



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- Assembly techniques Constant Acceleration
 - 4 Devices of each type
 - Constant Acceleration Mil-STD-883, Method 2001
 - 3,000, 5,000 and 10,000g, in the Y1 direction
 - DC test and Visual Inspection intermediate and end-point test
 - A seal test was performed between each step in addition to that defined for the end test in the Test Plan (CCD57-10 only)
 - Device post test DPA
 - Mil-STD-883, Method 1010, Condition D, wirebond pull
- All devices passed this test without catastrophic failure or apparent degradation (CCD55-20)
 - Some extrusion of window sealing material was observed on CCD57-10 at higher acceleration levels



CCD57-10 Window Seal after 10,000g Constant Acceleration



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- Package Attributes: Terminal Strength, Moisture Resistance and Solderability
- 3 devices of each type
 - Terminal Strength, Mil-STD-883, Method 2004, Condition B2
 - All pins one side of package
 - Moisture Resistance, Mil-STD-883, Method 1004,
 - Devices Unbiased and pre-baked to +50C, 24 hours
 - Solderability, Mil-STD-883, Method 2004, Condition B2
 - Remaining pins other side of package





- ESA Constructional Analysis
 - 3 Devices of each type
 - Mil-STD-883
 - External Visual Inspection, Method 2009.9
 - Physical Dimensions and Weight
 - Radiographic Inspection, Method 2012.6
 - Hermiticity (CCD57-10 only), Method 1014.9
 - (Fine Leak Condition A1/ Gross Leak Condition C1)
 - PIND (CCD57-10 only), Method 2020.7
 - Internal Visual Inspection, Method 2010.10
 - Scanning Electron Microscope (SEM) Inspection, Method 2018.3
 - Focused Ion Beam (FIB) Analysis (Disassembling for CCD55-20)
 - Bond Strength, Method 2011.7
 - Die Shear, Method 2019.5
 - Material Analysis

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ESA Constructional Analysis

- CCD55-20
 - ESA Report CA 0476
 - Suitable for Space Application in General Construction
 - Exception for the Thermistors
 - Failure of destructive wire bond test
- CCD57-10
 - ESA Report CA 0473
 - Manufactured to standards suitable for Space Applications



- Electrical Operating Area and Temperature Characterisation
 - Investigation into the working range of the devices with regard to the applied bias conditions and measurements at high and low temperatures was also performed
 - Details of this are included in the Final Evaluation Test reports
- Evaluation Test Reports
 - CCD57-10, ESA-E2V-RP-009
 - CCD55-20, ESA-E2V-RP-010

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Conclusions - General

- Evaluation programme has been completed successfully
- Both Device Types have been demonstrated as suitable for Space Applications
 - Construction
 - Reliability
 - Stability of Performance
- A Domain has been defined and therefore a baseline has been established from which read-across or delta-evaluations can be performed
- Useful feedback has been obtained to enable the screening of future CCD product to be targeted and effective, and to improve e2v technologies' documentation and procedures

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Conclusions

- CCD55-20
 - Specific problem with generation of excessive image defects was observed on devices from some wafers
 - This would have been identified by screening
 - Use of included parts requires separate attention to qualification
 - e.g. thermistors
 - Handling procedures, even established ones, require constant vigilance and attention to jigging etc.

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Conclusions

- CCD57-10
 - The correct operation and use of the shielded antiblooming capability requires understanding of the impacts of intended environment
 - Irradiation and endurance effects.
 - The "Indalloy" window sealing technique provides a robust and durable hermetic seal
 - Appropriate screening regimes must be applied

Conclusions

e2v technologies therefore commend the evaluated CCD types:

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- CCD57-10 -*-B19, Front-Illuminated
- CCD55-20 -*-C61, Back-illuminated

(equivalent to the CCD55-20 -*-B18 as evaluated

but without thermistors fitted)

for inclusion in the ESA European Preferred Parts List,

 and propose that any e2v technologies CCD demonstrated to be within the defined Domain be considered as evaluated to the conditions of the Evaluation Plan by similarity.

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