Image Sensor Detailed Specification

STAR 250 Detailed Specification

Document history record:

Issue	Date	Description of change
Draft	July 29, 2003	Origination
1.0	Aug. 5, 2003	• Completion of TBDs • Update of Figure 4a and 5b
1.1	Oct. 22, 2003	• Par 4.6.2: Increased high test temperature • Par 5: Increased max temperature and storage temperature
1.2	Jan. 22, 2004	• Par 2, 4.4.1, 4.4.3 updated • Table 1c, 2, 3, 7 updated • Figure 2a and 2b updated
1.3	May 12, 2004	Par 4.4.2: Corrected lead finish material thickness
1.4	Dec. 13, 1004	• Table 1c, 1d, 1e, 1f, 6, 7b, 7c updated • Updated par 4.4.1: thermal resistance • Added Appendix F on observed annealing effects
1.5	May 13, 2005	• Table 1c updated • Par 1.9 “soldering instructions” added • Par. 1.10 updated • Table 1b updated • Par. 4.4.1. Thermal resistance value added
1.6	June 29 2005	• Correction of several typing errors • Par 1.11, 3, 4.1, 4.2 updated • Changed environmental temperature specification to 22±3°C • Table 1c, 1d, 1e, 1f, 4 updated • Added appendix F: observed effects during annealing after total dose irradiation
1.7	Dec 22, 2005	• Added formulas in par 3 • Added par 4.10: LAT and screening • Tables 1c, 1e, 2, 3a, 3b, 4, 6, 7a, 7b, 7c updated
2.0	March 28, 2006	• Tables 1d, 1e and 1f removed • Par 4.10.2 and 4.10.3 removed • Par 4.2 updated • Par. 4.9.2 updated • Table 4 updated • Table 7a, 7b and 7c updated

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1 General

1.1 Scope

This specification details the ratings, physical, geometrical electrical and electro-optical characteristics, test- and inspection-data for a CMOS Active Pixel image Sensor (CMOS APS) based on type STAR250. The sensor has a format of 512 by 512 pixels at 25 μm pitch, and contains on-chip 10-bit ADC

This specification shall be read in conjunction with the ESCC Generic Specification 9020.

1.2 Component type variants

A summary of the type variants of the basic CMOS image sensor is given in Table 1a: “Type variant summary”. The complete list of detailed specifications for each type variant is given in Tables 1c for each type separately.

All specifications in Table 1c are given at 25 ± 3 °C, under nominal clocking and bias conditions. Exceptions are noted in the ‘remarks’ field.

1.3 Maximum rating

The maximum ratings which shall not be exceeded at any time during use or storage are as scheduled in Table 1b.

1.4 Parameter derating information (Figure 1)

Not applicable

1.5 Physical dimensions and geometrical information

The physical dimensions of the assembled component are shown in Figure 2a. The geometrical information in Figure 2b describes the position of the die in the package.

1.6 Pin assignment

Figure 3a contains the pin assignment. The figure contains a schematic drawing and a pin list. A detailed functional description of each pin can be found in Appendix A.

1.7 Timing diagrams

Figure 3b contains the timing diagrams and the timing indications. Appendix B contains a user manual that gives more textual details on how to operate the sensor.

1.8 Functional diagram

Table 3c shows the functional diagram. The user manual in appendix B describes the functionality of the image sensor in more detail.

1.9 Soldering instructions

Soldering is restricted to manual soldering only. No wave or reflow soldering is allowed. For the manual soldering, following restrictions are applicable:

- Solder 1 pin on each of the 4 sides of the sensor
- Cool down period of min. 1 minute before soldering another pin on each of the 4 sides
- Repeat soldering of 1 pin on each side, including a 1 minute cool down period.

1.10 Handling and precautions

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. The following guidelines are applicable:

- Always manipulate the devices in an ESD controlled environment
- Always store the devices in a shielded environment that protects against ESD damage (at least a non-ESD generating tray and a metal bag)
- Always wear a wrist strap when handling the devices and use ESD safe gloves

The STAR250 is classified as class 1A (JEDEC classification – [AD03]) device for ESD sensitivity.

1.11 Storage information

The components must be stored in a dust-free and temperature-, humidity and ESD controlled environment.

The specific storage conditions are:

- Devices must always be stored in special ESD-safe trays such that the glass window is never touched.
- The trays are closed with EDS-safe rubber bands
- The trays are sealed in an ESD-safe conductive foil in clean room conditions.
- For transport and storage outside a clean room the trays are packed in a second ESD-save bag that is sealed in clean room.

2 Applicable documents

The following documents form part of this specification and shall be read in conjunction with it:

Nr	Reference	Title	Issue	Date
AD01	ESCC Generic Specification 9020	Charge Coupled Devices, Silicon,Photosensitive	Rev. C	Feb. 1998
AD02	APS-FF-DU-03-006	Electro-optical test methods for CMOS image sensors	1.1	29 nov 2003
AD03	JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	B	June 2000

Related documents:

Nr	Reference	Title	Issue	Date
AD01	ESCC Generic Specification 9020	Charge Coupled Devices, Silicon,Photosensitive	Rev. C	Feb. 1998

3 Terms, Definitions Abbreviations, Symbols and Units

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC basic Specification 21300 shall apply.

In addition the following table contains terms that are specific to CMOS image sensors and are not listed in ESCC21300

Symbol	Parameter
INL	**ADC integral non linearity**
DNL	**ADC differential non-linearity**
FPN	**Fixed pattern noise**

The following formulas are applicable to convert %Vsat and mV/s into e- and e-/s:

- $$FPN[e-] = \frac{FPN[\%Vsat] * \overline{Vsat}}{conversion\_gain}$$
- $$Dark\_signal[e-/s] = \frac{Dark\_signal[V/s]}{conversion\_gain}$$
- $$DSNU[e-] = \frac{DSNU[\%Vsat] * \overline{Vsat}}{conversion\_gain}$$
- Conversion gain for STAR250: 5,7 µV/e-

4 Requirements

4.1 General

At this stage of the evaluation, the requirements for the procurement of the components specified herein are not finalized. These requirements will be based upon the ESCC Generic specification No 9020 for Charge Coupled Devices.

4.2 Deviations from generic specification

Lot acceptance and screening are based on ESCC 9020. Par. 4.10 describes the lot acceptance and screening.

4.3 Mechanical requirements

4.3.1 Dimension check

The dimensions of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 2a.

4.3.2 Geometrical characteristics

The geometrical characteristics of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 2b.

4.3.3 Weight

The maximum weight of the components specified herein shall be as specified in Table 1c, item 5.

4.4 Materials and finishes

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used.

4.4.1 Case

The case shall be hermetically sealed and have a ceramic body and a glass window.

Type	JLCC-84
Material:	Black Alumina BA-914
Thermal expansion coefficient	7.6 x 10^{-6} /K
Hermeticity	< 5 x 10E-7 atm cc/s
Thermal resistance	Appr. 5,1 ºC/W

4.4.2 Lead material and finish

Lead material	KOVAR
1e Finish	Nickel, min 2 µm
2^{nd} Finish	Gold, min 1.5 µm

4.4.3 Window

The window material shall be BK7G18 with anti-reflective coating applied on both sides.

The optical quality of the glass shall have the following specification:

Scratch max dimension	<=10 µm
Scratch max number	5
Dig max dimension	<=60 µm
Dig max number	25

The anti reflective coating shall have a reflection coefficient < 1.3% absolute and < 0.8% on average, over a bandwidth from 440 nm to 1100 nm (TBC).

4.5 Marking

4.5.1 General

The marking shall consist of a lead identification and traceability information.

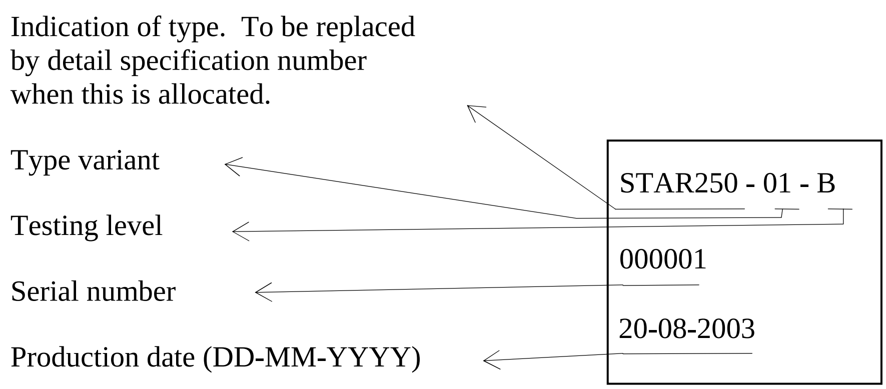
4.5.2 Lead identification

An index to pin 1 shall be located on the top of the package in the position defined in Note 1 to Figure 2a. The pin numbering is clock-wise, when looking at the top-side of the component.

4.5.3 Traceability information

Each component shall be marked such that complete traceability can be maintained.

The component shall bear a number that is constituted as follows:



4.6 Electrical and electro-optical measurements

4.6.1 Electrical and electro-optical measurements at reference temperature

The parameters to be measured to verify the electrical and electro-optical specifications are scheduled in Table2. Unless otherwise specified, the measurements shall be performed at a environmental temperature of 22±3°C.

For all measurements the nominal power supply, bias and clocking conditions apply. The nominal power supply and bias conditions are given in Figure 4a, the timing diagrams in Figure 3b.

Remark: The given bias and power supply settings imply that the devices are measured in “soft-reset” condition.

4.6.2 Electrical and electro-optical measurements at high and low temperature

The parameters to be measured to verify the electrical and electro-optical specifications are scheduled in Table 3. Unless otherwise specified, the measurements shall be performed at -40 (-5 +0) °C and at +85 (+5 -0) °C.

4.6.3 Circuits for electrical and electro-optical measurements

Circuits for performing the electro-optical tests in Table 2 are shown in Figure 4.

4.7 Burn-in test

4.7.1 Parameter drift values

The parameter drift values for power burn-in are specified in Table 4 of this specification. Unless otherwise specified the measurements shall be conducted at environmental temperature of 22±3°C and under nominal power supply, bias and timing conditions.

The limit values of any parameter -as indicated in Table 2- shall not be exceeded.

4.7.2 Conditions for high temperature reverse bias burn-in

Not Applicable

4.7.3 Conditions for power burn-in

The conditions for power burn-in shall be as specified in Table 5b of this specification

4.7.4 Electrical circuits for high temperature reverse bias burn-in

Not applicable

4.7.5 Electrical circuits for power burn-in

Circuits to perform the power burn-in test are shown in Figure 5b of this specification.

4.8 Environmental and endurance tests

4.8.1 Electrical and electro-optical measurements on completion of environmental test

The parameters to be measured on completion of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at environmental temperature of 22±3°C. Measurements of dark current must be performed at 22±1°C and the actual environmental temperature must be reported with the test results.

4.8.2 Electrical and electro-optical measurements at intermediate point during endurance test

The parameters to be measured at intermediate points during endurance test of environmental tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at environmental temperature of 22±3°C

4.8.3 Electrical and electro-optical measurements on completion of endurance test

The parameters to be measured on completion of endurance tests are scheduled in Table 6. Unless otherwise stated, the measurements shall be performed at environmental temperature of 22±3°C

4.8.4 Conditions for operating life test

The conditions for operating life tests shall be as specified in Table 5b of this specification.

4.8.5 Electrical circuits for operating life test

Circuits for performing the operating life test are shown in figure 5b of this specification.

4.8.6 Conditions for high temperature storage test

The temperature to be applied shall be the maximum storage temperature specified in Table 1b of this specification.

4.9 Total dose radiation test

4.9.1 Application

The total dose radiation test shall be performed in accordance with the requirements of ESCC Basic specification 22900

4.9.2 Parameter drift values

The allowable parameter drift values after total dose irradiation are listed in Table 4. The parameters shown are valid after a total dose of 250Krad and 168h/100°C annealing.

4.9.3 Bias conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 6 of this specification.

4.9.4 Electrical and electro-optical measurements

The parameters to be measured, prior to, during and on completion of the irradiation are listed in Table 7 of this specification. Only devices that meet the specification in Table 1 of this specification shall be included in the test sample.

4.10 Lot acceptance and screening

This document describes the LAT and screening on the STAR250FM devices.

All tests on device level have to be performed on screened devices.

4.10.1 Wafer lot acceptance

This is the acceptance of the silicon wafer lot. This has to be done on every wafer lot with STAR250 and STAR1000 always being separated lots.

Test	Test method	Nr of devices	Test condition	Test location
Wafer processing data	PID	NA	NA	CY
SEM	ESCC 21400	4 naked dies	NA	IGG
Total dose test	ESCC 22900	3 devices	100 krad	ESTEC by CY
Endurance test	PID	6 devices	2000h - +125C	IGG

Before and after total dose test and endurance test:

- Electrical measurements before and after
- Visual inspection before and after
- EO measurements before and after

4.10.2 Assembly lot acceptance

Test	Test method	Number of devices	Test condition	Test location
Special MPD in process control				MPD
Bond strength test	MIL-STD-883 method 2011	2	D	MPD
MPD Geometrical data review	Review	All		CY
Solderability Terminal strength Marking permanence	MIL-STD883, method 2003 MIL-STD 883, Method 2004 ESCC 24800	2	 D	IGG
Geometrical measurements Temperature cycling	PID MIL-STD 883, method 1010	4	 10 cycles - 55/+120	CY IGG
Thermal shock Moisture resistance RGA	MIL-STD 883 method 1011 MIL-STD-883, method 1004 MIL-STD 883, method 1018.3	4	B - 15 shocks - 55/+120 Procedure 1	IGG IGG ORS

Before and after the following tests are done:

- Electrical measurements
- Visual inspection
- Fine leak test
- Gross leak test

4.10.3 Periodic testing

Test	Test method	Number of devices	Test condition	Test location
Mechanical shock	MIL-STD 883, method 2002	2	B - 5 shocks, 1500g – 0,5ms – ½ sine, 3 axes	De Nayer lab
Vibration	MIL-STD 883, Method 2007	2	A - 4 sweeps, 20g 80 to 2000 Hz, 0,06 inch 20 to 80 Hz.	De Nayer lab
Constant acceleration	MIL-STD 883, Method 2001	2	D	De Nayer lab

Before and after the following tests are done:

- Electrical measurements
- Visual inspection
- Fine leak test
- Gross leak test

4.10.4 Screening

Test	Test method	Number of devices	Test condition	Test location
Xray		All		IGG
PIND	MIL-STD-883 method 2020	All	A	IGG
Stabilization bake	MIL-STD-883 method 1008	All	48h at 85C.	IGG
Visual inspection	PID	All		CY
RT Electrical measurements	PID	All		CY
Temperature cycling	MIL-STD-883 method 1010	All	B - 10 cycles - 40/+85	IGG
RT Electrical measurements	PID	All		CY
Burn-in	PID	All	240h at +85C.	IGG
Electrical measurements HT/LT/RT	PID	All	HT +85 C LT -40 C	CY
Fine leak test	MIL-STD-883 method 1014	All	Read and record.	IGG
Gross leak test	MIL-STD-883 method 1014		Perfluorocarbon test	IGG
Visual inspection	PID	All		CY

5 Tables and figures

Table 1a: Type variant summary

Variant	Number of FPN defects	Number of DSNU defects	Number of PRNU defects
01	0	0	0

Table 1b: Maximum ratings

No	Characteristics	Symbol	Limits		Units	Remarks
			Min	Max		
1	Any supply voltage		-0.5	+7	V	
2	Voltage on any input terminal		-0.5	Vdd + 0.5	V	
3	Operating temperature		-40	+85	°C	
4	Storage temperature (momentarily)		-40	+120	°C	Not longer than 1 hour.
5	Storage temperature (long term)		-40	+85	°C	
6	Soldering temperature		NA	260	°C	Hand soldering only; see par.1.9 for soldering instructions

Table 1c: Detailed specification
All type variants

Design specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
1	Image sensor format		512 by 512 pixels				
2	Pixel size		25 by 25			µm	
3	ADC resolution		10 bit				
3b	Timing diagram		Figure 3b				

Mechanical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
4a	Flatness of image area		NA	NA	10	µm	Peak-to-peak at 25 ± 3 °C
4b	Total tickness		2.7	2.8	2.9	mm	Package + epoxy + glass lid
4c	Die position, X offset		-0.05	0	0.05	mm	
4d	Die position, Y offset		-0.032	0.068	0.168	mm	
4e	Die position, parallelism		-0.05	0	0.05	mm	
4f	Die position, Y tilt		-0.05	0	0.05	mm	
5	Weight		6.2	6.45	6.7	g	

Window specifications

No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
6	Spectral range for optical coating of window		440	NA	1100	nm	To be confirmed by window manufacturer
7	Reflection coefficient for window		NA	< 0.8	< 1.3	%	Over bandwidth indicated in 6
8	Optical quality: Scratch max width Scratch max number Dig max size Dig max number		NA	NA	 10 5 60 25	 µm µm	

Environmental specifications

No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
9	Operating temperature range		-40	NA	+85	°C	
10	Total dose radiation tolerance		230	NA	NA	Krad (Si)	Device still operating to specification in Table 1d
11	Equivalent proton fluence		3.10^{10}	NA	NA	Proton/cm^2	Proton energy: 10MeV Device still operating to specification in Table 1e
12	SEL threshold		28	NA	NA	MeV cm^3 mg^{-1}	Device still operating to specification in Table 1f

Electrical specifications

No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
13	Total power supply current stand-by		NA	67.1	70.2	mA	Under nominal bias conditions and at nominal pixel rate
14	Total power supply current, operational		NA	73.1	75.9	mA	Under nominal bias conditions and at nominal pixel rate
15	Power supply current to ADC, operational		NA	47.7	49.8	mA	Under nominal bias conditions and at nominal pixel rate
16	Power supply current to image core, operational		NA	25.3	27.20	mA	Under nominal bias conditions and at nominal pixel rate
17	Input impedance digital input		200	NA	NA	KΩ	
18	Input impedance Dark Reference input		200	NA	NA	KΩ	

Electrical specifications							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
19	Input impedance ADC input		200	NA	NA	KΩ	
20	Output impedance digital outputs		NA	NA	100	Ω	Note[1]
21	Output impedance analogue output		NA	NA	100	Ω	Note 1
22	Output amplifier voltage range		0.5	NA	4.5	V	Under nominal power supply and bias conditions, at 22 ± 3 °C
23	Dark reference offset		NA	0.5	0.7	V	Note [2]
25	Output amplifier gain setting 1		2.25	2.30	2,36		Note [3]
26	Output amplifier gain setting 2		4,28	4,43	4,57		Note 3
27	Output amplifier gain setting 3		7.95	8,27	8.55		Note 3
28	ADC ladder network resistance		1066	1206	1346	Ω	at 25 ± 3 °C
28a	ADC ladder network temperature coefficient			4,6		Ω/°C	Between -40°C and +85°C
29	ADC Differential non linearity		NA	3.1	5.8	LSB	
30	ADC Integral non linearity		NA	1,4	1,8	LSB	
31	ADC set-up time		NA	NA	250	ns	To reach 1% conversion accuray
32	ADC delay time		NA	NA	72	ns	

Electro-optical specifications							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
33	Saturation voltage output		1.55	1,78	NA	V	
34	Linear range			128		Ke-	Within ±1% Note [4]
36	Full well charge			311		Ke-	Note 4

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[1] Output impedance is specified under quasi-static conditions. During transients the output amplifier enters in current-limited mode and the output impedance increases, depending on the capacitive load of the external circuits.
[2] Dark reference offset specifies the offset between the applied dark reference voltage and the actual level at the analogue output terminal. Specified at gain setting 0.
[3] Gain specification relative to gain setting 0.
[4] Full well charge and linear range are calculated from detailed electro-optical response measurements.. At this time not enough measurements are available for reliable determination of the minimum and maximum values.

Electro-optical specifications

No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
37	Quantum efficiency x Fillfactor			35	NA	%	Between 450 nm and 750 nm. Refer to appendix C for complete curve
38	Responsivity narrow band blue		24300	26800	NA	ADU	At 475 nm ±20 nm
39	Responsivity narrow band green		24100	26300	NA	ADU	At 526 nm ±20 nm
40	Responsivity, narrow band red		20600	24300	NA	ADU	At 630 nm ±20 nm
41	Charge to voltage conversion factor			5.7		µV/e-	Note [5]
42	Temporal noise, nominal clock rate		NA	0.86	1.35	mV	At 22 ± 3 °C and 5 MHz clock rate
43	Temporal noise, reduced clock rate		NA	0.90	1.57	mV	At 22 ± 3 °C and 2 MHz clock rate.
44	Temporal noise, enhanced clock rate		NA	6.51	29.7	mV	At 22 ± 3 °C and 10 MHz clock rate
45	Local fixed pattern noise standard deviation, nominal clock rate		NA	0.05	0.08	%Vsat	Note [6] At22 ± 3 °C and 5 MHz clock rate
46	Global fixed pattern noise standard deviation, nominal clock rate		NA	0.23	0.43	%Vsat	Note [7] At 22 ± 3 °C and 5 MHz clock rate
47	Local fixed pattern noise standard deviation, reduced clock rate		NA	0.06	0.08	%Vsat	Note [8] At 22 ± 3 °C and 2 MHz clock rate
48	Global fixed pattern noise standard deviation, reduced clock rate		NA	0.26	0.36	%Vsat	Note At 22 ± 3 °C and 2 MHz clock rate [9]
49	Local fixed pattern noise standard deviation, enhanced clock rate		NA	0.10	0.38	%Vsat	At 22 ± 3 °C and 10 MHz clock rate

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[5] Charge to voltage conversion factor is calculated from the detailed electro-optical response measurements.. At this time not enough measurements are available for reliable determination of the minimum and maximum values.

[6] Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.

[7] Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

[8] Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.

[9] Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

Electro-optical specifications							
No	Characteristics	Symbol	Limits			Units	Remarks
			Min	Typ	Max		
50	Global fixed pattern noise standard deviation, enhanced clock rate		NA	0.31	0.73	%Vsat	At22 ± 3 °C and 10 MHz clock rate
51	Number of FPN signal defects	Ndef1	See Table 1a: type variant summary				
52	FPN limit for Ndef1		15			%	
53	Column FPN		NA	0.23	0.32	%Vsat	At 22 ± 3 °C.
54	Average dark signal		NA	35	76	mV/s	At 22 ± 1 °C,
55	Dark signal temperature dependency		NA	9.2	NA	°C	Specification indicates temperature rise for doubling average dark current.
56	Local dark signal non uniformity standard deviation		NA	0.98	1.34	%Vsat	At 22 ± 1 °C.
57	Global dark signal non uniformity standard deviation		NA	1.22	1.63	%Vsat	At 22 ± 1 °C
58	Number of DSNU signal defects		See Table 1a: type variant summary				
59	DSNU limit for Ndef1		15			%	
60	Local photo response non uniformity, standard deviation		NA	0,49	0.59	%	Note [10]
61	Global photo response non uniformity, standard deviation		NA	1.65	2.97	%	Note [11]
62	Number of PRNU defects		See Table 1a: type variant summary				
63	PRNU limit for Ndef1		15			%	Note 11
64	MTF X direction			0.36	NA		Note[12]
65	MTF Y direction			0.39	NA		Note [13]
66	Pixel to pixel cross talk X direction		NA	16		%	Note [14]

[10] Percentage of signal (black offset subtracted), measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window PRNUs.

[11] Percentage of signal (black offset subtracted),, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

[12] MTF is calculated from the detailed electro-optical response measurements.. At this time not enough measurements are available for reliable determination of the minimum and maximum values.

[13] Measurements based on a limited number of samples. Only typical values are available

[14] Pixel to pixel optical crosstalk in % of charge in illuminated pixel.

Electro-optical specifications							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
67	Pixel to pixel cross talk Y direction		NA	16		%	Note 14
68	Anti-blooming capability		NA	X1000	NA		Anti-blooming is not relevant for CMOS image sensors.

The pixel-to-pixel crosstalk is calculated from the MTF measurement. At this moment not enough measurements are available to define the minimum and maximum values.

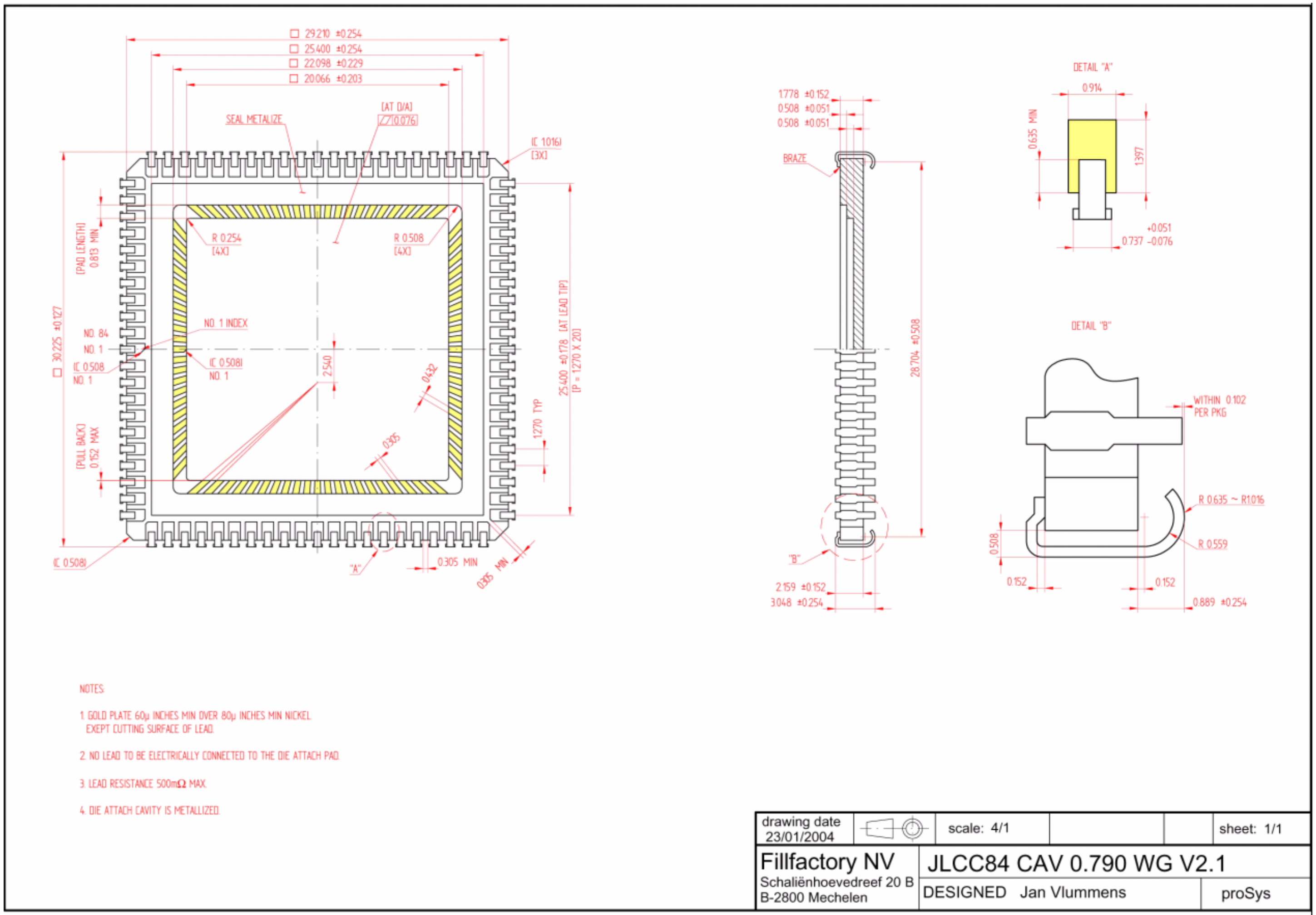


Figure 2a:Physical dimensions

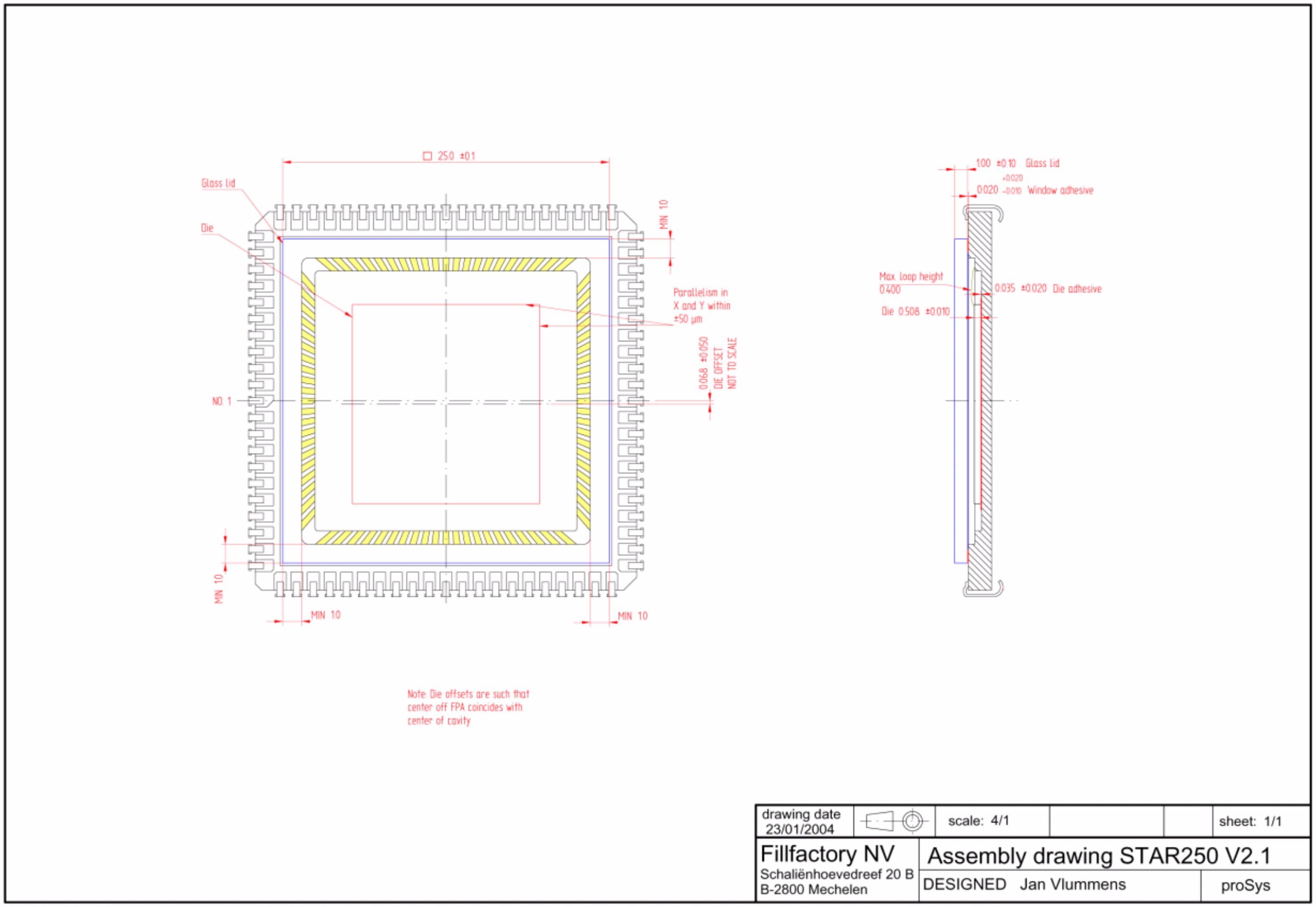


Figure 2b: Geometrical characteristics

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	S	22	SYNC_YL	43	OUT	64	D9
2	R	23	EOS_YL	44	IN_ADC	65	GND_ADC_ANA
3	RESET	24	CLK_X	45	NBIASANA2	66	VDD_ADC_ANA
4	SELECT	25	SYNC_X	46	NBIASANA	67	VDD_ADC_DIG
5	L/R	26	EOS_X	47	VLOW_ADC	68	GND_ADC_DIG
6	A0	27	CLK_YR	48	G_AB	69	VDD_ADC_DIG_3.3/5
7	A1	28	SYNC_YR	49	VDD_RESR	70	VHIGH_ADC
8	A2	29	EOS_YR	50	VDD_DIG	71	CLK_ADC
9	GND_ANA	30	GND_AMP	51	GND_DIG	72	PBIASDIG2
10	VDD_ANA	31	VDD_AMP	52	VDD_PIX	73	PBIASENCLOAD
11	VDD_DIG	32	GND_DIG	53	VDD_ADC_ANA	74	PBIASDIG1
12	GND_DIG	33	VDD_DIG	54	GND_ADC_ANA	75	BITINVERT
13	A3	34	VDD_ANA	55	D0	76	VDD_PIX
14	A4	35	GND_ANA	56	D1	77	GND_DIG
15	A5	36	CAL	57	D2	78	VDD_DIG
16	A6	37	G0	58	D3	79	VDD_RESL
17	A7	38	G1	59	D4	80	TRI_ADC
18	A8	39	NBIASARR	60	D5	81	TESTDIODE
19	LD_Y	40	PBIAS	61	D6	82	TESTPIXELARRAY
20	LD_X	41	NBIAS_AMP	62	D7	83	TESTPIXEL_RESET
21	CLK_YL	42	BLACKREF	63	D8	84	TESTPIXEL_OUT

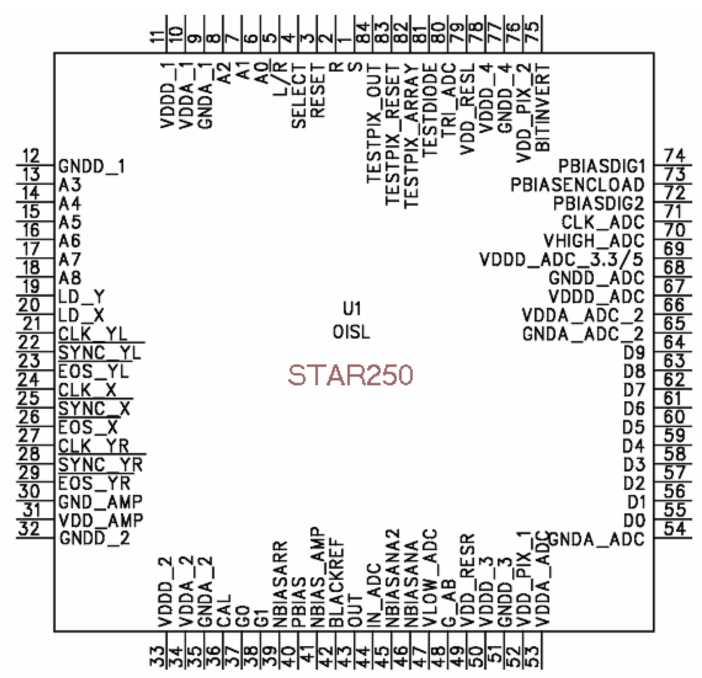


Figure 3a: Pin assignment

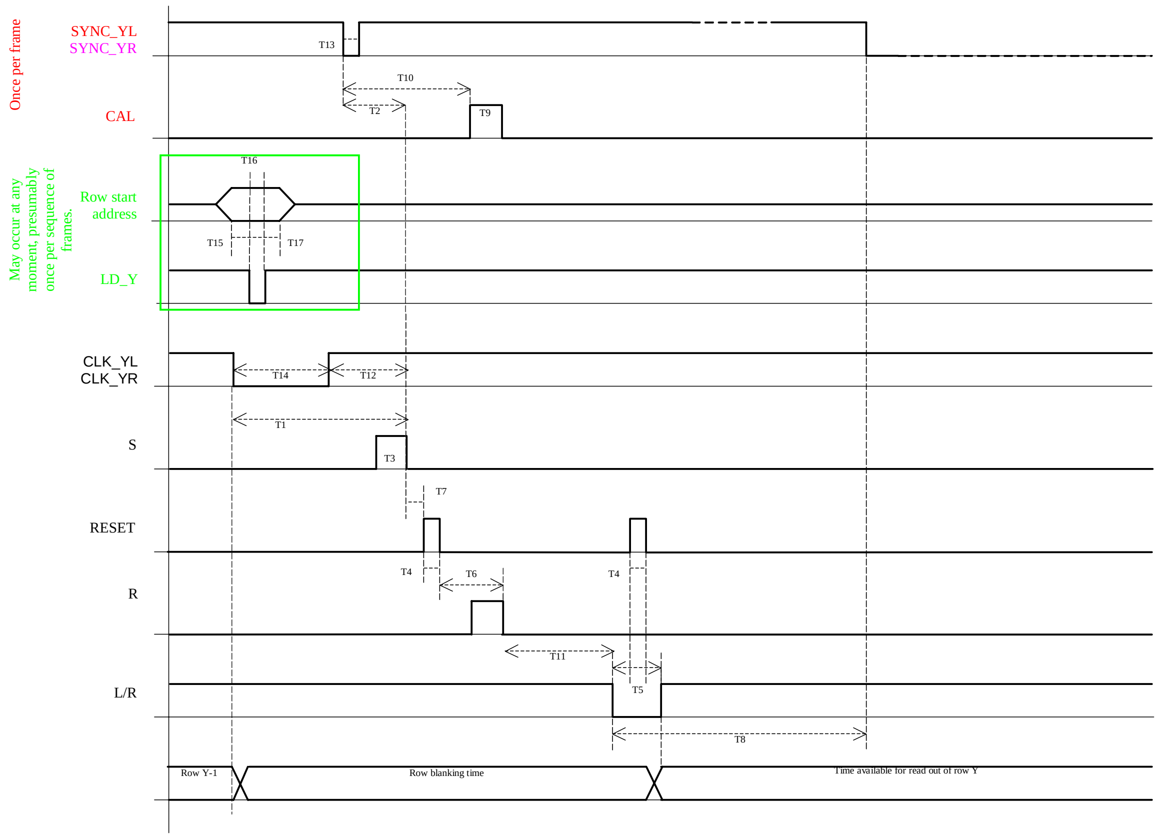


Figure 3b1: Timing diagram: Reset and line-read-out timing

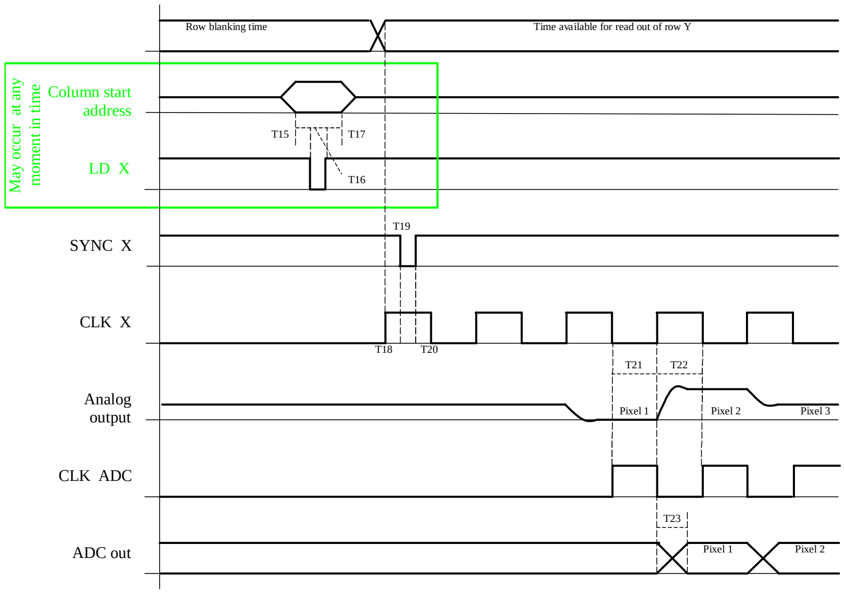


Figure 3b2: Timing diagram: Pixel read-out timing

Symbol	Min	Typ	Description
T1	1.8 µs		Delay between selection of new row by falling edge on CLK_YL and falling edge on S. Minimal value. Normally, CLK_YR should be low already at the end of the previous sequence.
T2	1.8 µs		Delay between selection of new a row by SYNC_YL and falling edge on S.
T3	0.4 µs		Duration of S and R pulse.
T4	0.1 µs		Duration of RESET pulse.
T5	T4 + 40 ns	0.3 µs	L/R pulse must overlap second RESET pulse at both sides.
T6	0.8 µs		Delay between falling edge on RESET and falling edge on R.
T7	20 ns	0.1 µs	Delay between falling edge on S and rising edge on RESET.
T8	0	1 µs	Delay between falling edge on L/R and falling edge on CLK_Y.
T9	100 ns	1 µs	Duration of cal pulse. The CAL pulse is given once each frame.
T10	0	2 µs	Delay between falling edge of SYNC_YL and rising edge of CAL pulse.
T11	40 ns	0.1 µs	Delay between falling edge on R and rising edge on L/R.
T12	0.1 µs	1 µs	Delay between rising edge of CLK_Y and falling edge on S.
T13		0.5 µs	Pulse width SYNC_YL / YR
T14		0.5 µs	Pulse width CLK_YL / YR
T15	10 ns		Address set-up time
T16	20 ns		Load X / Y start register value
T17	10 ns		Address stable after load
T18	10 ns		
T19	20 ns		SYNC_X pulse width. SYNC_X while CLK_X is high.
T20	10 ns		
T21		40 ns	Analogue output is stable during CLK_X low.
T22		40 ns	CLK_X pulse width: During this clock phase the analogue output ramps to the next pixel level.
T23		125 ns	ADC digital output stable after falling edge of CLK_ADC

Figure 3b3: Timing diagram: Timing specifications

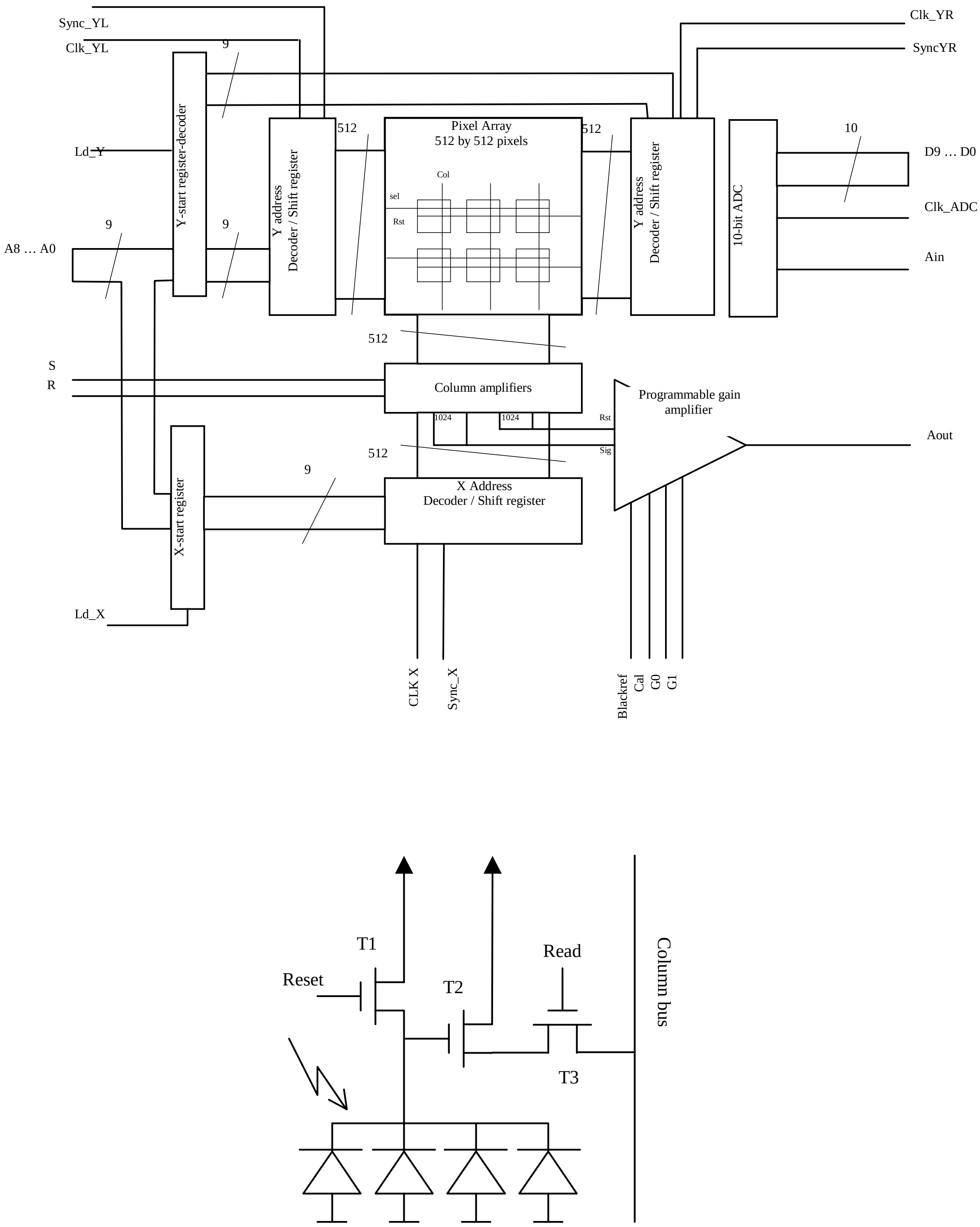


Figure 3c: functional diagram

Table 2: Electrical and electro-optical measurements at reference temperature

The limits in this table set the acceptance criteria for procurement of samples.

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
0	Contact test, ESD input structures			No fail	No fail	
13	Total power supply current stand-by			NA	69.6	mA
14	Total PS current, operational			NA	75.3	mA
15	PS current ADC, operational			NA	49.4	mA
16	PS current to image core, operational			NA	26.7	A
23	Offset 0			-100	100	mV
25	Output amplifier gain setting 1			2.26	2.36	
26	Output amplifier gain setting 2			4.31	4.58	
27	Output amplifier gain setting 3			8.01	8.63	
28	ADC ladder network resistance			1094	1318	Ω
29	ADC Differential non linearity			NA	5.26	LSB
30	ADC Integral non linearity			NA	1.75	LSB
33	Saturation voltage output			1.6	NA	V
38	Responsivity narrow band blue			25000	NA	ADU
39	Responsivity narrow band green			24700	NA	ADU
40	Responsivity, narrow band red			21300	NA	ADU
42	Temporal noise, nom. clock frequency			NA	1.25	mV
43	Temporal noise, red. clock frequency			NA	1.44	mV
44	Temporal noise, enhanced clock freq.			NA	25.0	mV
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.09	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.40	%Vsat
47	Local fixed pattern noise standard deviation, reduced clock frequency			NA	0.09	%Vsat
48	Global fixed pattern noise standard deviation, reduced clock frequency			NA	0.50	%Vsat
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	0.38	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	0.66	%Vsat
51	Number of FPN signal defects			NA	table 1a	
53	Column FPN			NA	0.39	%Vsat
54	Average dark signal			NA	68	mV/s
56	Local DSNU standard deviation			NA	1.38	%Vsat
57	Global DSNU standard deviation			NA	1.66	%Vsat
58	Number of DSNU signal defects			NA	table 1a	
60	Local PRNU, standard deviation			NA	0.65	%
61	Global PRNU, standard deviation			NA	3.73	%
62	Number of PRNU defects			NA	table 1a	

Table 3a: Electrical and Electro-optical measurements at high temperature

	Characteristics	**Symbol**	**Test condition**	**Limit min**	**Limit max**	**Unit**
13	Total power supply current stand-by			NA	66.2	mA
14	Total PS current, operational			NA	71.5	mA
15	PS current ADC, operational			NA	47.8	mA
16	PS current to image core, operational			NA	24.8	A
28	ADC ladder network resistance			1338	1611	Ω
33	Saturation voltage output			1.6	NA	V
38	Responsivity narrow band blue			24600	NA	ADU
39	Responsivity narrow band green			24400	NA	ADU
40	Responsivity, narrow band red			21000	NA	ADU
44	Temporal noise, enhanced clock freq.			NA	75.0	mV
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	1.09	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	2.84	%Vsat
54	Average dark signal			NA	68	mV/s
56	Local DSNU standard deviation			NA	1.38	%Vsat
57	Global DSNU standard deviation			NA	4.17	%Vsat
58	Number of DSNU signal defects			NA	NA	
60	Local PRNU, standard deviation			NA	1.03	%
61	Global PRNU, standard deviation			NA	3.84	%
62	Number of PRNU defects			NA	table 1a	

Table 3b: Electrical and Electro-optical measurements at low temperature

	Characteristics	**Symbol**	**Test condition**	**Limit min**	**Limit max**	**Unit**
13	Total power supply current stand-by			NA	73.3	mA
14	Total PS current, operational			NA	81.5	mA
15	PS current ADC, operational			NA	52.2	mA
16	PS current to image core, operational			NA	29.9	A
28	ADC ladder network resistance			811	990	Ω
33	Saturation voltage output			1.6	NA	V
38	Responsivity narrow band blue			27000	NA	ADU
39	Responsivity narrow band green			26600	NA	ADU
40	Responsivity, narrow band red			21600	NA	ADU
44	Temporal noise, enhanced clock freq.			NA	2.5	mV
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	0.09	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	0.40	%Vsat
54	Average dark signal			NA	NA	mV/s
56	Local DSNU standard deviation			NA	NA	%Vsat
57	Global DSNU standard deviation			NA	NA	%Vsat
58	Number of DSNU signal defects			NA	NA	
60	Local PRNU, standard deviation			NA	0.85	%
61	Global PRNU, standard deviation			NA	4.11	%
62	Number of PRNU defects			NA	table 1a	

Table 4a: Parameter drift values for burn in

The min and max limits of table 2 apply

Table 4b: Parameter drift values for radiation testing

Total dose radiation drift values							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
54	Average dark signal rise		NA	250	600	e-/s per Krad	At 22 ± 1 °C,
56	Local dark signal non uniformity rise		NA	47	96	e-/s per Krad	At 22 ± 1 °C
57	Global dark signal non uniformity rise		NA	58	119	e-/s per Krad	At 22 ± 1 °C

proton radiation drift values							
No	**Characteristics**	**Symbol**	**Limits**			**Units**	**Remarks**
			Min	**Typ**	**Max**		
54	Average dark signal rise		NA	4700		e-/s	At 22 ± 1 °C, 1E11 protons of 60MeV

Table 5a: Conditions for high temperature reverse bias burn-in

No	**Characteristics**	**Symbol**	**Test condition**	**Unit**
Not applicable				

Table 5b: Conditions for power burn-in and operating life tests

No	**Characteristics**	**Symbol**	**Test condition**	**Unit**
1	Ambient temperature	Tamb	85	°C
2	All power supplies	Vdd	+5.5	V
3	Bias conditions		See Figure 5b	
4	X clock frequency		5	MHz

Table 6: Electrical and electro-optical measurements on completion of environmental tests and at intermediate points and on completion of endurance testing

	Characteristics	**Symbol**	**Test condition**	**Limit min**	**Limit max**	**Unit**
0	Contact test, ESD input structures			No fail	No fail	
13	Total power supply current stand-by			NA	69.6	mA
14	Total PS current, operational			NA	75.3	mA
15	PS current ADC, operational			NA	49.4	mA
16	PS current to image core, operational			NA	26.7	A
23	Dark reference offset			-100	100	mV
25	Output amplifier gain setting 1			2.26	2.36	
26	Output amplifier gain setting 2			4.31	4.58	
27	Output amplifier gain setting 3			8.01	8.63	
28	ADC ladder network resistance			1094	1318	Ω

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
29	ADC Differential non linearity			NA	5.26	LSB
30	ADC Integral non linearity			NA	1.75	LSB
33	Saturation voltage output			1.6	NA	V
38	Responsivity narrow band blue			25000	NA	ADU
39	Responsivity narrow band green			24700	NA	ADU
40	Responsivity, narrow band red			21300	NA	ADU
42	Temporal noise, nom. clock frequency			NA	1.25	mV
43	Temporal noise, red. clock frequency			NA	1.44	mV
44	Temporal noise, enhanced clock freq.			NA	25.0	mV
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.09	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.40	%Vsat
47	Local fixed pattern noise standard deviation, reduced clock frequency			NA	0.09	%Vsat
48	Global fixed pattern noise standard deviation, reduced clock frequency			NA	0.50	%Vsat
49	Local fixed pattern noise standard deviation, enhanced clock frequency			NA	0.38	%Vsat
50	Global fixed pattern noise standard deviation, enhanced clock frequency			NA	0.66	%Vsat
51	Number of FPN signal defects			NA	table 1a	
53	Column FPN			NA	0.39	%Vsat
54	Average dark signal			NA	68	mV/s
56	Local DSNU standard deviation			NA	1.38	%Vsat
57	Global DSNU standard deviation			NA	1.66	%Vsat
58	Number of DSNU signal defects			NA	table 1a	
60	Local PRNU, standard deviation			NA	0.65	%
61	Global PRNU, standard deviation			NA	3.73	%
62	Number of PRNU defects			NA	table 1a	

Table 7a: Electrical and electro-optical measurements during and on completion of total-dose irradiation testing

	Characteristics	Symbol	Test condition	Limit min	Limit max	Unit
13	Total power supply current stand-by			NA	69.6	mA
14	Total PS current, operational			NA	75.3	mA
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.09	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.40	%Vsat
51	Number of FPN signal defects			NA	table 1a	
54	Average dark signal			NA	Table 4	e-/s
56	Local DSNU standard deviation			NA	Table 4	e-
57	Global DSNU standard deviation			NA	Table 4	e-

Table 7b:

Electrical and electro-optical measurements during and on completion of proton irradiation testing

Proton irradiation is performed with 1E11 protons at an energy of 60 MeV

	Characteristics	**Symbol**	**Test condition**	**Limit min**	**Limit max**	**Unit**
13	Total power supply current stand-by			NA	69.6	mA
14	Total PS current, operational			NA	75.3	mA
45	Local fixed pattern noise standard deviation, nominal clock frequency			NA	0.09	%Vsat
46	Global fixed pattern noise standard deviation, nominal clock frequency			NA	0.40	%Vsat
51	Number of FPN signal defects			NA	table 1a	
54	Average dark signal			NA	table 4	

Table 7c: Electrical and electro-optical measurements during and on completion of heavy ion irradiation testing

During heavy ion testing no specific tests or measurement are executed. Instead the image sensors are operated at nominal speed and power supply current is monitored.

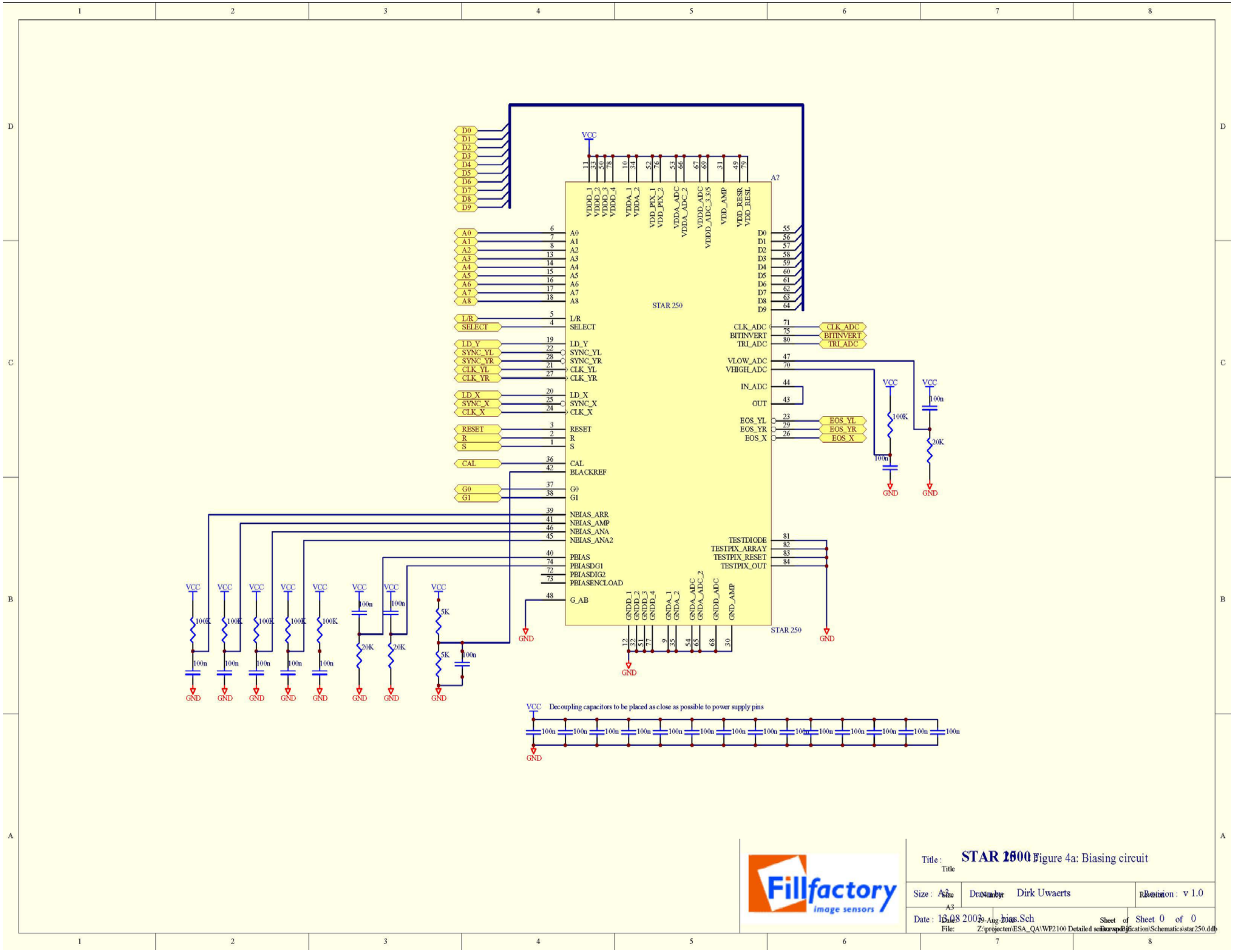
Heavy ion irradiation testing is performed up to a total dose of 10E7 particles with an effective LET of 127.8 MeV/mg/cm2**.**

	Characteristics	**Symbol**	**Test condition**	**Limit min**	**Limit max**	**Unit**
13	Total power supply current stand-by			NA	69.6	mA
14	Total PS current, operational			NA	75.3	mA

Not applicable

Figure 1: Parameter derating information

Figure 4: Circuits and diagrams for electrical and electro-optical measurements



STAR 250
Decoupling capacitors to be placed as close as possible to power supply pins
Title : STAR 2500 Figure 4a: Biasing circuit
Size : A3
Drawn by: Dirk Uwaerts
Revision : v 1.0
Date : 13.08.2003
bias.Sch
Sheet 0 of 0

Not applicable

Figure 5a: Electrical circuit for high temperature reverse bias burn-in

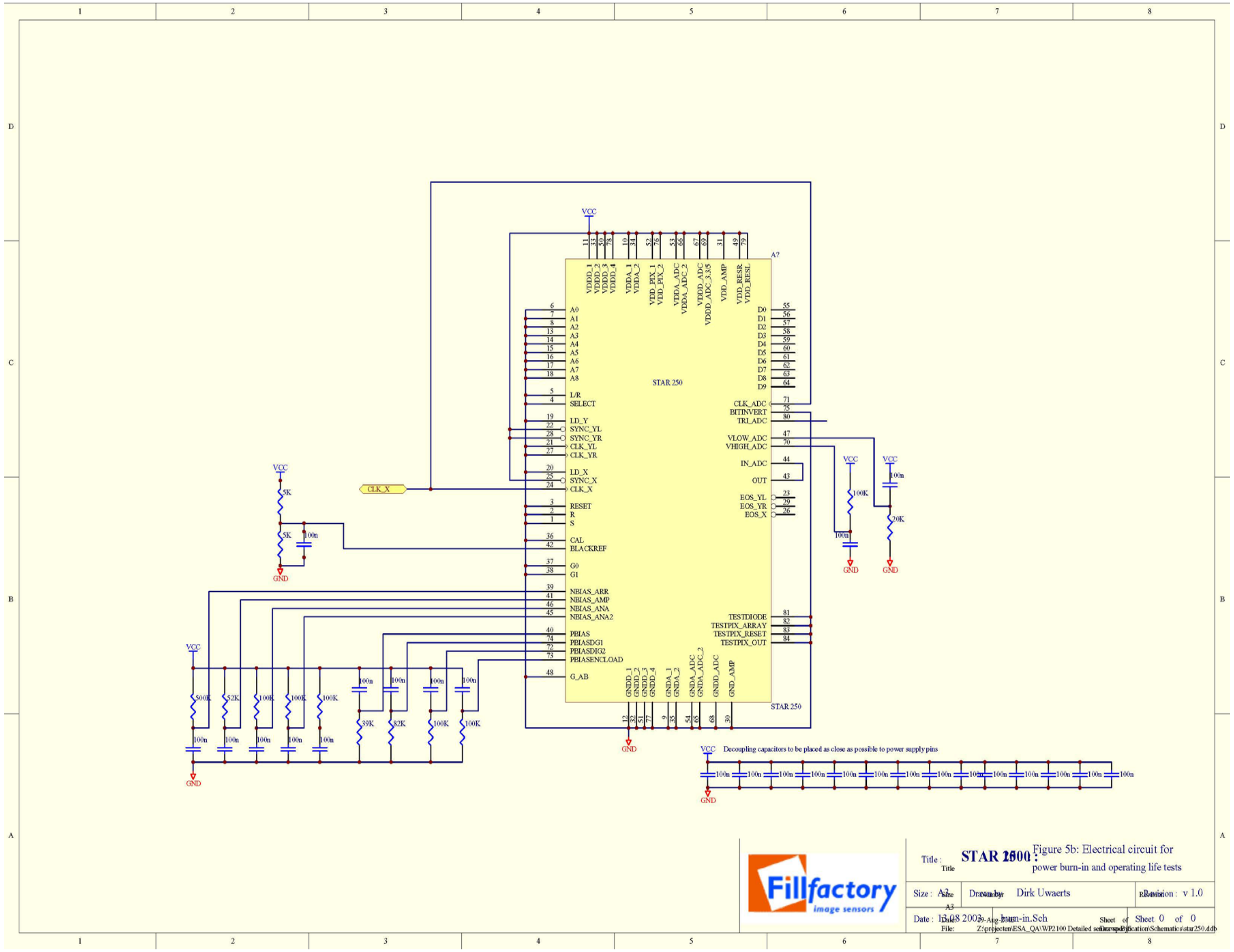


Figure 5b: Electrical circuit for power burn-in and operating life tests

The bias circuit for total dose radiation testing is identical to figure 5b

Figure 6: Biasing circuit for total dose radiation testing

Appendix A: Pin description

This appendix contains a pin description for the STAR250 CMOS image sensor

Power supply connections

10	VDD_ANA	Analog power supply: 5 V
11	VDD_DIG	Digital power supply 5V
31	VDD_AMP	Power supply of output amplifier: 5 V
33	VDD_DIG	Digital power supply 5V
34	VDD_ANA	Analogue power supply: 5 V
49	VDD_RESR	Reset power supply 5V
50	VDD_DIG	Digital power supply 5V
53	VDD_ADC_ ANA	ADC analogue power supply 5V
66	VDD_ADC_ ANA	ADC analogue power supply: 5 V
67	VDD_ADC_ DIG	ADC digital power supply 5V
69	VDD_ADC_ DIG_3.3/5	ADC 3.3V power supply for digital output of ADC. For interface with 5V external system: connect to VDD_ADC_DIG. For interface with 3.3 V external system: connect to 3.3V power supply.
52 76	VDD_PIX	Pixel array power supply [default: 5V, the device is then in "soft reset". In order to avoid the image lag associated with soft reset, reduce this voltage to 3…3.5 V "hard reset"]
78	VDD_DIG	Digital power supply 5V
79	VDD_RESL	Reset power supply 5V

Ground connections

9	GND_ANA	Analog ground
12	GND_DIG	Digital ground
30	GND_AMP	Ground of output amplifier
32	GND_DIG	Digital ground
35	GND_ANA	Analog ground
51	GND_DIG	Digital ground
54	GND_ADC_ANA	ADC analog ground
65	GND_ADC_ANA	ADC analog ground
68	GND_ADC_DIG	ADC digital ground
77	GND_DIG	Digital ground

Digital input signals

1	S	Control signal for column amplifier Apply pulse pattern – see sensor timing diagram
2	R	Control signal for column amplifier Apply pulse pattern – see sensor timing diagram
3	RESET	Resets row indicated by left/right shift register high active (1= reset row) Apply pulse pattern – see sensor timing diagram

4	SELECT	Selects row indicated by left/right shift register high active (1=select row) Apply 5 V DC for normal operation
5	L/R	Use left or right shift register for SELECT and RESET 1 = left / 0 = right – see sensor timing diagram
6	A0	Start address for X- and Y-pointers (LSB)
7	A1	Start address for X- and Y-pointers
8	A2	Start address for X- and Y-pointers
13	A3	Start address for X- and Y-pointers
14	A4	Start address for X- and Y-pointers
15	A5	Start address for X- and Y-pointers
16	A6	Start address for X- and Y-pointers
17	A7	Start address for X- and Y-pointers
18	A8	Start address for X- and Y-pointers (MSB)
19	LD_Y	Latch address (A0…A8) to Y start register (0 = track, 1 = hold)
20	LD_X	Latch address (A0…A8) to X start register(0 = track, 1 = hold)
21	CLK_YL	Clock YL shift register (shifts on falling edge)
22	SYNC_YL	Sets YL shift register to location preloaded in Y start register Low active (0=sync) Apply SYNC_YL when CLK_YL is high
24	CLK_X	Clock X shift register (output valid & stable when CLK_X is low)
25	SYNC_X	Sets X shift register to location preloaded in X start register. Low active (0=sync) Apply SYNC_X when CLK_X is high After SYNC_X, apply falling edge on CLK_X, and rising edge on CLK_X.
27	CLK_YR	Clock YR shift register (shifts on falling edge)
28	SYNC_YR	Sets YR shift register to location preloaded in Y start register Low active (0=sync) Apply SYNC_YR when CLK_YR is high
36	CAL	Initialise output amplifier Output amplifier will output BLACKREF in unity gain mode when CAL is high (1) Apply pulse pattern (one pulse per frame) – see sensor timing diagram
37	G0	Select output amplifier gain value: G0 = LSB; G1 = MSB 00 = unity gain; 01 = x2; 10= x4; 11=x8
38	G1	idem
71	CLK_ADC	ADC clock ADC converts on falling edge
75	BITINVERT	1 = invert output bits 0 = no inversion of output bits
80	TRI_ADC	Tri-state control of digital ADC outputs 1 = tri-state; 0 = output

Table 13: Digital output signals

23	EOS_YL	End-of-scan of YL shift register Low first clock period after last row (low active)
26	EOS_X	End-of-scan of X shift register Low first clock period after last active column (low active)
29	EOS_YR	End-of-scan of YR shift register Low first clock period after last row (low active)

55	D0	ADC output bit (LSB)
56	D1	ADC output bit
57	D2	ADC output bit
58	D3	ADC output bit
59	D4	ADC output bit
60	D5	ADC output bit
61	D6	ADC output bit
62	D7	ADC output bit
63	D8	ADC output bit
64	D9	ADC output bit (MSB)

Analog input connections

39	NBIASARR	Connect with 500 KΩ to Vdd and decouple to ground by 100 nF capacitor
40	PBIAS	Connect with 40 KΩ to ground and decouple to Vdd by 100 nF capacitor for 12.5 MHz pixel rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation)
41	NBIAS_AMP	Output amplifier speed/power control Connect with 82K to VDD and decouple with 100 nF to GND for 12.5 MHz output rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation)
42	BLACKREF	Control voltage for output signal offset level Buffered on-chip, the reference level can be generated by a 100K resistive divider. Connect to +/- 2 V DC for use with on-chip ADC
44	IN_ADC	Input, connect to sensor's output Input range is between 2 & 4 V (VLOW_ADC & VHIGH_ADC)
45	NBIASANA2	Connect with 100 KΩ to VDD and decouple to GND
46	NBIASANA	Connect with 100 KΩ to VDD and decouple to GND
47 70	VLOW_ADC VHIGH_ADC	Low reference and high reference voltages of ADC should be about 2 and 4 V. The internal resistance between VLOW_ADC and VHIGH_ADC is about 1.1 K. The required voltage settings on VLOW_ADC and VHIGH_ADC can be approximated by tying VLOW_ADC with 1.2 K to GND and VHIGH_ADC with 560 Ohm to VDD
48	G_AB	Anti-blooming drain control voltage: Default: connect to ground. The anti-blooming is operational but not maximal Apply 1 V DC for improved anti-blooming
72	PBIASDIG2	Connect with 100K to GND and decouple to VDD
73	PBIASENCLOAD	Connect with 100K to GND and decouple to VDD
74	PBIASDIG1	Connect with 47K to GND and decouple to VDD

Analog output connections

43	OUT	Analogue output signal To be connected to the analogue input of the ADC

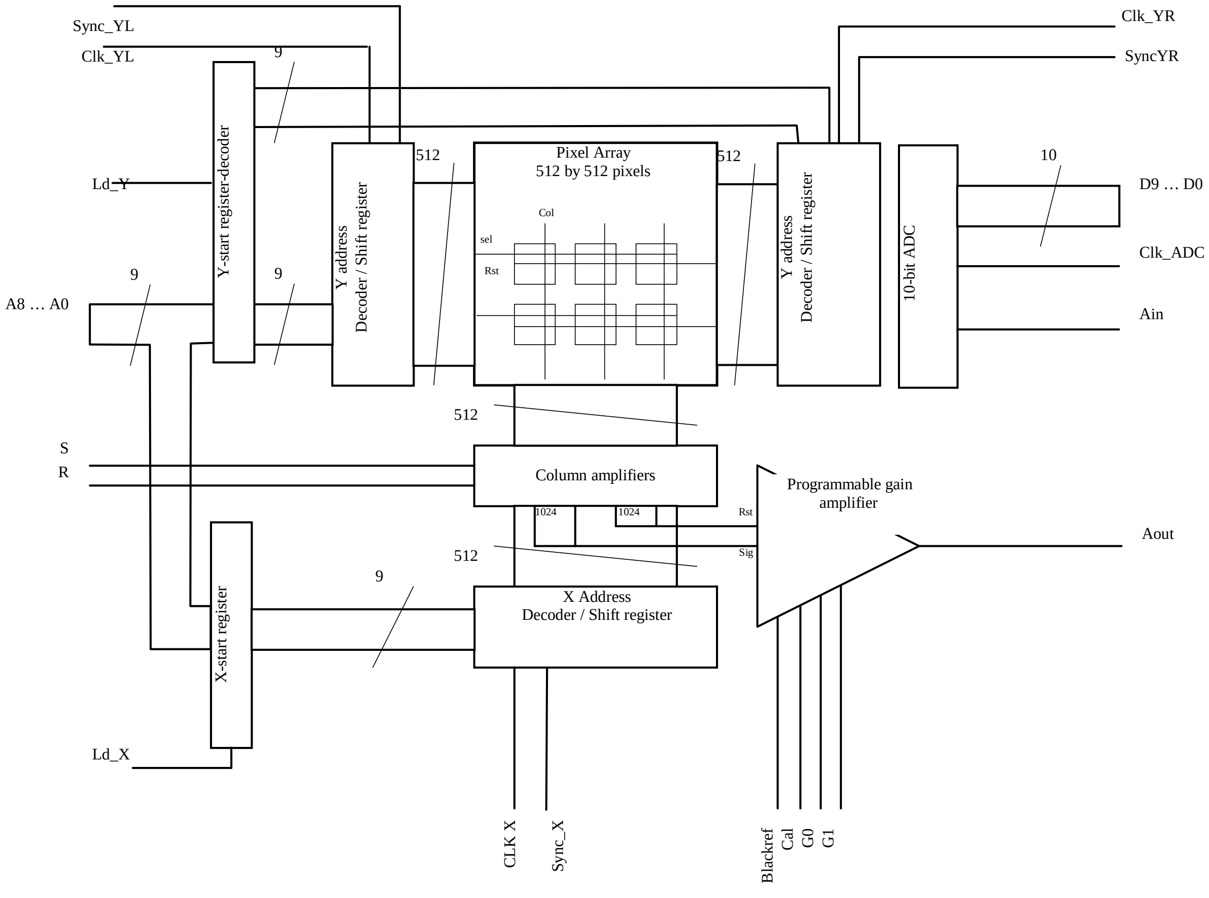
Test structures

81	TESTDIODE	Plain photo diode, size: 14 x 25 pixels Must be left open for normal operation
82	TESTPIX ARRAY	Array of test pixels, connected in parallel (14 x 25 pixels) Must be left open for normal operation
83	TESTPIXEL _RESET	Reset input of single test pixel Must be tied to GND for normal operation
84	TESTPIXEL _OUT	Output of single test pixel Must be left open for normal operation

Appendix B: User Manual

Image sensor architecture

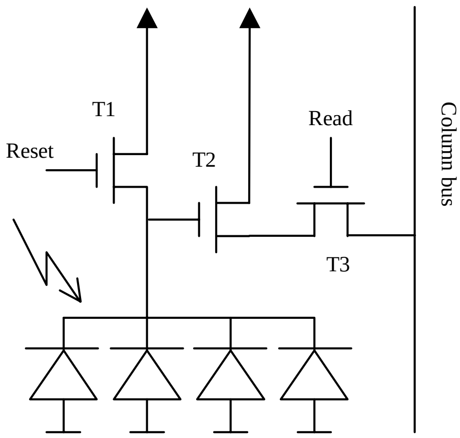
The base line of the STAR250 sensor design consists of an imager with a 512 by 512 array of active pixels at 25 µm pitch. The detector contains on-chip correction for Fixed Pattern Noise (FPN) in the column amplifiers, a programmable gain output amplifier and a 10-bit Analog to Digital Converter (ADC). Through additional preset registers the start position of a window can be programmed to enable fast read out of only part of the detector array.



Star250 schematic

Electrical signal path

The image sensor consists of several building blocks as outlined in Figure 1. The central element is a 512 by 512 pixel array with square pixels at 25 µm pitch. Unlike in classical designs the pixels of this sensor contain four photodiodes. This configuration enhances the MTF and reduces the PRNU. Figure 2 shows an electrical diagram of the pixel structure. The four photodiodes are connected in parallel to the reset transistor (T1). Transistor T2 converts the charge, collected on the photo diode node to a voltage signal that can be connected to the column bus by T3. The "Reset"- and the "Read"- entrance of the pixel are connected to one of the Y shift registers each.



Pixel schematic

These shift registers are located next to the pixel array and contain as many outputs as there are rows in the pixel array. They are designed as“1-hot” registers (YL and YR shift register) each allowing selection of one row of pixels at a time. A clock pulse moves the pointer one position down the register resulting in the subsequent selection of every individual row for either reset or for read-out. The spatial offset between the two selected rows determines the integration time. A synchronization pulse to the shift registers loads the value from a preset register into the shift register forcing the pointer to a pre-determined position. Windowing in the vertical (Y-) direction is achieved by presetting the registers to a row that is not the first row and by clocking out only the required number of rows.

All pixel outputs are connected to a column bus and each column bus feeds the pixel signal to a column amplifier. Using a double sampling technique these amplifiers can subtract the remaining pixel offset from the signal. To serialize the output signal from the column amplifiers an identical shift/preset technique is used as for the vertical (Y-) direction. Windowing is thus also possible in the X-direction.

The signal from the column amplifiers is then fed to an output amplifier with four pre-settable gains. The offset correction of this amplifier is done through a black-reference procedure. The signal from the output amplifier is externally available on the analogue output terminator of the device.

The on-chip 10-bit ADC is electrically separated from the other circuits of the device and can be used if required. Alternatively an external ADC can be used and the internal ADC can be powered down.

Integrating imager operation principles

The STAR250 is a line-scan based integrating imager with provisions for versatile readout (windowing, electronic shuttering...). This combination results in certain timing relations and dependencies that are relevant to the end-user. These relations are defined and explained in the following paragraphs.

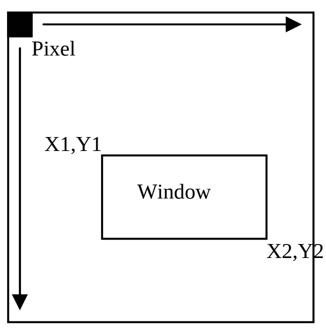


Image definitions

The following definitions concern the STAR250 image plane dimensions, and the format of the resulting pictures.

Figure 1a: Coordinate system on the image.

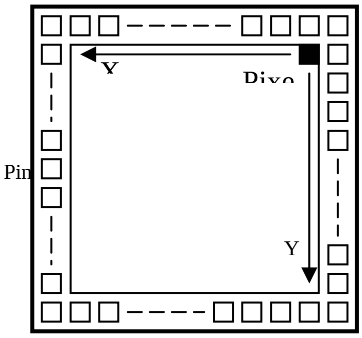


Figure 2b: Coordinate system on the physical die.

Image coordinates are defined with respect to an absolute origin1 (0,0). Figure 3a shows the coordinate system projected on the image, as it can be seen on a computer display or a printout. Figure 3b shows the coordinate system on the physical die.

This origin is at the *top-left corner* of the image, corresponding to the *top-right corner* on the actual STAR250 chip. The imager X-axis runs horizontally towards the right from the origin; the Y-axis runs vertically and downwards from the origin. In the resulting image reference frame, windows are scanned line by line, from top to bottom. Lines are scanned pixel by pixel, from the left to the right.

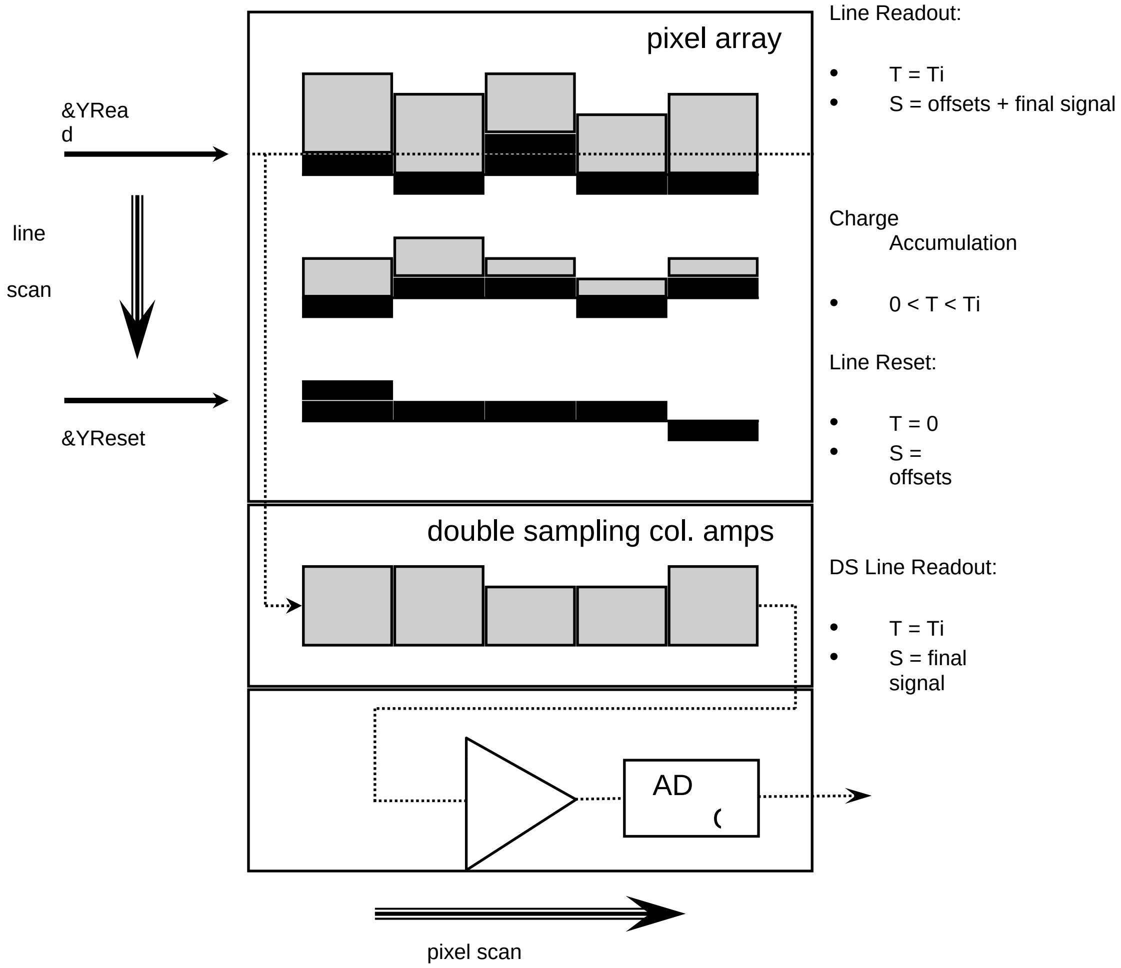
Term	Definition	Value
Matrix	Full-size picture, 512 x 512 pixels	
Window	Region-of-interest, portion of a matrix under readout, a rectangular area of less than 512 x 512 pixels, at a user-defined position in the matrix plane	
Frame	Synonym to window, including the special case of a matrix	
H_{frame}	Effective frame height	(Y2-Y1+1)
W_{frame}	Effective frame width	(X2-X1+1)
H_{matrix}	Matrix height	512 lines
W_{matrix}	Matrix width	512 pixels
X1	Top-left X coordinate of a frame	
Y1	Top-left Y coordinate of a frame	
X2	Bottom-right X coordinate of a frame	
Y2	Bottom-right Y coordinate of a frame	
X_{rd}	X coordinate of pixel currently under readout	
Y_{rd}	Y coordinate of line currently under readout (YL)	
Y_{rst}	Y coordinate of line currently under reset (YR)	
Delay Lines	Number of lines equivalent to the integration time	SYNC_YL-SYNC_YR

Operation

Integrating imager operation

In a line-scan integrating imager with electronic shutter, two continuous processes take care of image gathering. The first process resets lines in a progressive scan. At line reset, all of the pixels in a line are drained from any photo charges collected since their last reset or readout. After reset, a new exposure cycle starts for that particular line.

During readout, photo charges collected since the previous reset, are converted into an output



voltage, which is then passed on - pixel by pixel - to the imager's pixel-serial output and ADC. Readout is destructive, i.e. the accumulation of charges from successive exposure phases is not possible in the present architecture.

Three internal address pointers control the processes of line and pixel readout and line reset. These pointers indicate the current line under readout (Y_{rd}), the current line under reset (Y_{rst}), and the current pixel under readout (X_{rd}), also see Figure 4. The progress rate of line resets is equal to the progress rate of line readouts. *Physically the Yread and Yrst register are located at left and right sides of the imager, and therefore named YL (the readout register) and YR (the reset register). The control of the row signals can be given to each of them, by the pin named L/R.*

The actual line readout process starts with addressing the line to read. This can be done either by initialising the Y_{rd} pointer with a new value, or by shifting it one position beyond its previous value. (Addressing the line to be reset, Yrst is done in an analogous fashion). During the "blanking time", after the new line is addressed on the sensor, the built-in column-parallel double sampling amplifiers are operated, which renders offset-corrected values of the line under readout.

After the blanking time, the pixels of the row addressed by YL, are read by multiplexing all of the pixels one by one to the serial output chain. The pixel is selected by the X_{rd} pointer, and that pointer can either be initialised with a new value, or be an increment of the previous position. The analog chain has further a track&hold stage, output buffer, followed by an (electrically separate) ADC.

The time between row resets and their corresponding row readouts is the effective exposure time (or integration time). This time is proportional to the number of lines, (*DelayLines*) between the line currently under reset and the line currently under readout: *DelayLines* = $(Y_{rst} - Y_{rd} + 1)$. This time is thus also equal to *the delay between the SYNC_YR pulse and the subsequent SYNC_YR.*

The effective integration time t_{int} is thus calculated as (*delaylines * line time*). The line time itself is a function of four terms: the time to output the desired number of pixels in the line (W_{frame}), and the overhead ("blanking") time that is needed to select an new line and perform the double sampling and reset operations.

Variable integration time (electronic shuttering)

The following figure illustrates the variable integration time, for the case of t_{int} equal to the frame read time $t_{rd,frame}$, the case of under-exposure, and the case of over-exposure.

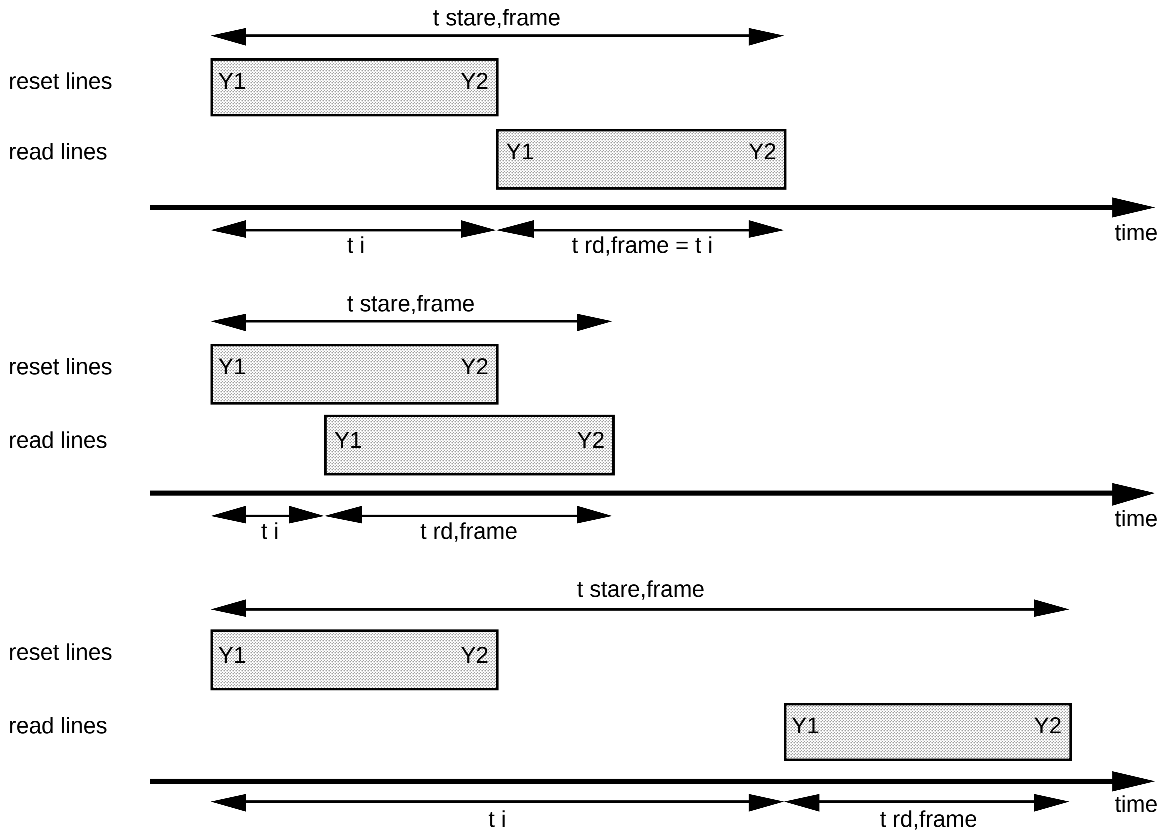


figure 5: Variable integration time: nominal exposure, under-exposure and over-exposure. A new reset or reset cycle (not shown) may start whitel the previous read is still going on. Note that a read cycle also resets, thus in principle a reset cycle is only neede in underexposure.

Image readout procedure

The procedure to read out a windowed image, characterized with the coordinates (X1, Y1) and (X2, Y2), and with an integration time equivalent to `DelayLines` lines, is:

A pre-amble or initialisation phase is not considered relevant. The sensor is read out continuously. The first frame – as there was no preceding reset of each pixel – is generally saturated and useless.

Image readout

In an infinite uninterrupted loop, do, line-by-line:

Synchronise the read (YL) and/or reset (YR) registers, IN THIS CASES:

-SYNC_YL to re-initiate the readout sequence to row position Y1

-SYNC_YR to re-initiate the reset pointer to row position Y1

for all other lines do not pulse one of these SYNC_Y*.

Operate the double sampling column amplifiers, with two RESETs. Apply one to reset the line that is currently selected to produce the reset reference level for the double sampling column amplifiers. Apply the other reset to another line, depending on the required integration time reduction.

Perform a line-readout:

Reset the X read address shift register to the value in its shadow register (X1).

For (X2-X1+1) pixels do:

Perform a pixel readout operation, operating the track/hold and the ADC

Shift the X read address shift register one position further.

Shift the Y read and reset address shift registers one position further; note: if either of Y read or reset address shift register comes at a position equivalent to Y2, wrap it around to position Y1 by pulsing SYNC_YL.

Timing and control sequences

The following paragraphs describe the timing of the digital control signals to be applied to the sensor. The given information is based upon simulations and must be confirmed by practical experiments after fabrication of test samples.

Basic timing

Figure 6 and Figure 7 show the basic timing diagram of the STAR250 image sensor and Table 3 shows the timing specifications of the clocking scheme.

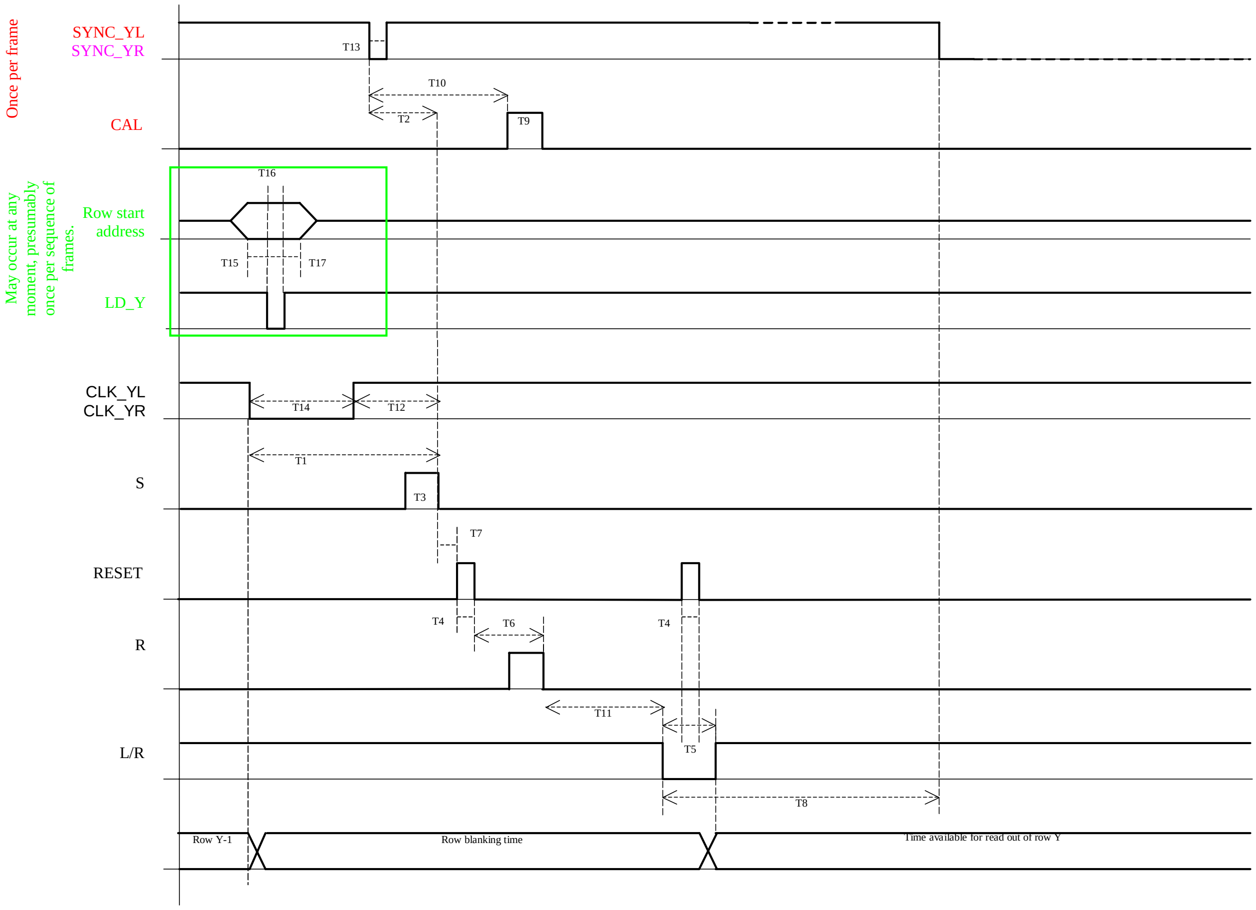


Figure 6: Frame read-out timing sequence

Note: SYNC_YR is not identical to as SYNC_YL. SYNC_YR is used in case of electronic shutter. The CLK_YR is driven identically as CLK_YL, but the SYNC_YR pulse leads the SYNC_YL pulse by a certain number of rows. This lead-time is the effective integration (electronic shutter ~) time. Relative to the row timing, both SYNC pulses are given at the same time position, once per frame, but during different rows.

SYNC_YL is pulsed when the first row will be read out and SYNC_YR is pulsed for the electronic shutter to start for this first row. CAL is pulsed on the first row too, 2 µs later than SYNC_YL.

The minimal idle time is 1.4 µs (before starting reading pixels). However, it is advised not to read out pixels during the complete row initialization process (in between the rising edge on S and the falling edge on L/R). In this case, the total idle time is minimally.

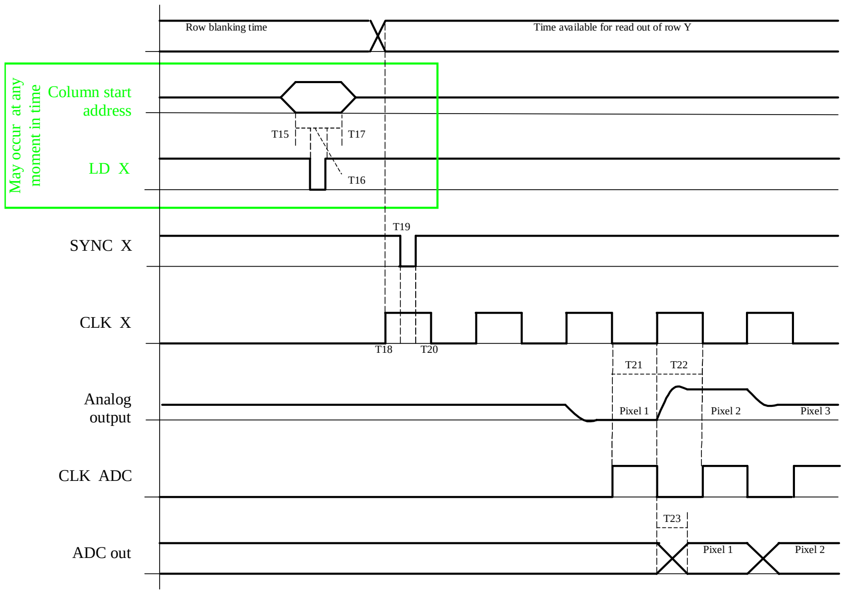
This timing assumes that the Y start register has been loaded in advance, which can occur at any time but before the pulse on SYNC_YL or SYNC_YR.

Timing specifications

Symbol	Min	Typ	Description
T1	1.8 µs		Delay between selection of new row by falling edge on CLK_YL and falling edge on S. Minimal value. Normally, CLK_YR should be low already at the end of the previous sequence.
T2	1.8 µs		Delay between selection of new a row by SYNC_YL and falling edge on S.
T3	0.4 µs		Duration of S and R pulse.
T4	0.1 µs		Duration of RESET pulse.
T5	T4 + 40 ns	0.3 µs	L/R pulse must overlap second RESET pulse at both sides.
T6	0.8 µs		Delay between falling edge on RESET and falling edge on R.
T7	20 ns	0.1 µs	Delay between falling edge on S and rising edge on RESET.
T8	0	1 µs	Delay between falling edge on L/R and falling edge on CLK_Y.
T9	100 ns	1 µs	Duration of cal pulse. The CAL pulse is given once each frame.
T10	0	2 µs	Delay between falling edge of SYNC_YL and rising edge of CAL pulse.
T11	40 ns	0.1 µs	Delay between falling edge on R and rising edge on L/R.
T12	0.1 µs	1 µs	Delay between rising edge of CLK_Y and falling edge on S.
T13		0.5 µs	Pulse width SYNC_YL / YR
T14		0.5 µs	Pulse width CLK_YL / YR
T15	10 ns		Address set-up time
T16	20 ns		Load X / Y start register value
T17	10 ns		Address stable after load
T18	10 ns		
T19	20 ns		SYNC_X pulse width. SYNC_X while CLK_X is high.
T20	10 ns		
T21		40 ns	Analogue output is stable during CLK_X low.
T22		40 ns	CLK_X pulse width: During this clock phase the analogue output ramps to the next pixel level.
T23		125 ns	ADC digital output stable after falling edge of CLK_ADC

How to load the X- and Y- start positions

The start positions (start addresses) for "ROI" (region of interest) are pre-loaded in the X or Y start register. They become effective by the application of the SYNC_X, SYNC_YL and/or SYNC_YR. The start X- or Y address must be applied to their common address bus, and the corresponding LD_X or LD_Y pin must be pulsed.



Column read-out timing sequence

On each **falling** edge of CLK_X, a new pixel of the same row (line) is accessed. The output stage is in hold when CLK_X is low and starts generating a new output after a rising edge on CLK_X.

The following timing constraints apply:

The X or Y start addresses can be uploaded well in advance, before the X or Y shift registers are preset by a SYNC pulse. However, if necessary, they can be loaded just before the SYNC_X or SYNC_Y pulse as shown in the figure.

E.g. the X start register can be loaded during the row idle time. The Y start register can be loaded during readout of the last row of the previous frame.

If the X or Y start address does not change for subsequent frames, it does not need to be reloaded in the register.

Other signals:

The SELECT signal must be tied to Vdd for normal operation. This signal was added for diagnostic reasons and inhibits the pixel array operation when held low.

The CAL signal sets the output amplifier DC offset level. When this signal is active (high) the pixel array is internally disconnected from the output amplifier, its gain is set to unity and its input signal is connected to the BLACK_REF input. This action must be performed at least once per frame. (on may even choose to do it once per line – but not advised)

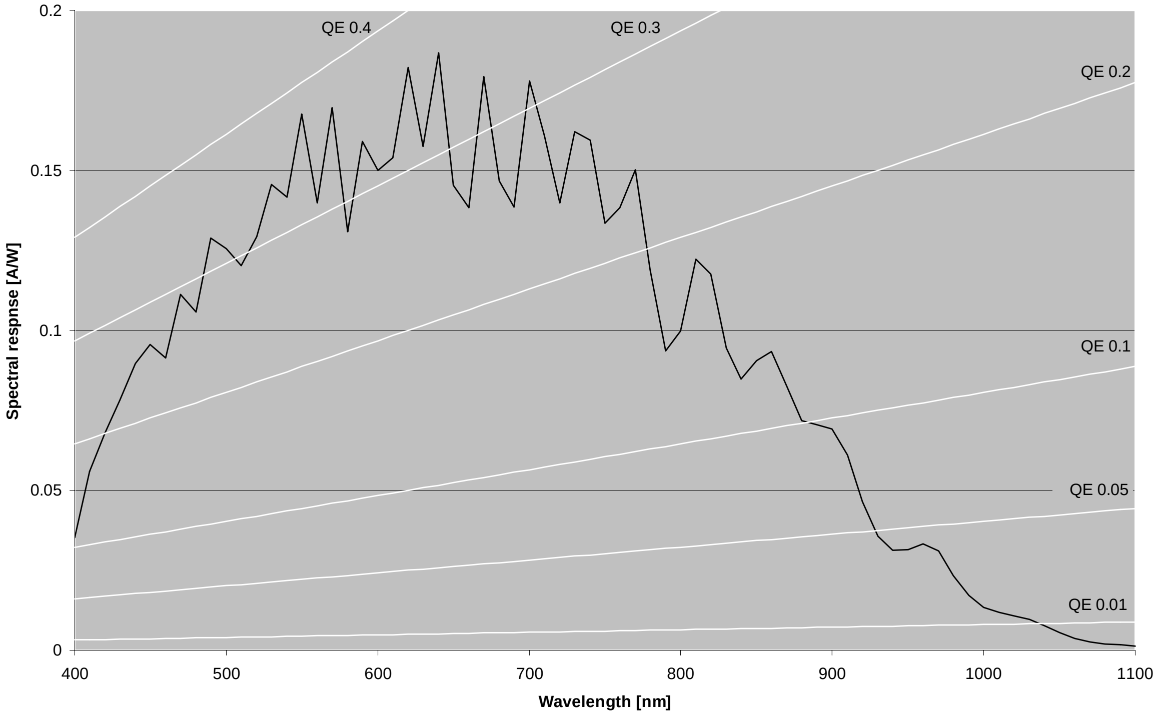
EOS_X, EOS_YL and EOS_YR produce a pulse when the respective shift register comes at its end. These outputs are used mainly during testing to verify proper operation of the shift registers.

TEST DIODE and TESTPIXEL ARRAY are connections to optical test structures that are used for electro-optical evaluation. TEST-DIODE is a plain photodiode with an area of 14x5 pixels. TESTPIXEL_ARRAY is an array (14x5) of pixels where the photodiodes are connected in parallel. These structures are used to measure the photocurrent of the diodes directly.

TESTPIXEL_RESET and TESTPIXEL-OUT are connections to a single pixel that can be used for test purposes.

Appendix C: Typical spectral response data

The following figure shows a typical spectral response curve. The fringes in the curve result from optical interference in the top dielectric layers.

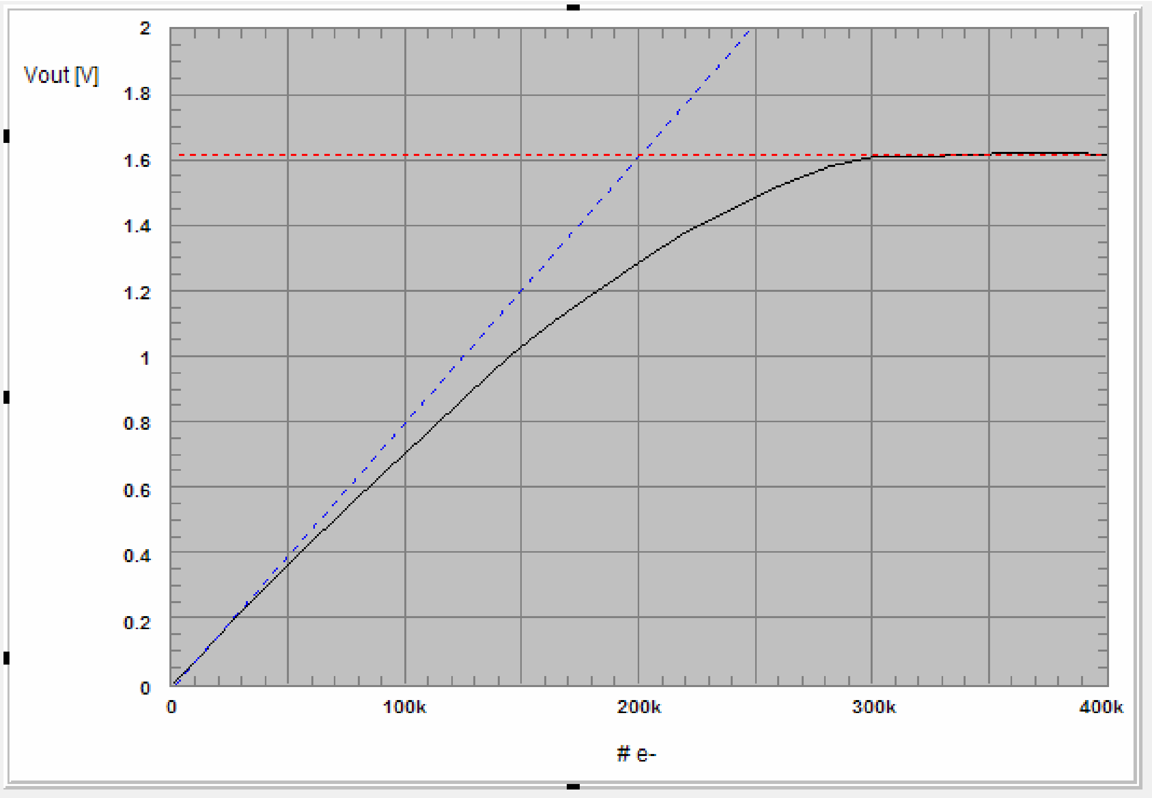


Typical spectral response curve, tabular data:

Wl [nm]	Pixel response [A/w]	Wl [nm]	Pixel response [A/w]
400	2.13E-02	760	1.05E-01
410	3.49E-02	770	1.08E-01
420	4.96E-02	780	8.77E-02
430	5.94E-02	790	8.17E-02
440	6.72E-02	800	9.29E-02
450	7.08E-02	810	9.14E-02
460	6.42E-02	820	8.13E-02
470	8.36E-02	830	7.60E-02
480	8.94E-02	840	7.42E-02
490	8.90E-02	850	6.51E-02
500	8.24E-02	860	5.38E-02
510	1.01E-01	870	4.82E-02
520	1.03E-01	880	4.84E-02
530	1.17E-01	890	5.04E-02
540	1.10E-01	900	4.86E-02
550	1.09E-01	910	4.06E-02
560	9.48E-02	920	3.28E-02
570	1.27E-01	930	2.95E-02
580	1.08E-01	940	2.91E-02
590	1.37E-01	950	2.87E-02
600	1.26E-01	960	2.70E-02
610	1.43E-01	970	2.30E-02
620	1.04E-01	980	1.85E-02
630	1.06E-01	990	1.57E-02
640	1.30E-01	1000	1.18E-02
650	1.01E-01	1010	1.01E-02
660	1.14E-01	1020	8.18E-03
670	1.34E-01	1030	6.16E-03
680	1.17E-01	1040	4.56E-03
690	1.31E-01	1050	3.44E-03
700	1.20E-01	1060	2.81E-03
710	9.68E-02	1070	2.44E-03
720	1.06E-01	1080	2.11E-03
730	1.20E-01	1090	1.78E-03
740	9.89E-02	1100	1.56E-03
750	8.97E-02		

Appendix D: Typical electro-optical response data

The following figure shows a typical electro-optical response curve. The saturation fit and +-1% linearity fit are plotted on the curve.

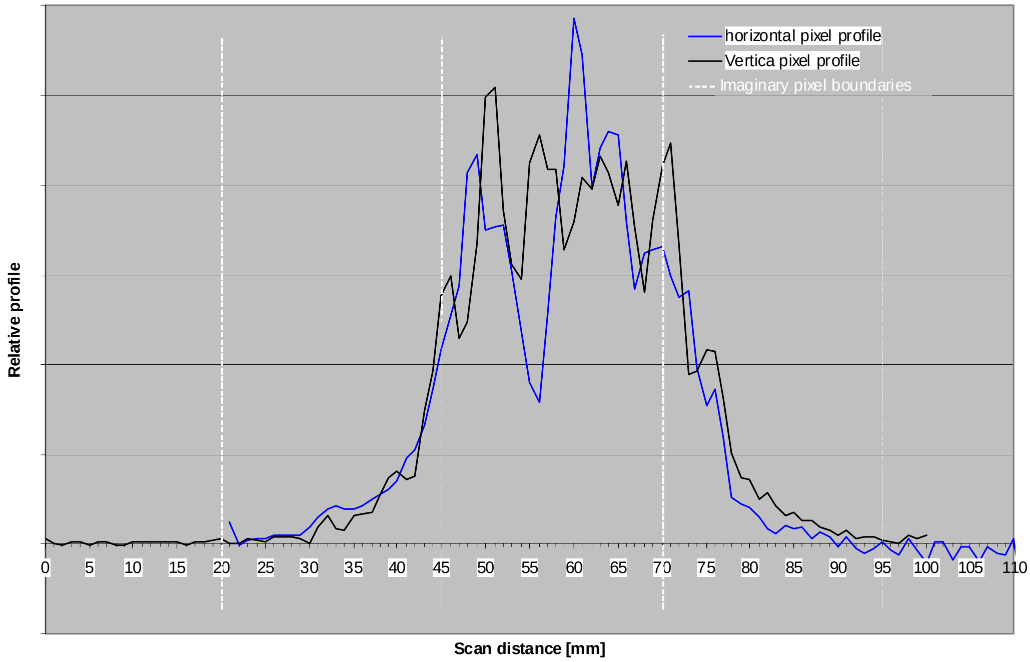


Typical electro-optical response, tabular data.

Pixel charge [e-]	Vout [V]	Pixel charge [e-]	Vout [V]
11751	0.083	220310	1.382
25341	0.194	240389	1.455
40764	0.303	259714	1.523
56791	0.413	281896	1.581
73543	0.530	301140	1.610
90866	0.650	321333	1.615
108500	0.765	341663	1.618
125952	0.882	361024	1.623
144565	1.002	381507	1.622
163281	1.110	402272	1.619
182306	1.204	424343	1.617
202061	1.296	445699	1.618

Appendix E: Typical pixel profile data

Horizontal and vertical pixel profile measurement data at 600 nm



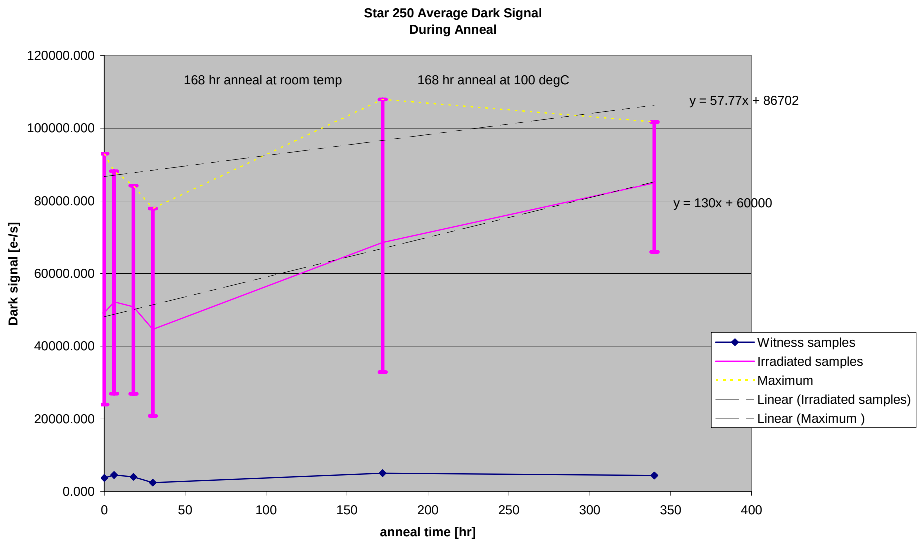
Horizontal pixel profile measurement data at 600 nm, tabular data.

Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]
0	1.1368	40	1.032	80	0.0256
1	1.1364	41	1.0076	81	0.0228
2	1.136	42	0.984	82	0.0196
3	1.1344	43	0.9572	83	0.016
4	1.1344	44	0.9264	84	0.014
5	1.1352	45	0.8952	85	0.0124
6	1.1344	46	0.8672	86	0.0116
7	1.1324	47	0.8368	87	0.0108
8	1.1324	48	0.8088	88	0.01
9	1.1312	49	0.774	89	0.0088
10	1.1304	50	0.7388	90	0.0084
11	1.13	51	0.6996	91	0.0076
12	1.1268	52	0.6632	92	0.0076
13	1.1264	53	0.6124	93	0.0068
14	1.1256	54	0.5692	94	0.006
15	1.1268	55	0.5264	95	0.0056
16	1.1248	56	0.4808	96	0.0056
17	1.1232	57	0.4408	97	0.0052
18	1.1224	58	0.4184	98	0.0044
19	1.1212	59	0.4036	99	0.0044
20	1.1188	60	0.3916	100	0.0044
21	1.1192	61	0.3728	101	0.004
22	1.1184	62	0.346	102	0.0036
23	1.1168	63	0.3164	103	0.0036
24	1.1148	64	0.2864	104	0.0036
25	1.1144	65	0.246	105	0.0036
26	1.1112	66	0.2116	106	0.004
27	1.1104	67	0.1808	107	0.0024
28	1.1088	68	0.1524	108	0.0028
29	1.1048	69	0.1244	109	0.0012
30	1.102	70	0.1052	110	0.0016
31	1.0996	71	0.088	111	0.0012
32	1.0952	72	0.0764	112	0.0008
33	1.0928	73	0.066	113	0.0012
34	1.0904	74	0.0564	114	0.002
35	1.0848	75	0.0496	115	0.0016
36	1.08	76	0.0444	116	0.0024
37	1.0716	77	0.038	117	0
38	1.0608	78	0.0324	118	0.0004
39	1.0476	79	0.0292	119	0.0004

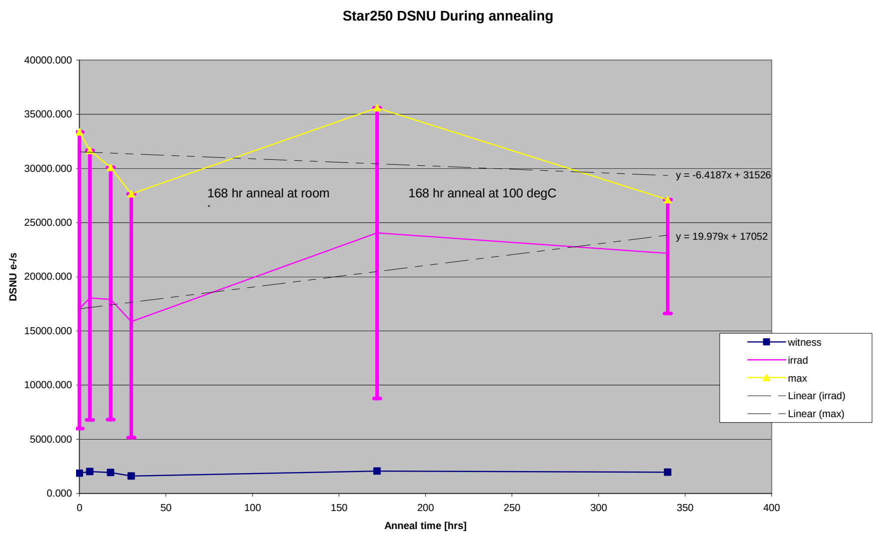
Horizontal pixel profile measurement data at 600 nm, tabular data.

Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]	Distance [µm]	Pixel Vout [V]
0	0	32	0.0244	64	0.9992
1	0	33	0.0288	65	1.0404
2	0.0004	34	0.0356	66	1.082
3	0.0004	35	0.0432	67	1.126
4	0.0004	36	0.0516	68	1.148
5	0.0004	37	0.058	69	1.1676
6	0.0008	38	0.0684	70	1.1876
7	0.0008	39	0.0872	71	1.2104
8	0.0012	40	0.1076	72	1.2292
9	0.0012	41	0.1408	73	1.2428
10	0.0016	42	0.1652	74	1.2504
11	0.0016	43	0.1888	75	1.2584
12	0.0016	44	0.2168	76	1.2644
13	0.002	45	0.2576	77	1.2692
14	0.002	46	0.3124	78	1.2756
15	0.0028	47	0.3556	79	1.278
16	0.0032	48	0.3884	80	1.2824
17	0.0032	49	0.4196	81	1.2848
18	0.0036	50	0.4512	82	1.288
19	0.0044	51	0.5024	83	1.29
20	0.0044	52	0.5404	84	1.292
21	0.0052	53	0.5864	85	1.2932
22	0.006	54	0.622	86	1.2944
23	0.0068	55	0.6548	87	1.296
24	0.0076	56	0.6944	88	1.296
25	0.008	57	0.7352	89	1.2976
26	0.0084	58	0.7744	90	1.2976
27	0.0116	59	0.8204	91	1.2984
28	0.014	60	0.8568	92	1.298
29	0.0152	61	0.8976	93	1.2988
30	0.0176	62	0.9392	94	1.2996
31	0.0212	63	0.9684	95	1.3004

Appendix F:
Observed effects during annealing after total dose irradiation



Star250 Average Dark Current during annealing



STAR 250 Dark Signal Non Uniformity during annealing

1. **Average dark current rise during annealing.**
   On the average, the dark current still increases during annealing. This observation is not in line with the conclusions of J. Bogaerts. However, during this test the samples

were annealed under bias while in the first test the samples were annealed without bias.

	STAR 250
Average dark current rise under annealing	130 e-/s per Krad
Maximum dark current rise under annealing	69 e-/s per Krad

2. **The average DSNU remains constant during annealing**
   It was observed that the average DSNU slightly rises during annealing at room temperature, immediately after irradiation but decreases at elevated temperature. The net effect is almost constant.

	STAR 250
Average DSNU rise during annealing	20 e-/s per Krad
Maximum-DSNU rise during annealing	-6 e-/s per Krad See remark !

3. **The spread in DSNU between samples decreases during annealing at temperature.**