Radiation Evaluation of ST Test Structures in commercial 130nm CMOS BULK and SOI In commercial 90nm CMOS BULK in commercial 65nm CMOS BULK and SOI

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Final Presentation of ESTEC Contract No. 13528/95/NL/MV, COO-18.
Progress Presentation of ESTEC Contract No. 18799/04/NL/AG, COO-3.

STMicroelectronics

Headline

- **Brief overview on ST (Crolles) developments in radiation test, modeling & hardening**
  - why does ST-Central R&D care about TERRESTRIAL radiations for years?
  - radiation test procedures for consumer applications
  - proprietary neutron & alpha simulators
  - original hardened solutions

- **Test parameters for the radiation assessment of commercial ST 130 and 90nm CMOS**
  - selection of several process options, circuits, devices, power supplies, etc
  - commercial technologies : not hardened against radiations

- **Main Single Event Effects (SEE) test results with heavy ions & protons**
  - 130nm BULK and SOI
  - 90nm BULK

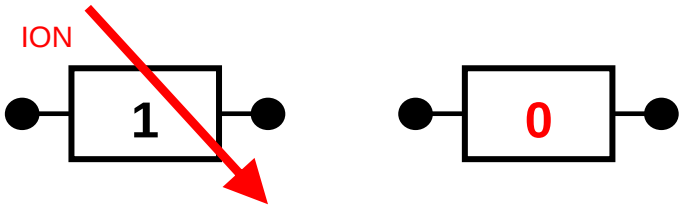
- **Main Total Ionizing Dose (TID) test results with a Co^{60} gamma source**
  - 130nm BULK
  - 90nm BULK

- **Preliminary results in ST 65nm CMOS BULK and SOI**

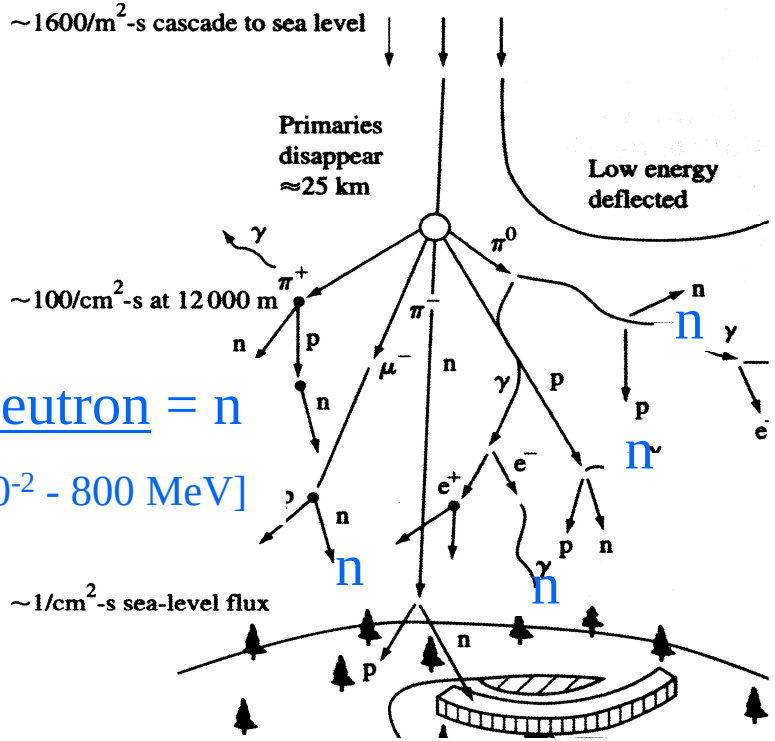
- **Conclusion**

Reminders on the Soft Error Rate (SER) problematic

A Soft Error (or Single Event Upset) is a non destructive logic state flipping in a memory cell



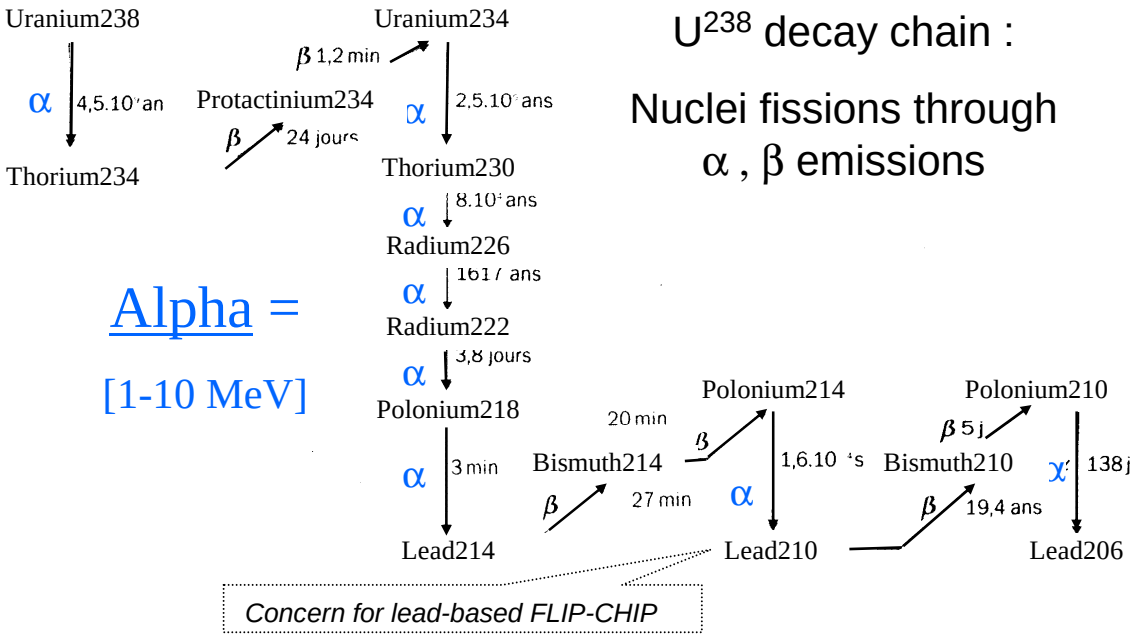
Cosmic Rays in the earth atmosphere



Neutron = n

[10^{-2} - 800 MeV]

Radioactive Impurities U/Th within process materials & packages



Alpha =

[1-10 MeV]

U^{238} decay chain :

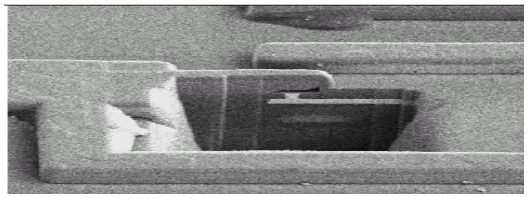
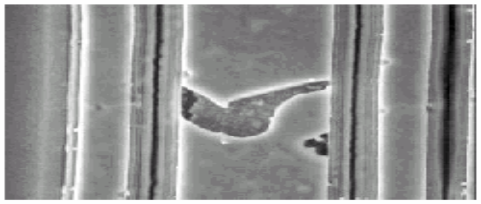
Nuclei fissions through α , β emissions

J.Ziegler, IBM JR&D, 1996

N.B : Total Dose, Heavy ions, Protons can be totally neglected at sea-level

Soft Error Rate (SER) vs. other reliability mechanisms

- **Typical failure rate for a hard reliability mechanism : 1-5 FIT (fails during 1^E9 hours)**
  - Illustrations of metal electromigration issues on nanotechnologies

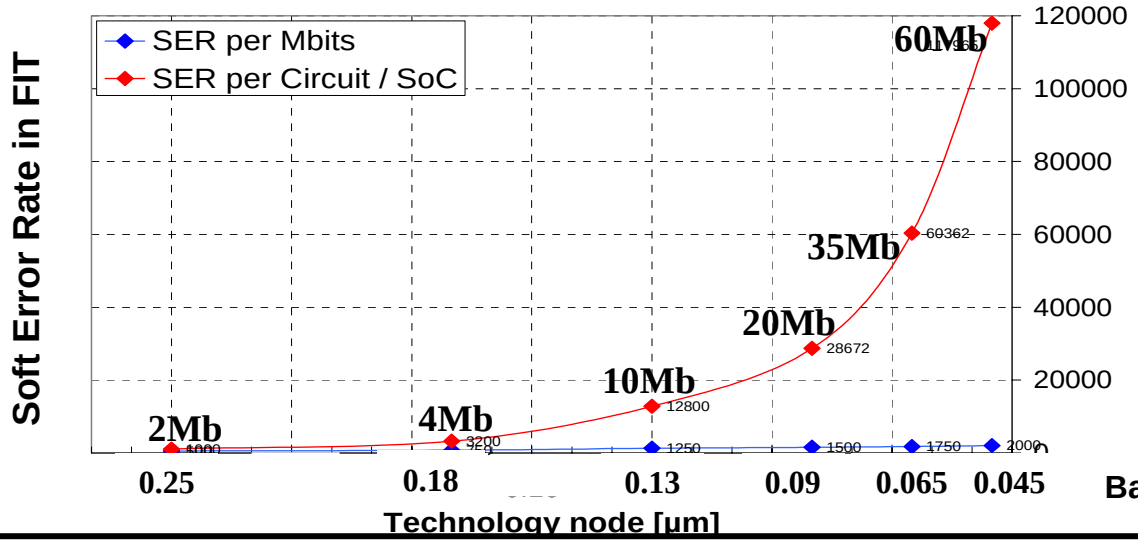




  - Oxide breakdown, Soft breakdown, hot carrier injection , NTBI, etc

- **Aggregate failure rate for all critical reliability mechanisms : 10-50 FIT (fails every 114,155 years)**

- **In contrast, without mitigation, the SER can potentially exceed 100,000 FIT/chip**
  - e.g. for a very large circuit operated at very low VDD

- **Trend : constant SER/Mb but SER/chip keeps on increasing with technology downscaling**
  - with the # of cells per mm2 doubling every new generation

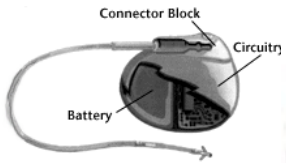


Based on ITRS roadmap

Terrestrial applications mainly concerned by SER

- **Data processing : network, server, printer, hard disk drive**
  - Critical neutron failures on SUN servers in 1999 (*EEtimes, Computer World*)
    - CEO of SUN :"a 300,000$ server should be bulletproof!"
  - Neutron-induced latchup events in CISCO routers in the field in 2004
    - *http://www.cisco.com/en/US/products/hw/routers/ps167/products_field_notice09186a00801*

- **Medical**
  - Pacemakers experienced neutron-induced shutdowns (IEEE TNS 1996)
  - Implantable electronics (e.g. defibrillators)

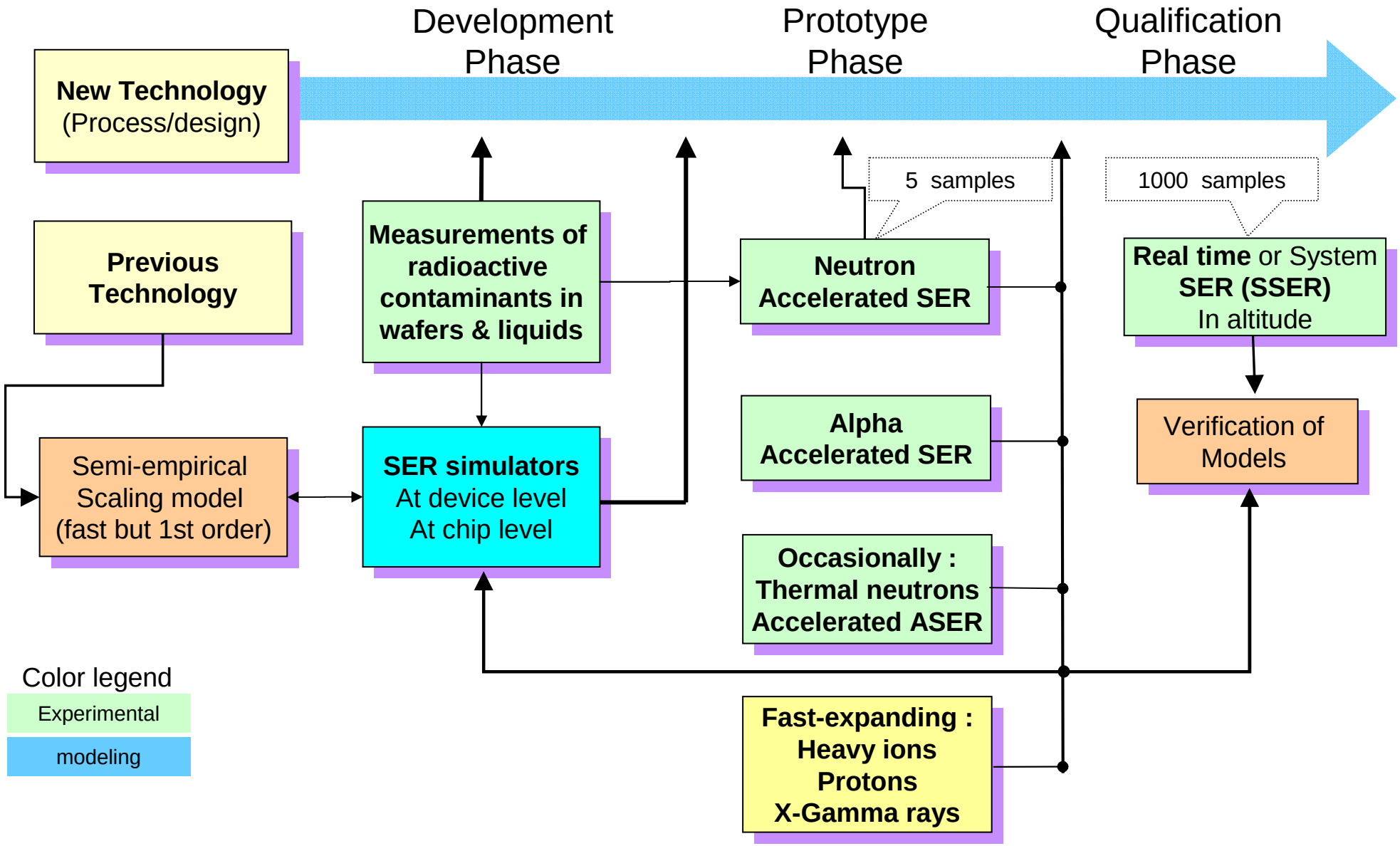


- **Automotive, Railways and Aeronautics**
  - SER is multiplied by 200-300 from sea level to aircraft altitudes
  - TGV experienced neutron-induced breakdowns

- **High Energy Physics**
  - Large Hadron Collider
    - CERN/ATLAS supplier Trophy rewarded to ST in May 2006 :

- **Chip manufacturers (consortiums SEMATECH & JEDEC)**
  - SER task forces acting for years within IBM, INTEL, TI, ST …
    - New web site for ST aerospace products : www.st.com/aerospace

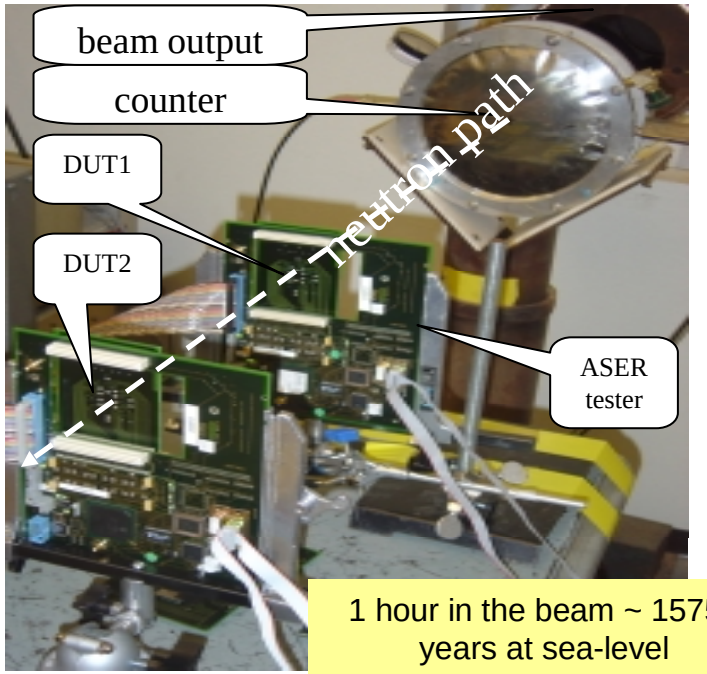
ST SER characterization flow



Test flow already applied to ST CMOS 130, 90 and 65nm
ST CMOS 45nm : about to be started

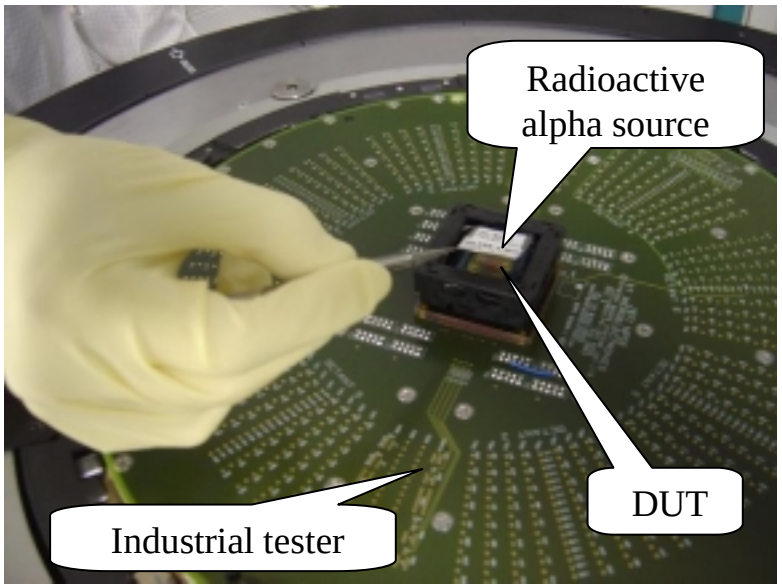
ST accelerated SER measurements : in North America & Crolles

Neutron : @ Los Alamos & Vancouver



1 hour in the beam ~ 15753 years at sea-level

Alpha : @ Crolles with a radioactive alpha source Am241 100µCi



- **Specific ASER tester : static/dynamic testing + latchup monitoring + heating 125°C**
  - -Usable with any kind of radiation source (heavy ions, protons, neutrons, gamma)
- **Test methodology : compliant with international test standards**
  - -JEDEC JESD89A : defined with the ST participation
    - -Joint Electron Device Engineering Council : 270 companies
  - -ESA SCC basic specifications N°25100 & 22900
- **More than 20 neutron test campaigns at Los Alamos and Vancouver since 2000**

ST real-time SER measurements : new test platform operational

- **ST SER mountain lab is located in the French Alps at 2552m (n flux ×6)**
  - project founded by ST-Crolles in 2002 with a French university (L2MP) and local authorities
    - Budget ~ 1 Meuros
  - XILINX also used the test platform since 2006

- **An original real-time SER tester has been designed and manufactured**
  - coupled with ovens (125deg C)
  - teleoperated control from Crolles

- **Excellent agreement between real time and accelerated SER data measured on 5 Gb ST SRAM 130nm**
  - cf. paper at RADECS'06 by Autran, Roche et al.
  - Coming up : ST CMOS 65nm

ASTEP, Plateau de Bure, France		
Latitude (°N)		44.6
Longitude (°E)		5.9
Elevation (m)		2550
Atm. depth (g/cm^2)		757
Cutoff rigidity γ (Gy)		5.0
Relative neutron flux	Active Sun low	5.76
	Quiet Sun peak	6.66
	Average	**6.21**

Table 1. Location and main environment characteristics of the ASTEP Platform (After Ref. [1]).

Figure 1. General view of the Observatory on the Plateau de Bure. ASTEP is hosted in Building POM2 (arrow).

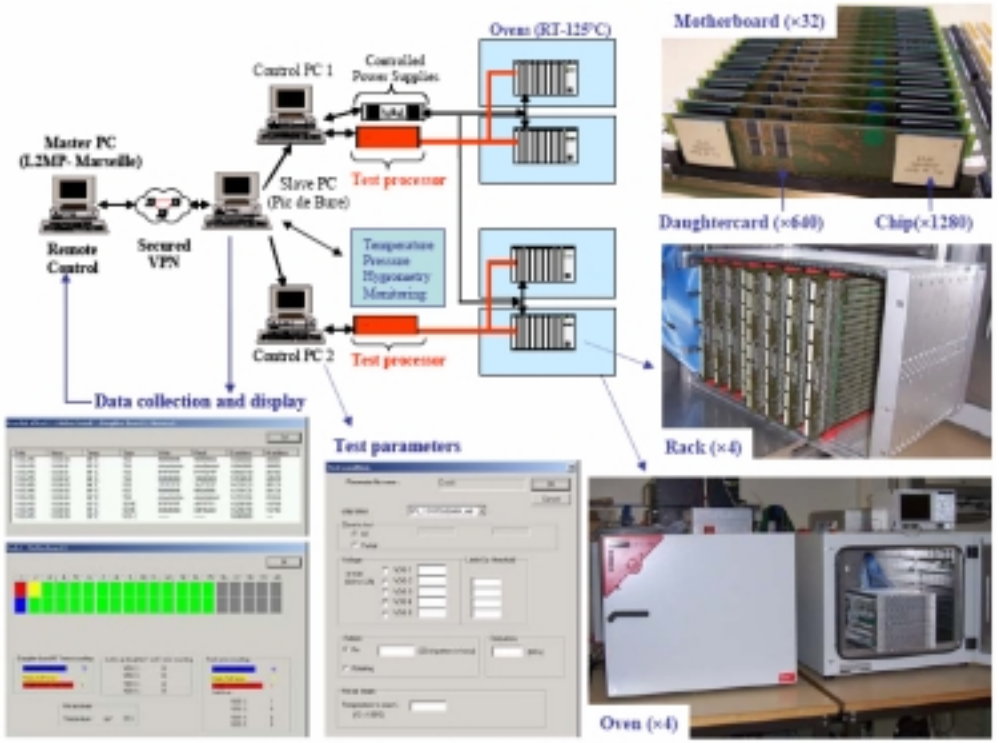
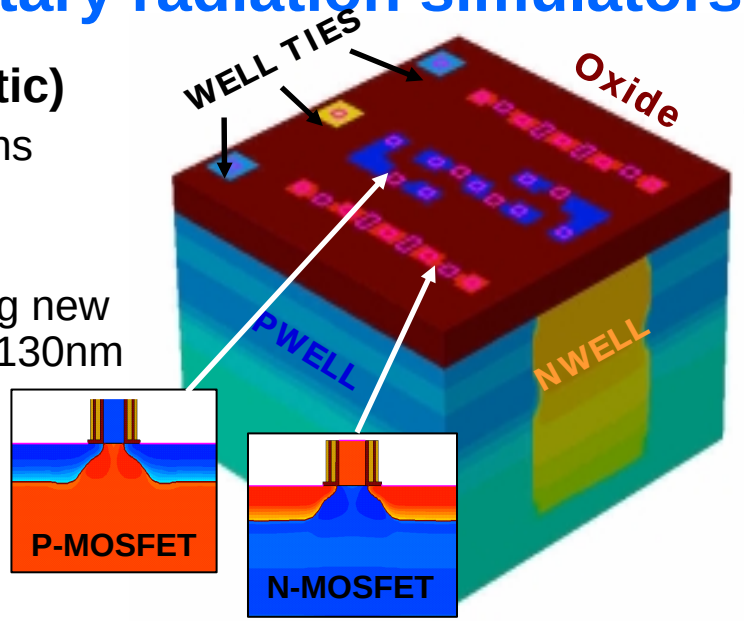


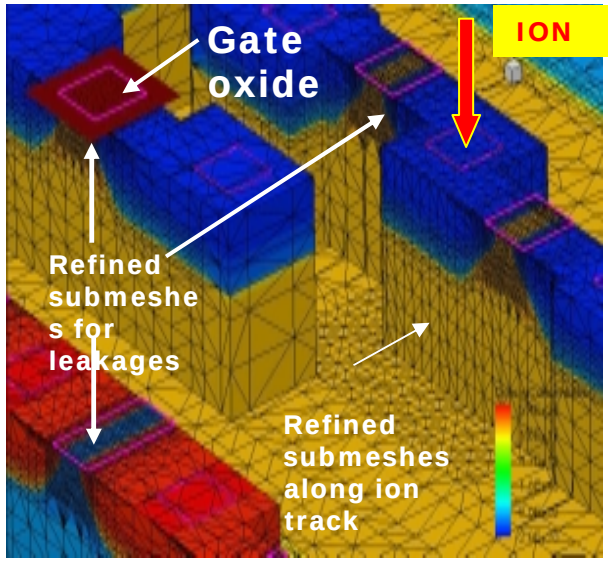
Figure 2. Schematic representation of the ASTEP Automatic Test Equipment (ATE).

ST original & proprietary radiation simulators (neutron, alpha, HI)

- **At device level (deterministic)**
  - 3D dynamic simulations of ions
  - Interest :insight into physical mechanisms causing upset
    - Mandatory for developing new hardening techniques < 130nm

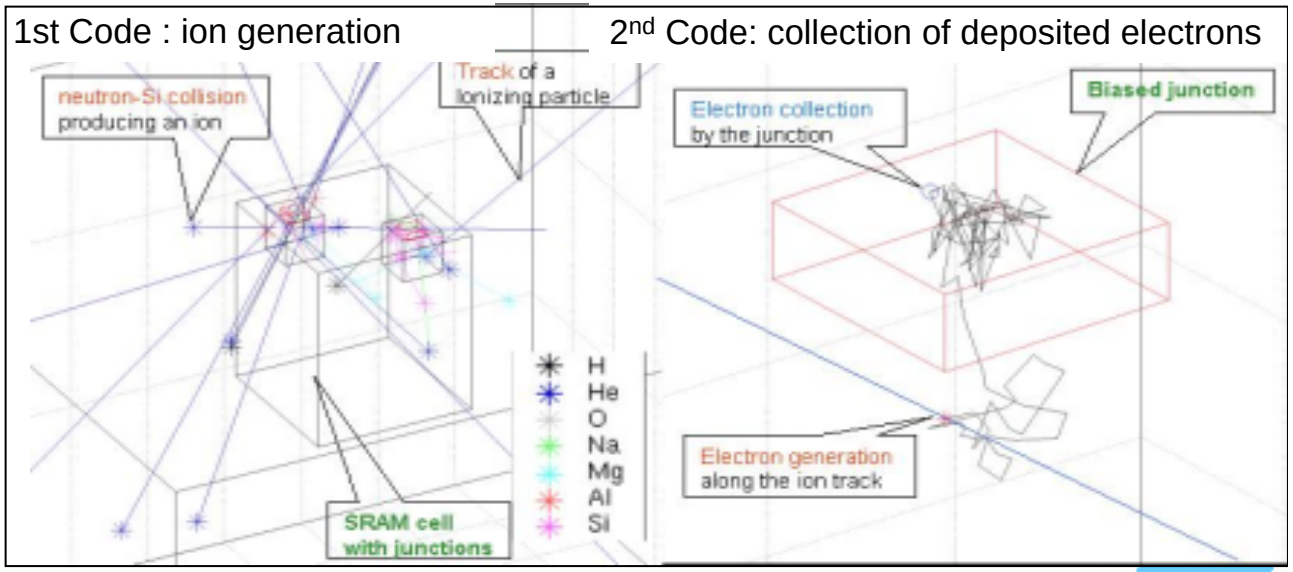
Rad-hard SRAM layout US patent number 2006/0,056,220 by P.Roche & F.Jacquet STMicroelectronics, France, 2006





90nm robust ST SRAM (12T)– 1,000,000 finite elements

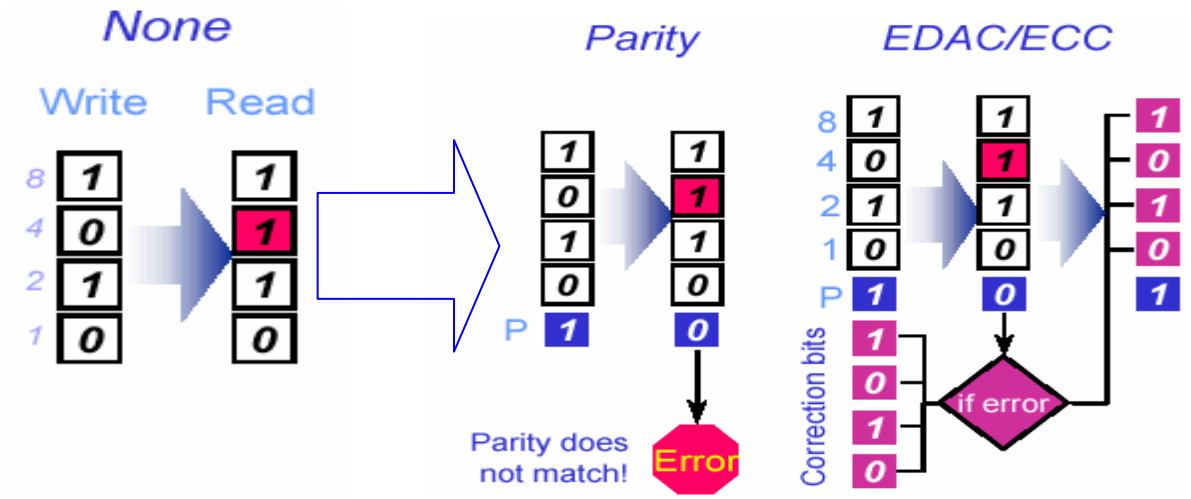
- **At chip level (statistical)**
  - Combination of proprietary Monte-Carlo codes and nuclear databases
    - Cf. NSREC'03 paper Roche et al.
  - Interest : quick & cheap assessment of fail rates in memory devices
    - Area, VDD, capacitor effects taken into account
  - An heavy ion code is being jointly developed by ST and CEM2 lab

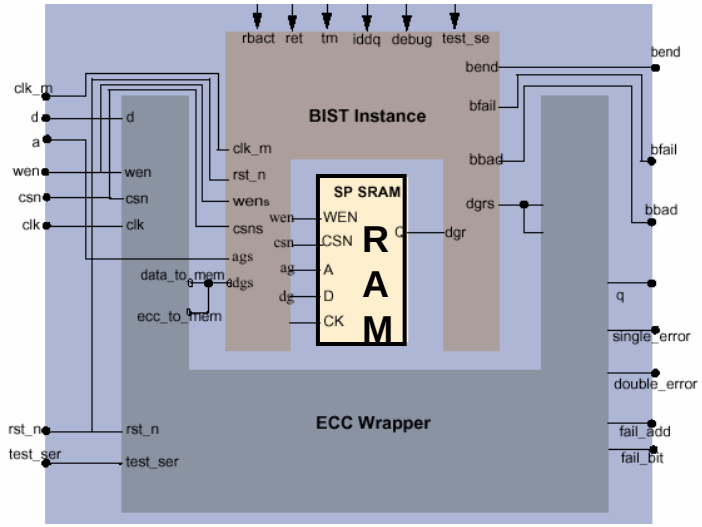


Examples of SER mitigation techniques at system level

- **RAM protected by Error Correction Codes (ECC) :** addition of parity or check bits

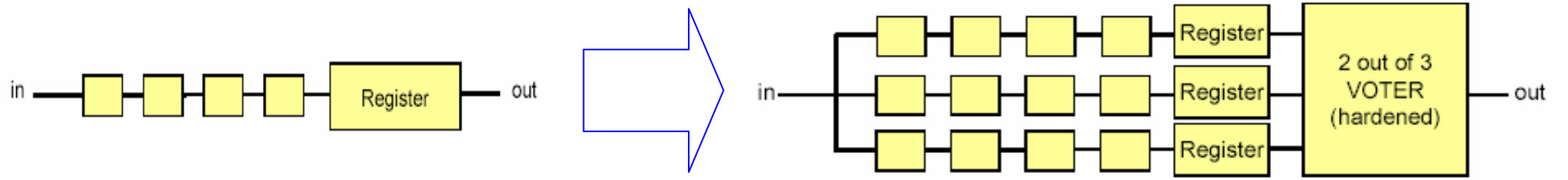
  ✓physical interleaving (physical separation of check bits) in conjunction with temporal scrubbing (periodical check for single error before a double error occurs in a same word)





ECC wrappers (and BIST) available in ST CMOS65

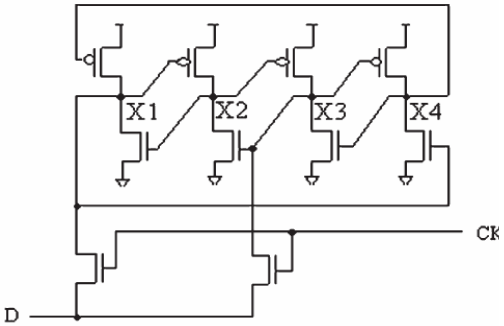
- **LOGIC protected by triple redundancy :** multiple identical logic paths feeding into a majority voting



ECC/EDAC available by default on ST eDRAM and as an option in ST eSRAM

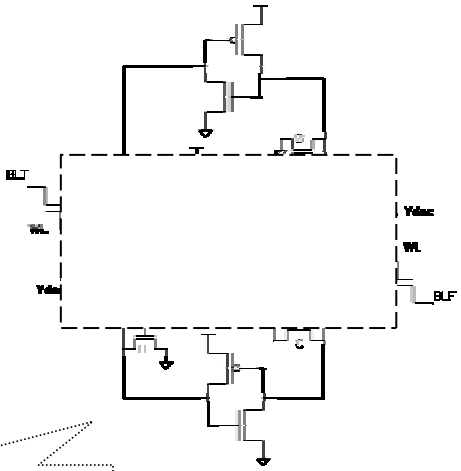
Examples of SER mitigations at device level with hardened cells

- **Example of SEU hardened static storage cell :** preserves the logic state even if one internal node is altered by ionizing particle strikes
  - Cons : area penalty
    - x2.5 for ST UHD 12T-SRAM in 90nm
  - Pros : used to protect SRAM, registers, BRAM, FFs
    - Rad-hard LAYOUT mandatory below 130nm
    - ST will be offering a robust library in CMOS65 in Q2'07



12T-SRAM cell schematic

US patent number 5,570,313, by P.Masson & R.Ferrant (ST) Thomson-CSF, France, 1996

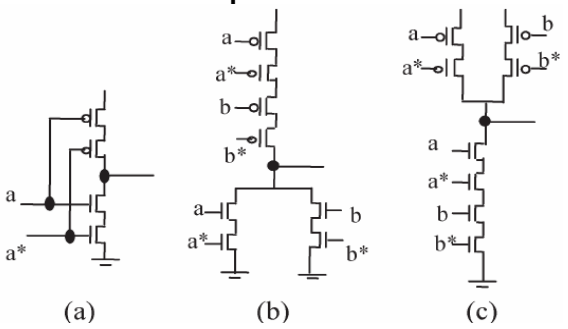


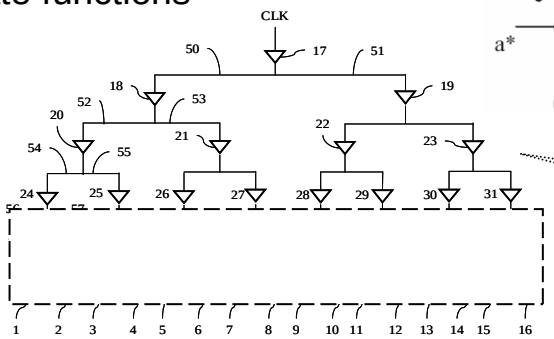
12T-SRAM cell schematic

Patent pending, by G.Gasiot & P.Roche STMicroelectronics, France, 2006

- **Examples of SET hardened cells :** maintain the previous output signal when one input of the dual to single path converter is impacted by ions
  - Cons : area penalty
  - Pros : radiation distortions cannot propagate through other logic elements because of the tri-state functions

>15 patents filed by ST-Crolles in hardening by design the past 6 years



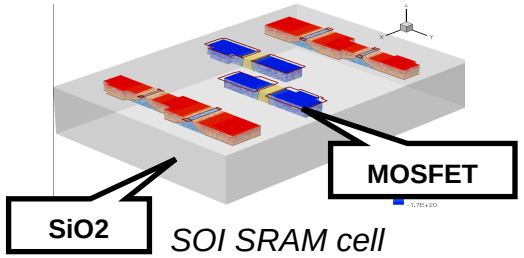


Robust clock tree Patent pending, by P.Roche & F.Jacquet STMicroelectronics, France, 2006

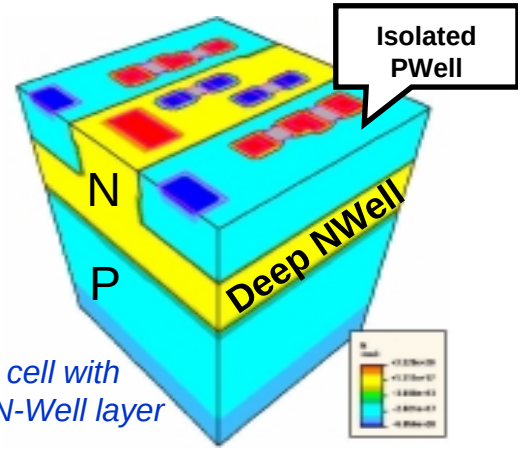
SER mitigation at technology level with standard process options

- **Comparisons of the relative effectiveness of standard process modifications for reducing the SRAM SER**
  - For CMOS 130nm/90nm technologies and below

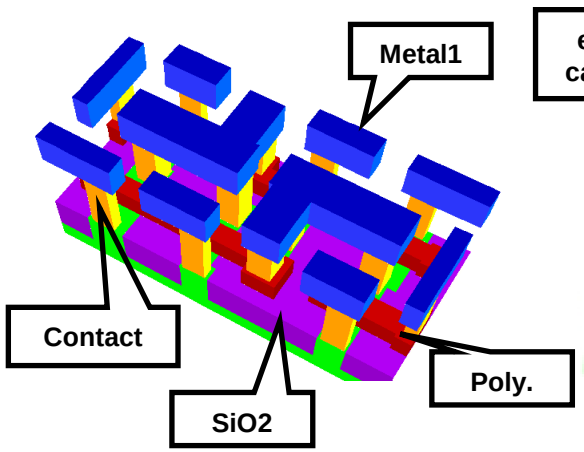
Process option	Relative SER*
Bulk General Purpose	reference : 100
Bulk Low Power	90
Deep N-Well (DNW)	60-75
Body tied PD SOI	<1
Floating body PD SOI	15-20
Fully Depleted SOI	10
Double Gate	2
Addition of two 3D eDRAM capacitors above the SRAM cell	0 (alpha) <1-10(neutron)

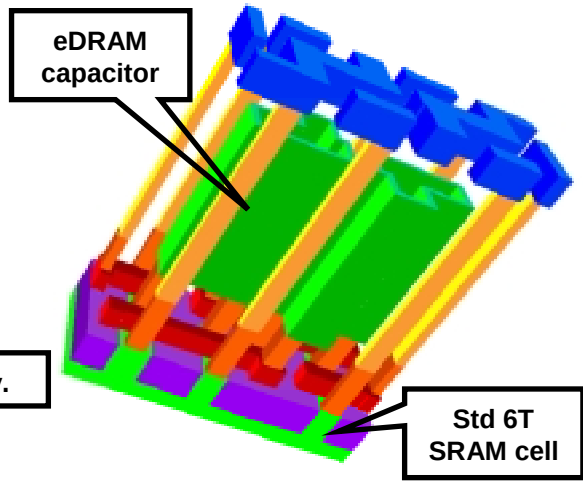


SOI SRAM cell



SRAM cell with Deep N-Well layer





Regular SRAM cell : 6T *ST Robust SRAM cell : 6T+2C (rSRAM™)*

- **Addition of big stacked capacitors (ST rSRAM™) allows for maximizing the SER reduction while not increasing the device area**

More details in : P.Roche et al., " Impacts of Front-End and Middle-End Process Modifications on Terrestrial SER" special issue on SER, ***IEEE TDMR*** *2005*

Intermediate conclusion : ST radiation characterization flow

- **is based on experimental tests (accelerated & real time)**
  - ten's of complex circuits already characterized In CMOS 250/180/130/90/65nm
    - Library Validation testchips
    - Specific SER testchips (robust SRAMs & Flip-flops)

- **uses original & proprietary simulators (deterministic & statistical)**
  - theoretical models have been co-developed with research labs since many years
  - 6 Ph.D programs sponsored by ST-Crolles for continuously improving the simulators

- **was already applied to ST CMOS 65nm with neutrons & alphas, and soon in 45nm**
  - 130nm/90nm CMOS : qualification completed in 2003-2005
  - 65nm CMOS : six 65nm complex testchips tested in North America and Crolles in 2005-2006
  - 45nm CMOS : new silicon available mid-March 2007

- **is compliant with international radiation test standards**
  - JEDEC for neutron & alpha : radiation tests & measurements of radioactive contaminants
  - ESA-SCC : to be made more explicit in the next part

Intermediate conclusion: ST radiation-hardened solutions

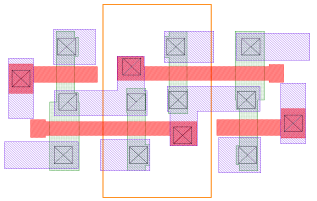
act at different levels and are available on request

- system level : with ECC wrappers (pipeline, fast access or low power schemes)
- device level : with restructured cells (addition of transistors)
  - Robust Library available in 65nm
- technology level : with 3D eDRAM cells added to the sensitive nodes

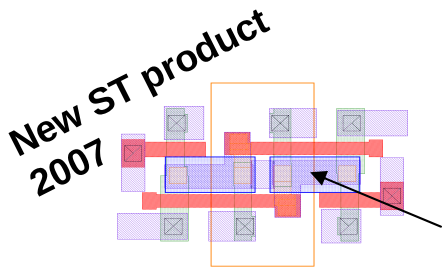
are original as for the rSRAM™ or rTCAM™ (addition in 3D of eDRAM caps)

- have successfully passed the reliability qualifications in 130nm and are being certified in 90nm
- combine very good electrical and radiation performances
- are officially part of ST technology programs in 130/90/65
- are embedded in consumer products in 90nm and 130nm CMOS (e.g. network or medical)

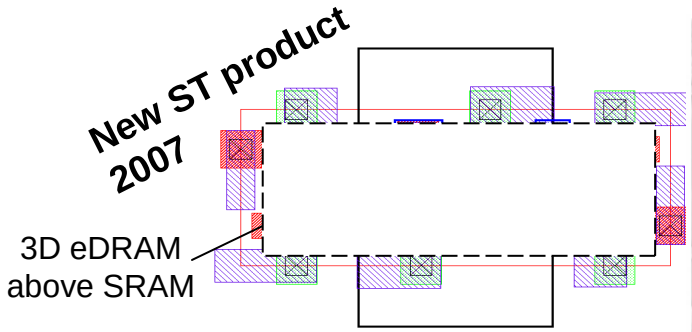
are mainly sized for the consumer market, but can be adjusted for more severe radiation environments



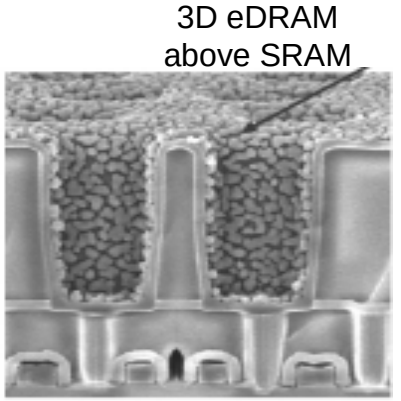
Standard SRAM
1 fF - 2.5µm2



Robust rSRAM™ network
36fF/cell - 2.5µm2



ULL Robust rSRAM™ medical
> 80fF/cell - 4µm2



SEM picture of the capacitor shape

Test parameters for the radiation assessment in 130 & 90nm

6 ST CMOS technologies measured : 4 core processes + 2 options

- 130nm CMOS SOI, General Purpose
- 90nm & 130nm CMOS Bulk, General Purpose & Low Power (higher Vth and thicker gate oxide)
- 90nm & 130nm eDRAM process options

8 complex & large circuits provided : Library Qualification & radiation testchips

- Circuits, test boards and test programs pre-validated with neutrons by ST-FTM and HIREX

40 IPs characterized under radiations : SRAM, DRAM, Flip-flops & TCAM

- Many different blocks (SRAMs, ROM, std cells, PLL, fuses, etc) powered during irradiations
- 4 SEE hardening solutions : optimized for consumer applications (NEUTRON IMMUNITY) not space

Main SEU & SEL parameters investigated :

- Doping profiles (Technology) : SEU charge collection & latchup
- Power Supply : different nominal VDDs (1V, 1V2) & I/Os biasing (1V2, 3V3)
- Device area : regular & UHD bitcells, 1P (single) & 2P (dual Port), DRAM, TCAM
- Chip-to-chip SEE variations : same devices in different testchips

Radiation test plan in 130nm & 90nm

- **2 samples of each of the 8 test structures were SEE tested with Heavy ions at**
  - HIF/UCL, Belgium and RADEF/Univ. of Jyvaskyla, Finland

Testchip features in 130n and 90nm

Name	Techno	Package	Pin #	Opening
QLIB	**90nm**	BGA-256+16	272	Chemical etch
RS90	**90nm**	BGA-256+16	272	mechanically
SERVAL90	**90nm**	BGA-256+16	272	mechanically
SER90	**90nm**	PGA-44	44	mechanically
CB75Q **SOI**	**130nm**	PGA-256	256	mechanically
SER130	**130nm**	QFP-100	100	mechanically
LARA	**130nm**	BGA-256+16	272	mechanically
NIRVANA	**130nm**	PBGA-292	292	mechanically

ST Test Matrix / Heavy Ion SEE Tests

Ion	LET MeV (mg/cm²)	SER 130	CB75QC MOS	CB75Q SOI	DRAM9	RS90	QIIIs90	SER90	SERV-AL90
JYFL – Ion Cocktail produced for ESA April 2005									
$^{15}N^{4+}$	1.8	xx		xx		xx	xx		
$^{20}Ne^{6+}$	3.9	xx	xx			xx	xx		
$^{40}Ar^{12+}$	10.2	xx	x			xx	xx		
$^{56}Fe^{15+}$	18.6	xx		xx					
$^{82}Kr^{22+}$	32.1	x				xx	xx		
$^{131}Xe^{36+}$	60.0			xx		x	xx		
UCL – Ion Cocktail #1 produced for ESA									
$^{15}N^{3+}$	2.9			xx				xx	xx
$^{20}Ne^{4+}$	5.8			xx					xx
$^{40}Ar^{8+}$	14.1			xx	xx			xx	xx
$^{84}Kr^{17+}$	34.0				xx			xx	xx
$^{132}Xe^{26+}$	55.9			xx					

- **2 types, one 90nm & one 130 nm, were also tested with protons at**
  - PIF/PSI, Switzerland
- **2 types, one 90nm & one 130 nm, were finally TID tested at**
  - ONERA, Toulouse, France

Main SEE test results in 130nm and 90nm

For 8 testchips tested with heavy ions
up to LET of 120 MeV/(mg.cm2)

&

For 2 testchips tested with protons
up to an energy of 60 MeV

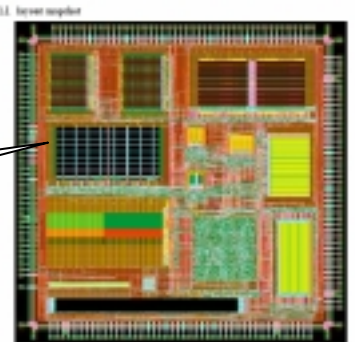
130nm SOI Library Qualification Testchip : regular & UHD SRAMs

Testchip features

-130nm SOI GP / VDD nominal 1.2V

-Many different blocks (SRAMs, ROM, std cells, PLL, etc) : all powered during irradiations

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
3x 1P-SRAM cell	2.50µm2	**3x 1Mb**	no	no	**Fast neutrons (1-800 MeV)**
1P-SRAM cell	2.09µm2 (UHD)	**1Mb**	no	no	



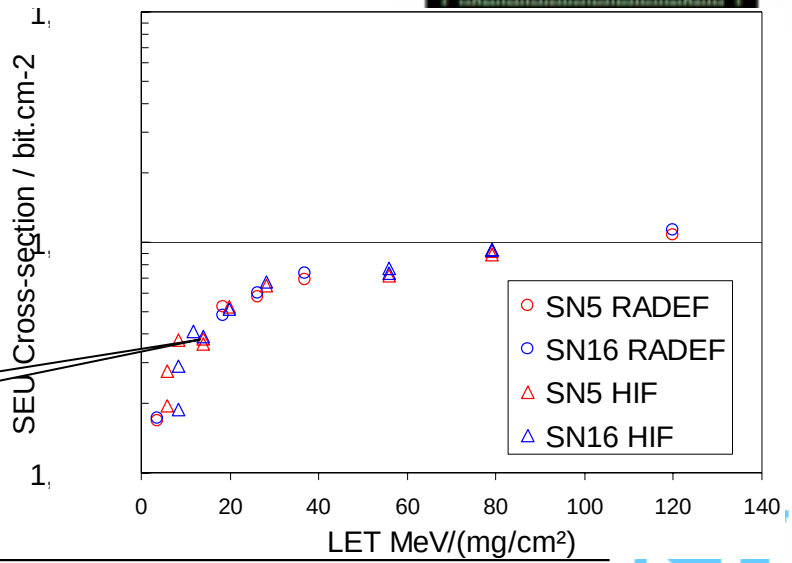
commercial SOI : same device area as in bulk (no body ties)

Main test parameters with heavy ions :

- 2 samples extensively tested at 2 radiation facilities
- VDD from 0.96 to 1.65V

Key test results with heavy ions :

- **SEU response** at VDD=1.2V :
  - Asymptotic cross-section : <1E-8 $cm^2.bit^{-1}$
  - No significant effect of the device area
- **no latchup** at 120 MeV/mg.cm^{-2}
- **no hard fail, large error or SEFI** at 120 MeV/mg.cm^{-2}



Excellent consistency of results with beams/samples/VDD/blocks

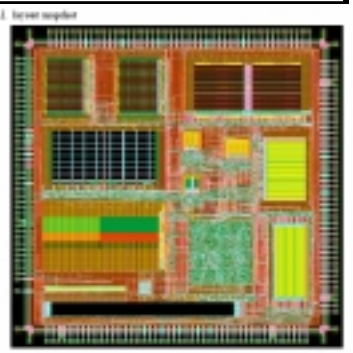
130nm SOI Library Qualification Testchip : regular & UHD SRAMs

Testchip features

-130nm SOI GP / VDD nominal 1.2V

-Many different blocks (SRAMs, ROM, std cells, PLL, etc) : all powered during irradiations

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
3x 1P-SRAM cell	2.50µm2	**3x 1Mb**	no	no	**Fast neutrons (1-800 MeV)**
1P-SRAM cell	2.09µm2 (UHD)	**1Mb**	no	no	



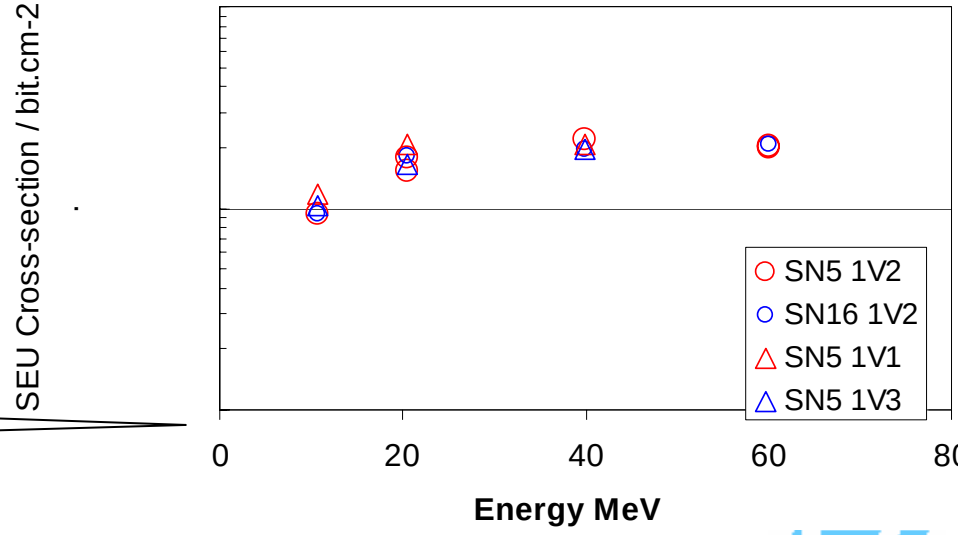
Main test parameters with PROTONS :

- 2 samples extensively tested
- VDD from 1.1V, 1.2V, 1.3V

Key test results with PROTONS :

- **SEU response** at 1.2V :
  - Asymptotic cross-section : ~1E-14 cm2.bit-1
  - No significant effect of the device area
- **no latchup** at 60 MeV (maximum energy used)
- **no hard fail, large error or SEFI** at 60 MeV

Excellent consistency of results with samples/VDD/blocks



130nm BULK eDRAM validation testchip

Testchip features

-130nm bulk GP / VDD nominal 1.2V and 3.3V (specific DRAM)

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
DRAM cell	0.53µm2	**3Mb**	Yes (ECC)	Yes	**Fast neutrons (1-800 MeV)** **Protons/neutrons at UCL** **Alpha particles**

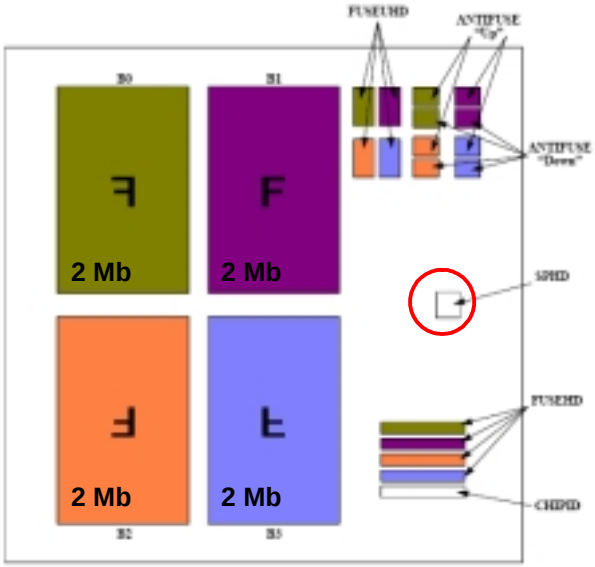
Main test parameters :

- 3 samples measured
- 2 different RAS conditions
- VDD set at 1V/3V (SEU Worst Case), few runs at 1.2V/3.3V (nominal)

Key test results with heavy ions :

- **in Worst Case SEU conditions** (VDD=1V, RAS=250ns) **with ECC deactivated :**
  - Asymptotic cross-section : ~**1.5E- 9 cm2.bit-1**

- **no hard fail** at 68 MeV/mg.cm^{-2} (max LET available)



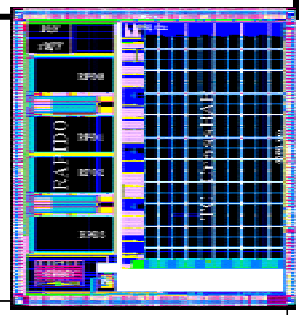
130nm BULK (1st) radiation testchip : regular & robust SRAMs

Testchip features

-130nm bulk GP / VDD nominal 1.2V

-Many different blocks (large SRAMs, std cells, PLL, etc) : all powered during irradiations

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
2 x 1P-SRAM cell	2.50µm2	**2 x 1Mb**	no	No / Yes	**Fast neutrons (1-800 MeV) + Alpha TID (1MradSi)**
2x Robust 1P-SRAM cell	2.50µm2	**2 x 1 Mb**	yes	No / Yes	



Main test parameters :

-2 samples tested

-VDD set at 1.2V

Estimated gain for the SEU rate in GEO ~10x with this 130nm rSRAM™

Key test results with heavy ions :

-**regular SRAM** / SEU response at 1.2V :

•Asymptotic cross-section : ~1E-7 $cm^2.bit^{-1}$

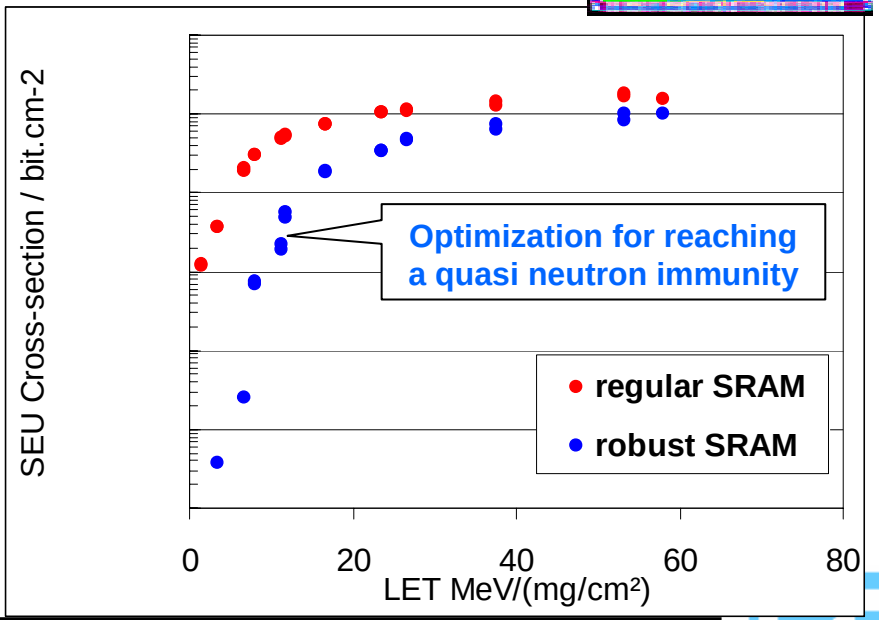
-**robust SRAM** (optimized for consumer products)

•Asymptotic cross-section : **improved by 3x**

•LET threshold : **increased by 10x**

-**no large error, hard fail or SEFI at 58 MeV/mg.cm-²**

-**no latchup at 58 MeV/mg.cm-²** (max LET available)



130nm BULK (2nd) radiation testchip : regular & robust Flip-flops

Testchip features

-130nm bulk GP / VDD nominal 1.2V

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
Standard Flip-flop (DF1)	28,24µm2	17,6K	No	No	**Alpha testing**
Standard Flip-flop (DF1)	28,24µm2	17,6K	No	Yes	
Robust rDF1	28,24µm2	17,6K / 17,6K	Yes	No/Yes	
Robust rDF1	28,24µm2	17,6K / 17,6K	Yes	No/Yes	
Robust 12T-DF1	2x DF1	6K / 6K	Yes	No/Yes	

Main test parameters :

- 2 samples tested
- VDD set at 1.2V with 3 test patterns

Key test results with heavy ions :

- **regular Flip-flops** / SEU response at 1.2V :
  - Asymptotic cross-sections : **2E-8 to 6E-8 $cm^2 \cdot bit^{-1}$**

- **robust Flip-flops** (terrestrial : no area penalty)
  - Asymptotic cross-sections : **improved by 2x - 10x**
  - LET threshold : **improved by 10x - 15x**

- **no latchup, hard fail or SEFI** at 64 MeV/mg.cm^{-2}

In 130nm regular Flip-flops are only 2-5x less SEU sensitive than SRAM cells

90nm BULK Library Qualification Testchip: regular 1P & 2P SRAMs

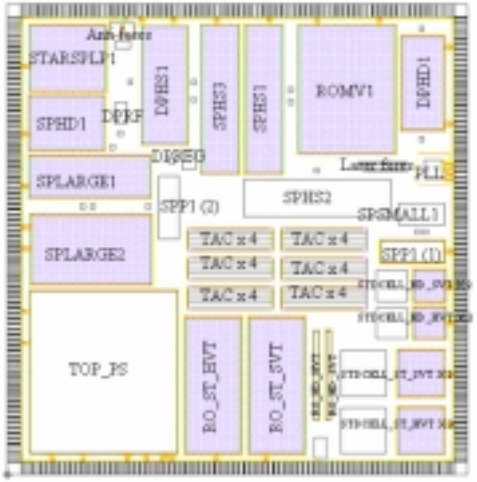
Testchip features

- 90nm bulk LP / VDD nominal 1.2V
- Many different blocks (SRAMs, ROM, std cells, analog, PLL, etc) : all powered during irradiations

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
1P-SRAM cell	1.15µm2	**1Mb**	no	no	**Fast neutrons (1-800 MeV)** **Alpha (5.4 MeV)**
2P-SRAM cell	2.07µm2	**2x 1Mb**	no	no	
1P-SRAM cell	1.15µm2	**2x 1Mb**	no	no	

Main test parameters :

- 2 samples extensively tested
- VDD set at 1V (nominal), few runs at 1.1V



Key test results with heavy ions :

- **1P-SRAM** / SEU response at 1.2V :
  - Asymptotic cross-sections : **2E-8 to 4E-8 $cm^2.bit^{-1}$**
- **2P-SRAM**
  - Asymptotic cross-section : slightly higher than 1P-SRAM
  - LET threshold : same as for the 1P
- **no hard fail, large error or SEFI at 120 MeV/mg.cm^{-2}**
- **no latchup at nominal VDD at 120 MeV/mg.cm^{-2}**

As 2P cell is larger than 1P its SEU sensitivity is higher

90nm BULK (1st) radiation testchip : regular Flip-flops

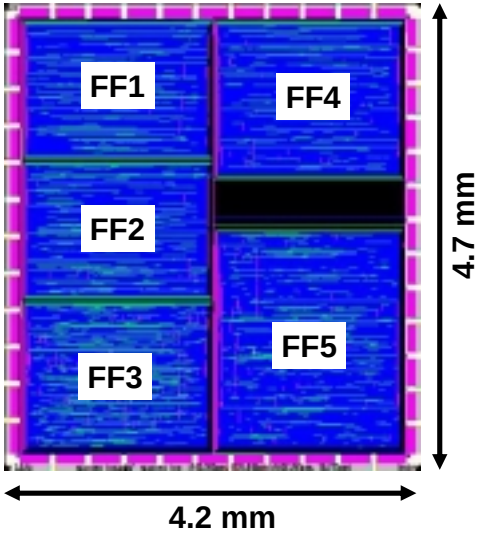
Testchip features

-90nm bulk LP / VDD nominal 1.2V

Cell	interest	Capacity	Hardening	Triple well	Other radiation test(s) performed
Standard Flip-flop (DF1QX05)	Ref.	100K	No	No	**Fast neutrons (1-800 MeV)** **Alpha testing**
Standard Flip-flop (DF1QX05V)	High VTh	100K	No	No	
Standard Flip-flop (DF1QX2 1)	high drive	100K	No	No	
Standard Flip-flop (DF2SQX05)	Std VTh	100K	No	No	
Standard Flip-flop (DF1SQY1)	HD	100K	No	No	

Main test parameters :

- 2 samples extensively tested
- VDD set at 1.2V with 3 test patterns and 2 clock states



Key test results with heavy ions :

- **Regular Flip-flops** / SEU response at 1.2V :
  - Asymptotic cross-sections : **6E-8 to 1E-7 cm².bit⁻¹**
- **no latchup, hard fail or SEFI at 68 MeV/mg.cm⁻²**

In 90nm regular Flip-flops are <u>more</u> HI sensitive than 90nm SRAMs & as sensitive as 130nm SRAMs

90nm BULK (2nd) radiation testchip : regular & robust rSRAM™

Testchip features

- 90nm Bulk GP / VDD nominal 1V
- Many different blocks (SRAMs, TCAM, Flip-flops, etc) : all powered during irradiations

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
1P-SRAM cell	**0.99µm2**	**1 Mb**	no	no	**Fast neutrons (1-800 MeV)** **Alpha (5.4 MeV)**
Robust UHD 1P-SRAM cell	**0.99µm2**	**1 Mb**	yes	no	
TerCAM cell	4.98µm2	288Kb + 512Kb	no	no	
Robust TerCAM cell	4.98µm2	288Kb + 512Kb	yes	yes	
Standard Flip-flop (DF1)		**64 Kbit**	no	no	
Robust Flip-flop	N/A	72Kbits	Yes	no	

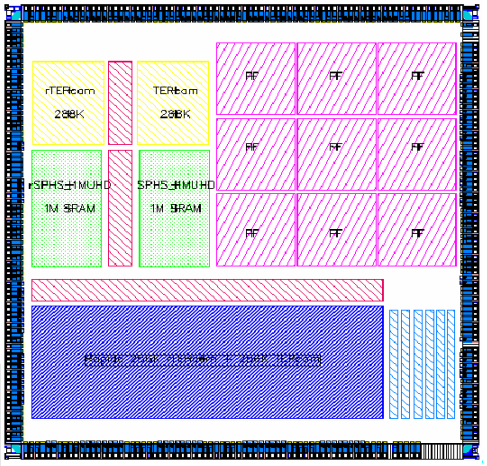
Main test parameters :

- 2 samples extensively tested
- VDD set at 1V (nominal), few runs at 1.1V and 1.2V

Key test results with heavy ions :

- **regular UHD SRAM** / SEU response at 1V :
  - Asymptotic cross-section : **5E-8 cm².bit⁻¹**
- **robust UHD rSRAM** (Ultra High Density)
  - Asymptotic cross-section : **improved by 3x**
  - LET threshold : **improved 5x**

HI SEU rates in orbits significantly reduced with 90nm rSRAM™



- **no large error, hard fail or SEFI at 68 MeV/mg.cm⁻²** (max LET available)
- **no latchup at nominal VDD at 68 MeV/mg.cm⁻²** (max LET available)

90nm BULK (2nd) radiation testchip : regular & robust rSRAM™

Testchip features

- 90nm Bulk GP / VDD nominal 1V
- Many different blocs (SRAMs, TCAM, Flip-flops, etc) : all powered during irradiations

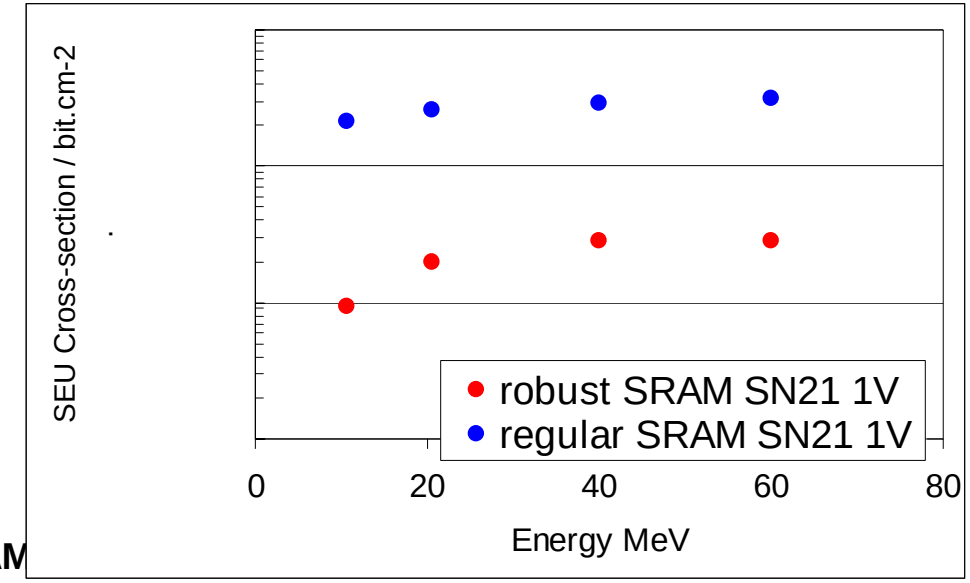
Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
1P-SRAM cell	**0.99µm2**	**1 Mb**	no	no	**Fast neutrons (1-800 MeV)** **Alpha (5.4 MeV)**
Robust UHD 1P-SRAM cell	**0.99µm2**	**1 Mb**	yes	no	
TerCAM cell	4.98µm2	288Kb + 512Kb	no	no	
Robust TerCAM cell	4.98µm2	288Kb + 512Kb	yes	yes	
Standard Flip-flop (DF1)		**64 Kbit**	no	no	
Robust Flip-flop	N/A	72Kbits	Yes	no	

Main test parameters with PROTONS :

- 2 samples extensively tested
- VDD set at 1V (nominal), at 0.9V and 1.1V

Key test results with PROTONS :

- **regular UHD SRAM** / SEU response at 1V :
  - Asymptotic cross-section : 3E-14 $cm^2.bit^{-1}$
- **robust UHD SRAM**
  - Asymptotic cross-section : **improved by 10x**
- **regular Flip-flop** / SEU response at 1V :
  - Asymptotic cross-sections : **x3 higher than SRAM**
- **no SEL, LE or SEFI at 60 MeV**



same as with HI

90nm BULK (3rd) radiation testchip : UHD SRAM with buried layer

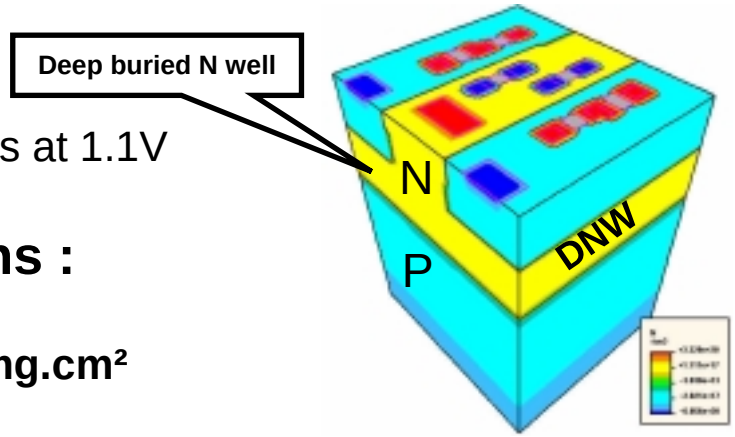
Testchip features

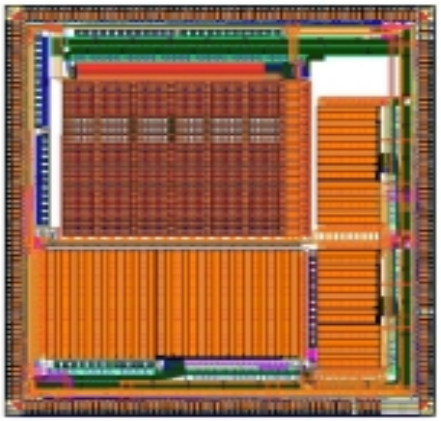
- 90nm Bulk LP / VDD nominal 1.2V
- Many different blocs : all powered during irradiations

Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
Robust* UHD 1P-SRAM cell	**1.15µm2**	**4Mb**	yes	yes	**Fast neutrons (1-800 MeV)** **Alpha (5.4 MeV)**
Robust UHD 1P-SRAM cell*	*1.15µm2*	*2x1Mb*	*yes*	*yes*	
Standard 1P-SRAM cell	*1,15µm2*	*1.16 Mb*	*no*	*yes*	
Robust TerCAM cell*	*1.15µm2*	*1.16 Mb*	*yes*	*yes*	
Standard 1P-SRAM cell	*0.99µm2*	*0.53 Mb*	*no*	*yes*	
Robust TerCAM cell*	*0.99µm2*	*0.53 Mb*	*yes*	*yes*	

Main test parameters :

- 2 samples extensively tested
- VDD set at 1.2V (nominal), few runs at 1.1V



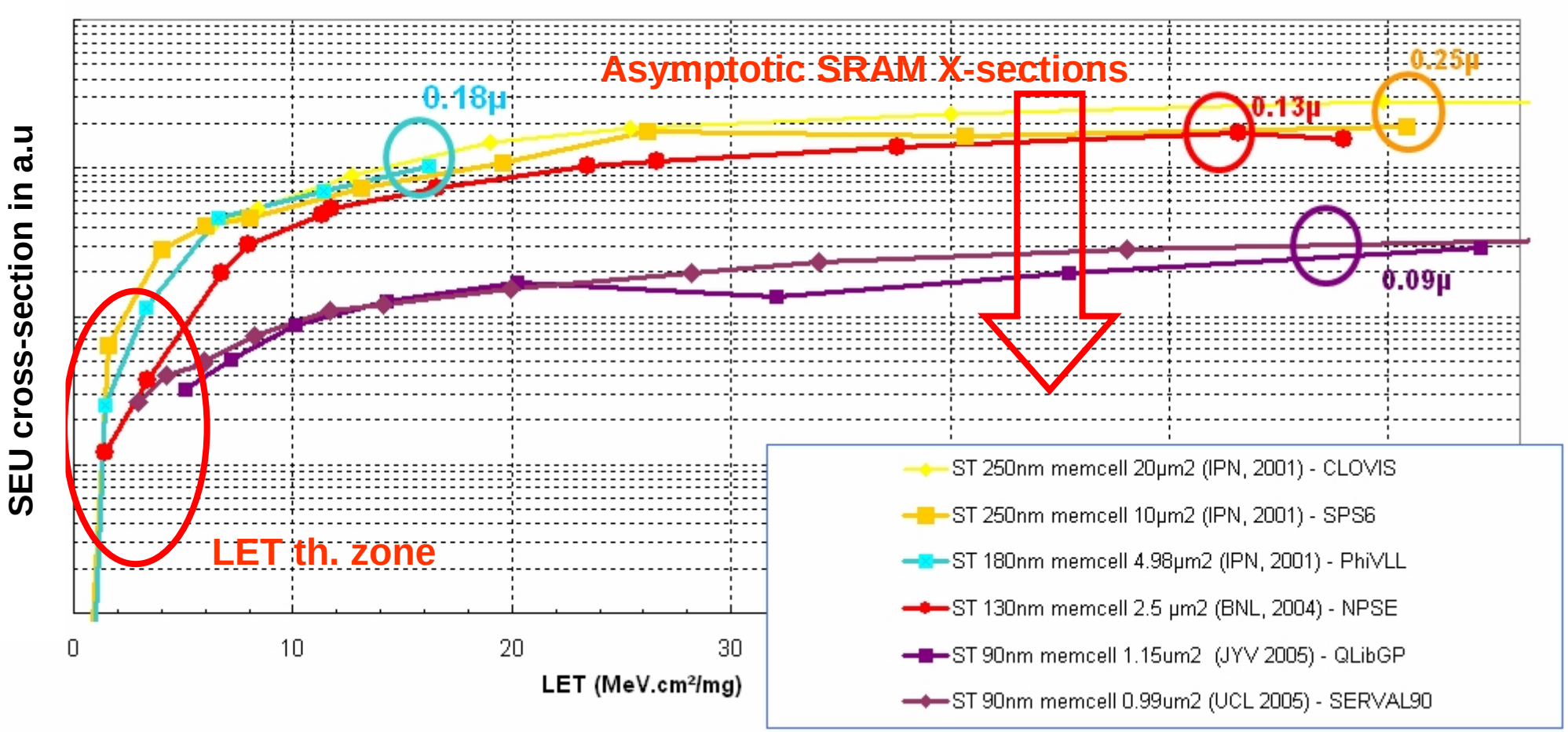


Key test results with heavy ions :

- **no hard fail or SEFI at 120 MeV/mg.cm²**
- **no latchup at nominal VDD, 1.2V, at 120 MeV/mg.cm-²**

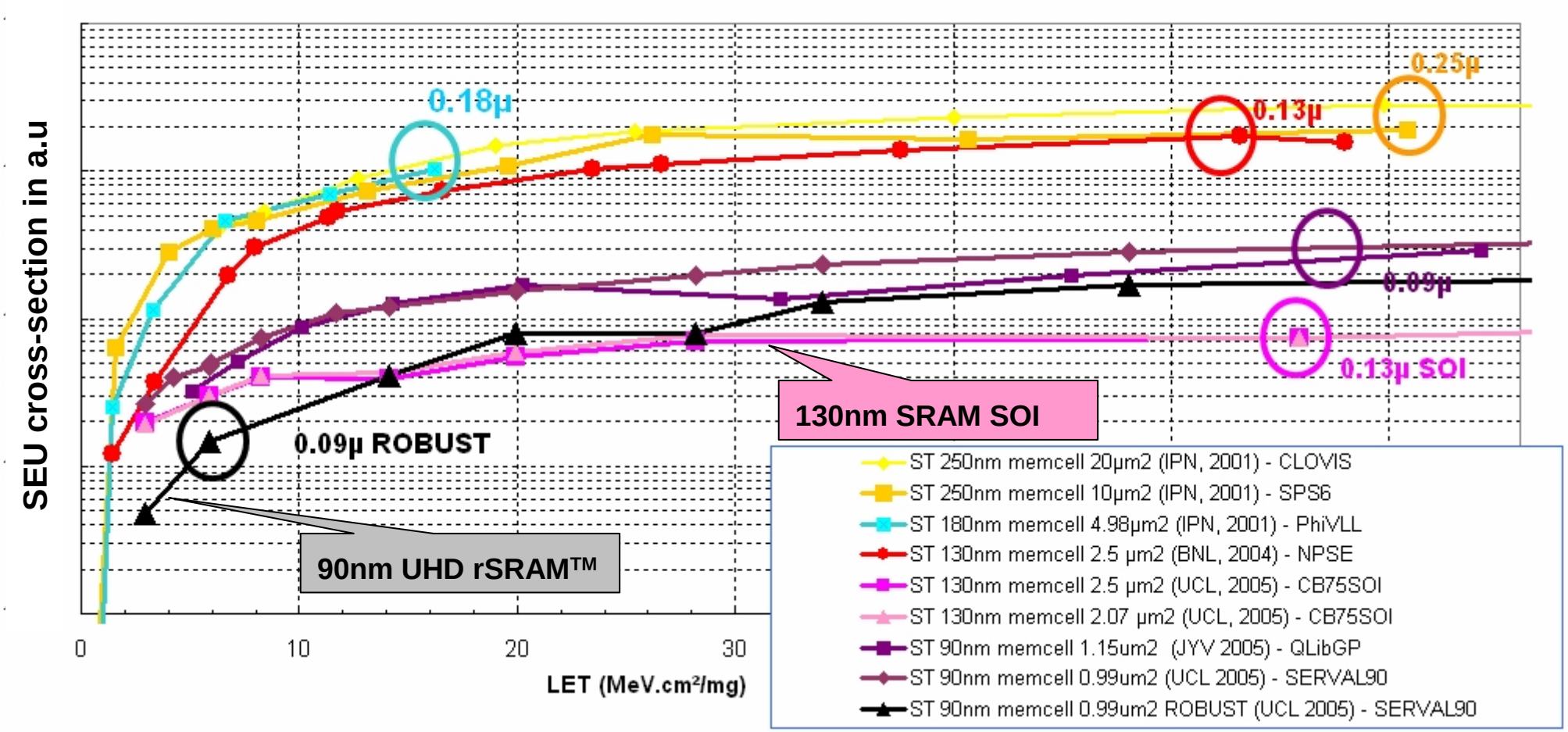
the Deep N-Well process option enables to get a complete SEL immunity in ST CMOS090

Conclusion on SEU testings : from ST CMOS 250nm to 90nm



- **SEU susceptibility (per bit) decreases as the technology (memory cell area) scales down**
- **Flip-flops have however become 2x to 3x more SEU sensitive than SRAMs in 90nm**
  - ✓radiation-hardened solutions exist (ST rFF™ or 12T-FF)

Conclusion on SEU testings : CMOS 130nm and 90nm

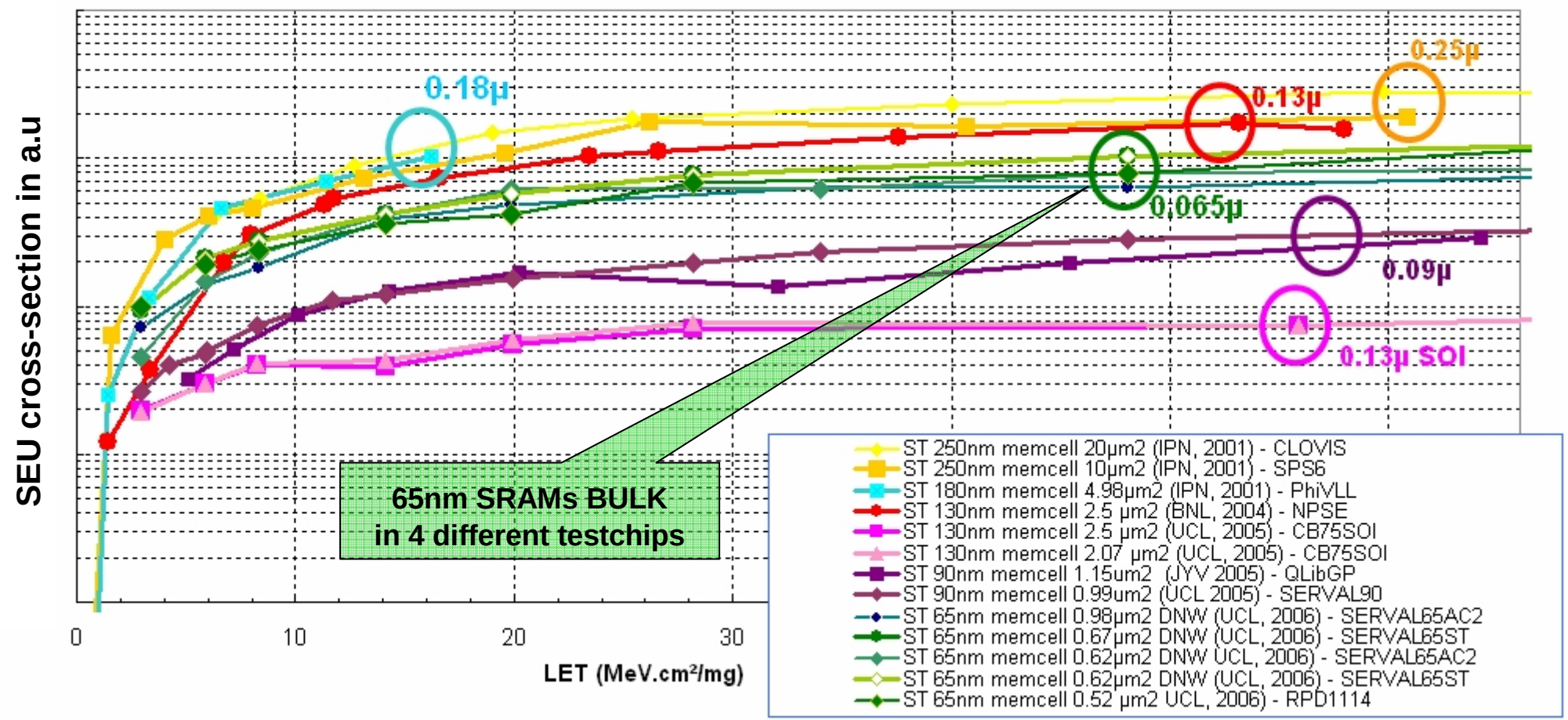


- For the tested 130nm/90nm circuits, the best SEE robustness was measured on :
  - 90nm UHD BULK SRAM protected by 3D eDRAMs
  - 130nm SOI SRAM

- ST CMOS 90nm remains fully functional & reliable even under extreme ion bombing
  - no hard-fail or chip functional interrupt up to LET of 120 MeV/mg.cm-2

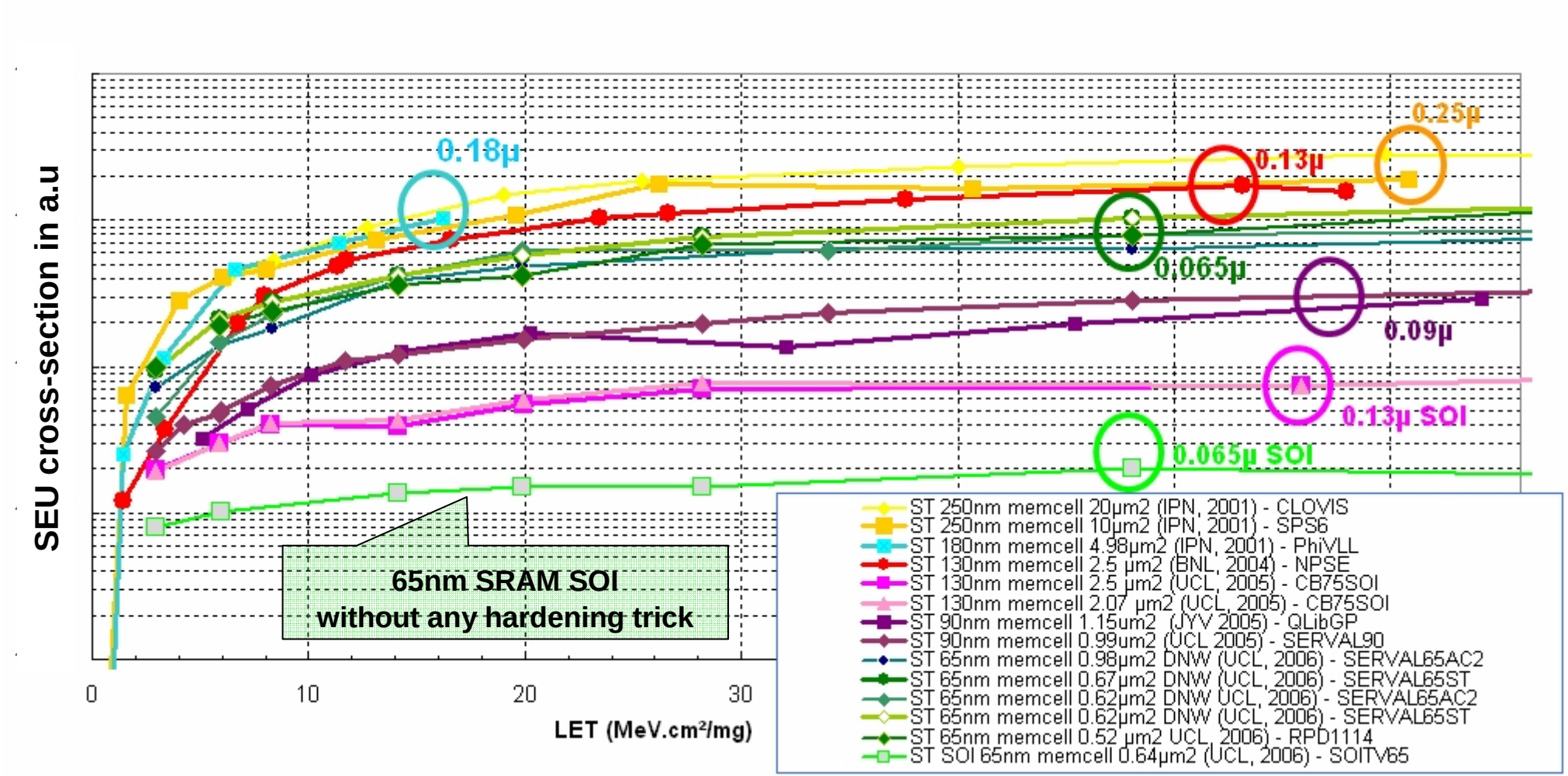
Conclusion on SEU testings : CMOS 65nm BULK (Preliminary)

- 5 testchips CMOS65, embedding non-hardened RAMs & FFs, measured at UCL end of 2006



- **Cross-sections in 65nm are in-between 130nm and 90nm because of a stronger MBU contribution**
  - 80% of MBUs at LET of 14.1
  - 95% of MBUs at LET of 19.9
  - 98% of MBUs at LET of 34
- **ST CMOS 65nm remains fully functional at LET of 68 MeV/mg.cm-2 (max. LET available at UCL)**

Conclusion on SEU testings : CMOS 65nm SOI (Preliminary)



- **The SOI 65nm showed the strongest robustness among all tested SRAMs (w/o hardening trick)**
  - positive conjunction of a very small silicon film with a weak parasitic bipolar transistor
  - **MBU < 5-10%** for all LET / tilts – even at 68 MeV/cm2.mg with 60°
- **Next steps of the ST 65nm radiation assessment in 2007: protons, HI (up to LET of 120) and Co60**

TID test results in 130nm & 90nm

for 2 testchips tested with gamma rays up to 100krad$_{Si}$

+ earlier test results in the Mrad$_{Si}$ regime

130nm Bulk Library Qualification Testchip

Testchip features

-130nm Bulk GP (General Purpose) / VDD nominal 1.2V

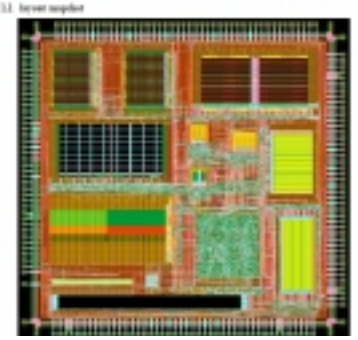
-**Many different blocks (SRAMs, ROM, std cells, PLL, etc) : all powered during irradiations**

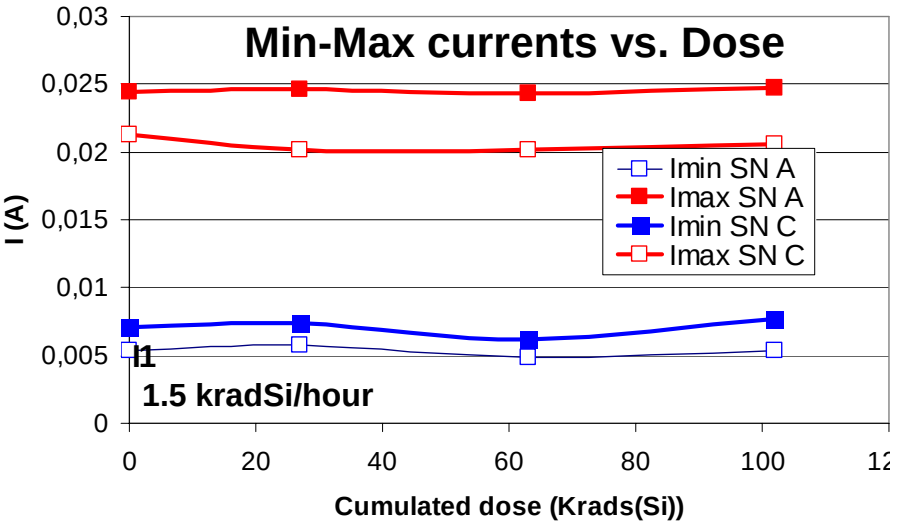
Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
3x 1P-SRAM cell	2.50µm2	3x 1Mb	no	no	**Fast neutrons (1-800 MeV)**
1P-SRAM cell	2.09µm2 (UHD)	1Mb	no	no	

Main test parameters with gamma source :

- 2 samples irradiated up to 100 kradSi + 24h at ambient
- VDD set to 1.2V, static & dynamic (5 MHz) testing

S/N	Run	Time (hours)	Cumulated dose (krads(Si))	Test Mode	Bias	result
A		0	0	Dynamic	On	fully functional
A	1	18	27	Dynamic	On	fully functional
A	4	42	63	Dynamic	On	fully functional
A	5	68	102	Dynamic	On	fully functional
C		0	0	Static	On	fully functional
C	7	18	27	Static	On	fully functional
C	9	42	63	Static	On	fully functional
C	12	68	102	Static	On	fully functional
C	13	92	Annealing at ambient (24h)	Static	On	fully functional





Key test results :

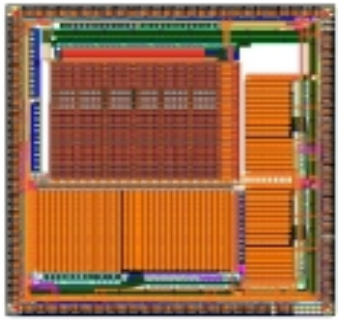
- **No significant current increase for the core VDD**
  - 2x drift max for VDD I/O (3.3V on thick gate oxide)
- **Devices were 100% functional** after 100kradsSi & 24h of annealing at ambient temperature

90nm BULK specific SER testchip

Testchip features

- 90nm Bulk, option LP (Low Power) / VDD nominal 1.2V
- **Many different blocks (SRAM blocs) : all powered during irradiations**

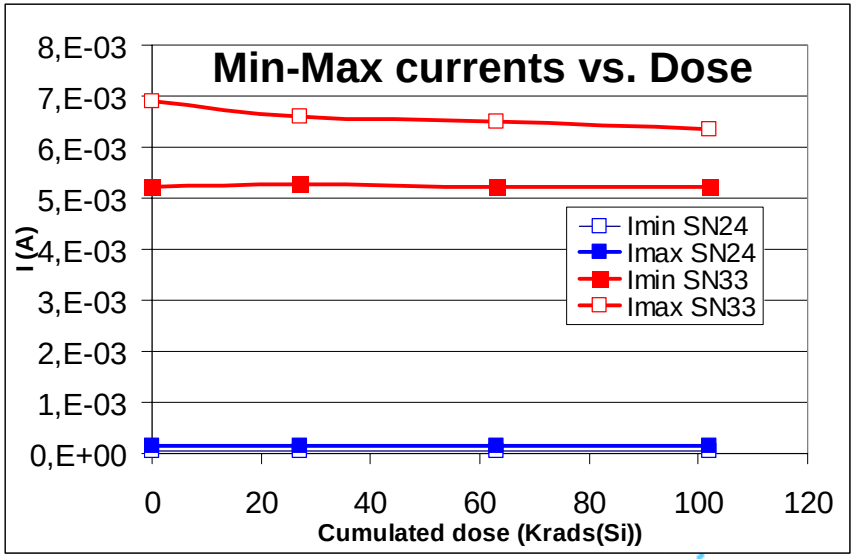
Cell	Area	Capacity	Hardening	Triple well	Other radiation test(s) performed
Robust* UHD 1P-SRAM cell	1.15µm2	4Mb	yes	yes	**Fast neutrons (1-800 MeV)** **Alpha (5.4 MeV)**



Main test parameters with gamma source :

- 2 samples irradiated up to 100 kradSi + 24h at ambient
- VDD set to 1.2V, static & dynamic (5 MhHz) testing

S/N	Run	Time (hours)	Cumulated dose (krads(Si))	Test Mode	Bias	result
24		0	0	Static	On	fully functional
24	2	18	27	Static	On	fully functional
24	3	42	63	Static	On	fully functional
24	6	68	102	Static	On	fully functional
33		0	0	Static	On	fully functional
33	8	18	27	Static	On	fully functional
33	10	42	63	Static	On	fully functional
33	11	68	102	Static	On	fully functional
33	14	92	Annealing at ambient (24h)	Static	On	fully functional



Key test results :

- **No current increase** after 100kradsSi
- **Devices were 100% functional** after 100kradsSi & 24h of annealing at ambient temperature

Similar extreme TID robustness in the Mrad regime for ST 130nm

- **Linear transistors ST 130nm with thin gate oxide irradiated up to 30 MradSi**
  - ✓ Threshold voltage shift < 10 mV : negligible
  - ✓ Subthreshold swing variations : negligible
  - ✓ Transconductance degradation of less than 10%

- **Linear transistors ST 130nm with thick gate oxide irradiated up to 30 MradSi**
  - ✓ Threshold voltage shift < 35 mV : negligible
  - ✓ Transconductance degradation of less than 10%

- **Two SRAMs 1Mb ST 130nm, standard and rSRAM^{TM}, irradiated up to 1 MradSi**
  - ✓ No bit error detected for each memory cut
    - at initial and after each exposure step (0, 100, 500 and 1000Krads(Si))
  - ✓ Full functionality of the 2 cuts after being exposed to a cumulative dose of 1Mrad(Si).

Whatever the γ or X-ray source, dose rate, cumulative dose, or type of device the tested ST 130nm & 90nm circuits are extremely TID resistant
(without any guard rings or edgeless transistors)

General conclusion for ST CMOS 130 and 90nm

- **The radiation testings were jointly performed by ESA-ESTEC, ST-FTM and HIREX for 1 year on**
  - **8 testchips during 2 HI campaigns in Belgium and Finland**
  - **2 testchips during 1 proton campaign in Switzerland**
  - **2 testchips with gamma rays in France**

- **More than 350 test runs and 1800 log files were analyzed**

- **The test results have shown for the commercial (non hardened) 130 and 90nm ST devices**
  - **no dose issue**
    - devices 100% functional after 100kradsSi & 24h of ambient annealing
  - **no hard fail occurrence or SEFI**
    - up to 120 MeV/mg.cm^{-2}
  - **no latchup with protons**
    - up to 60 MeV
  - **no latchup with heavy ions in 130nm BULK & SOI**
    - up to respectively 64 & 120 MeV/mg.cm^{-2}
  - **no latchup with heavy ions in 90nm BULK**
    - up to 120 MeV/mg.cm^{-2} at nominal VDD
  - **the best SEU robustness for the 90nm UHD rSRAM™ & 130nm SOI SRAM**
    - SEU rates very likely decreased by several decades

- **First HI tests on 5 ST 65nm testchips have already demonstrated a good reliability and hardness**