Technology needs for new computer developments at RUAG Space

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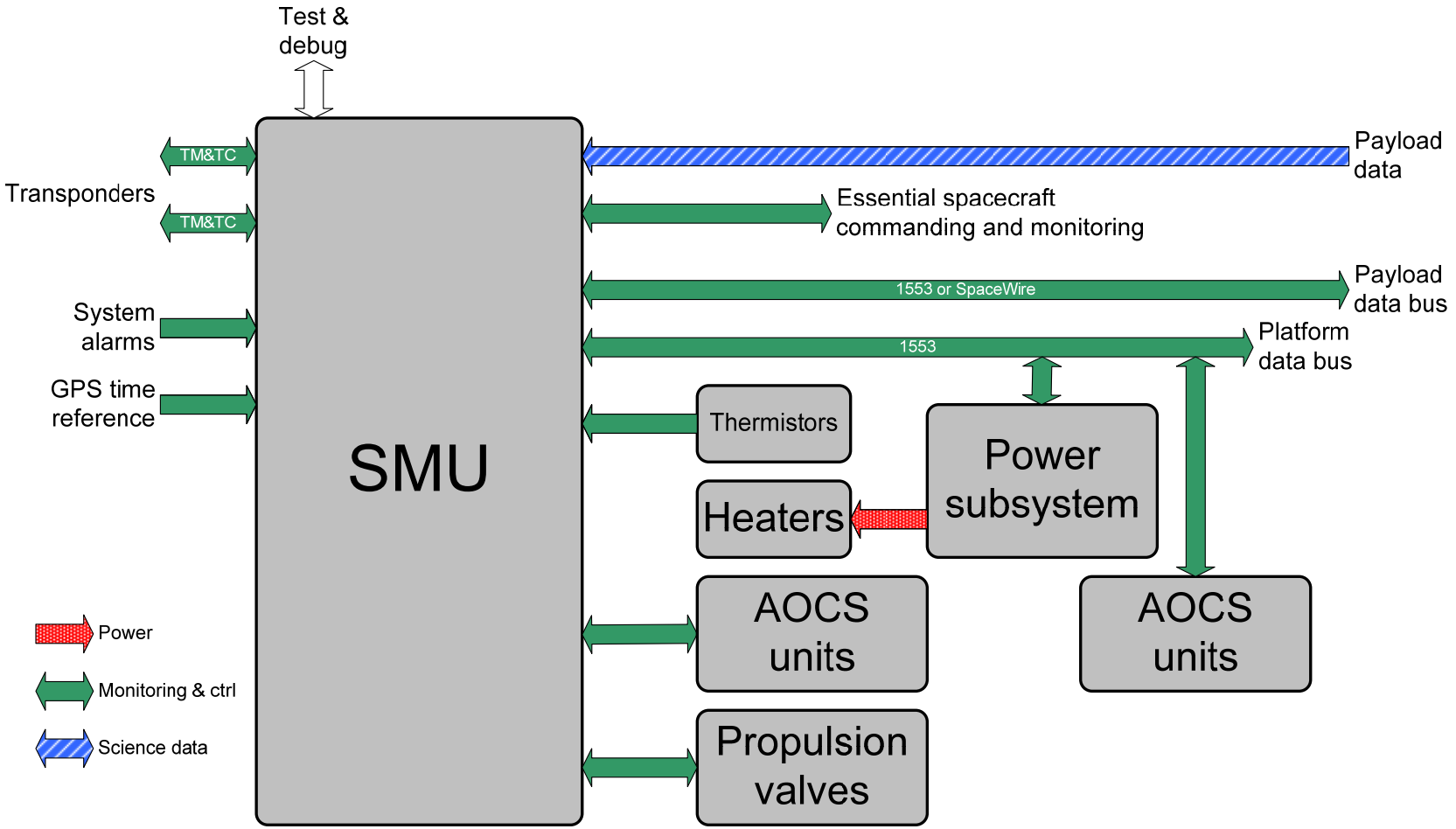
What is an SMU?

- Spacecraft Management Unit (SMU) tasks
  - Ground protocol handler, Telecommand and Telemetry
  - Processing capability and application program interface
  - Timing and synchronisation management
  - Mass memory (platform memory or small science data memory)
  - Discrete I/O interfaces (standard I/O, AOCS, propulsion)
  - Fault Detection, Isolation and Recovery (FDIR) to supervise and manage the processing function

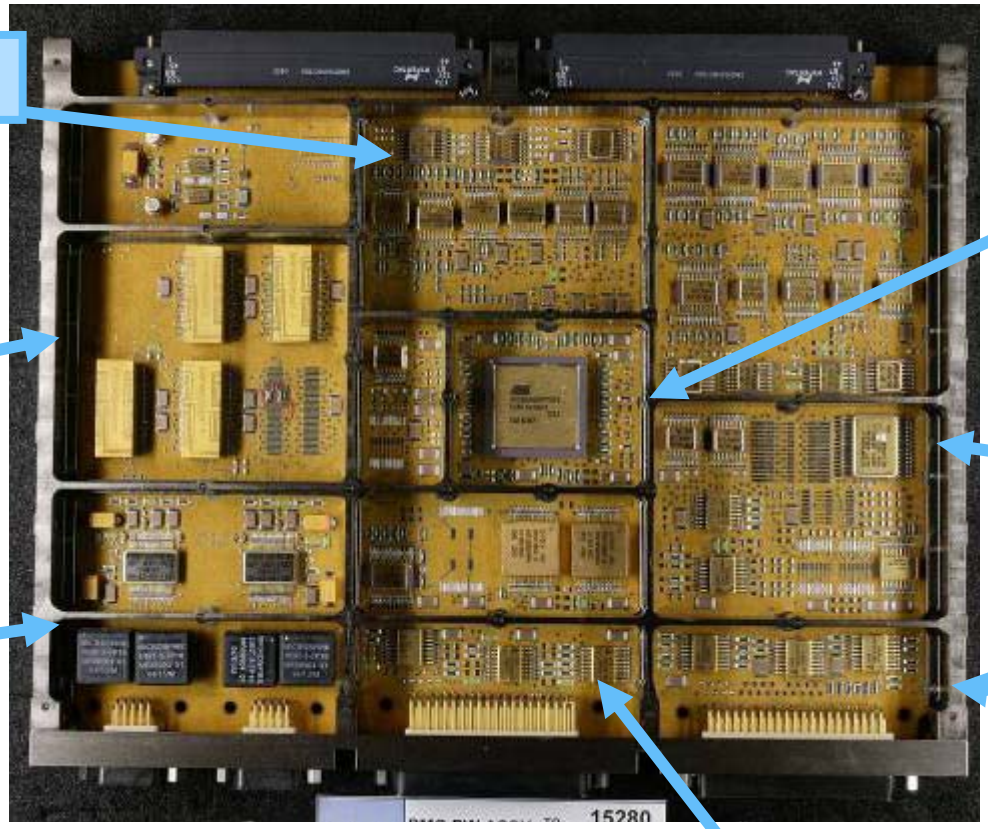
The SMU location in the spacecraft



Computer technologies in use

- Basic key technologies for current computer generation
  - Rad hard ASIC technology with 0.35 and 0.18 µ feature size
  - Mixed ASIC technology 0.35µ and larger
  - PROM, EEPROM, SRAM, SDRAM and Flash memories
  - Analog multiplexers
  - FET transistors of various sizes
  - XO, TCXO and sometimes OCXO
  - Interface circuits for RS-422, LVDS, 1553 and sometimes RS-485
  - Printed circuit boards with dual-sided mounting and up to 18 layers using buried via holes
  - HDD and MDM type external connectors

Typical processor board



Problem areas

- For “discrete” ICs, packages from the 70-ies still used
  - 1 mm^2 chip becomes 200 mm^2 board area
- Rising vibration and shock requirements
- ECSS standardisation efforts not always reflected in available technology:
  - SpaceWire: No European LVDS supplier
  - Discrete I/F: No European RS-422 I/F supplier
  - CAN: Old RS-485 technology still used
  - 1553: European alternatives exist, but with problems

Problem areas cont'd

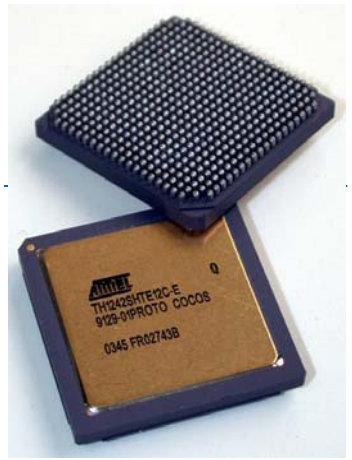
- No European low cost ASIC capability
- No European PROM capability
- Paper administration when using "new" technology
- Non-standardised functionality prevents investments in new technology
- Short technology lifetime is not compatible with end customer needs for qualified products
- Is the space industry even losing its position as leaders in trailing edge technology ?

Current trends

- Single source is becoming more common
- European supply of complex functions like ASICs and FPGAs is fading
- Commercial evolution towards lead-free processes affects parts availability and drives process development

- Or is this just extending the problem list ?

Package pin count evolution

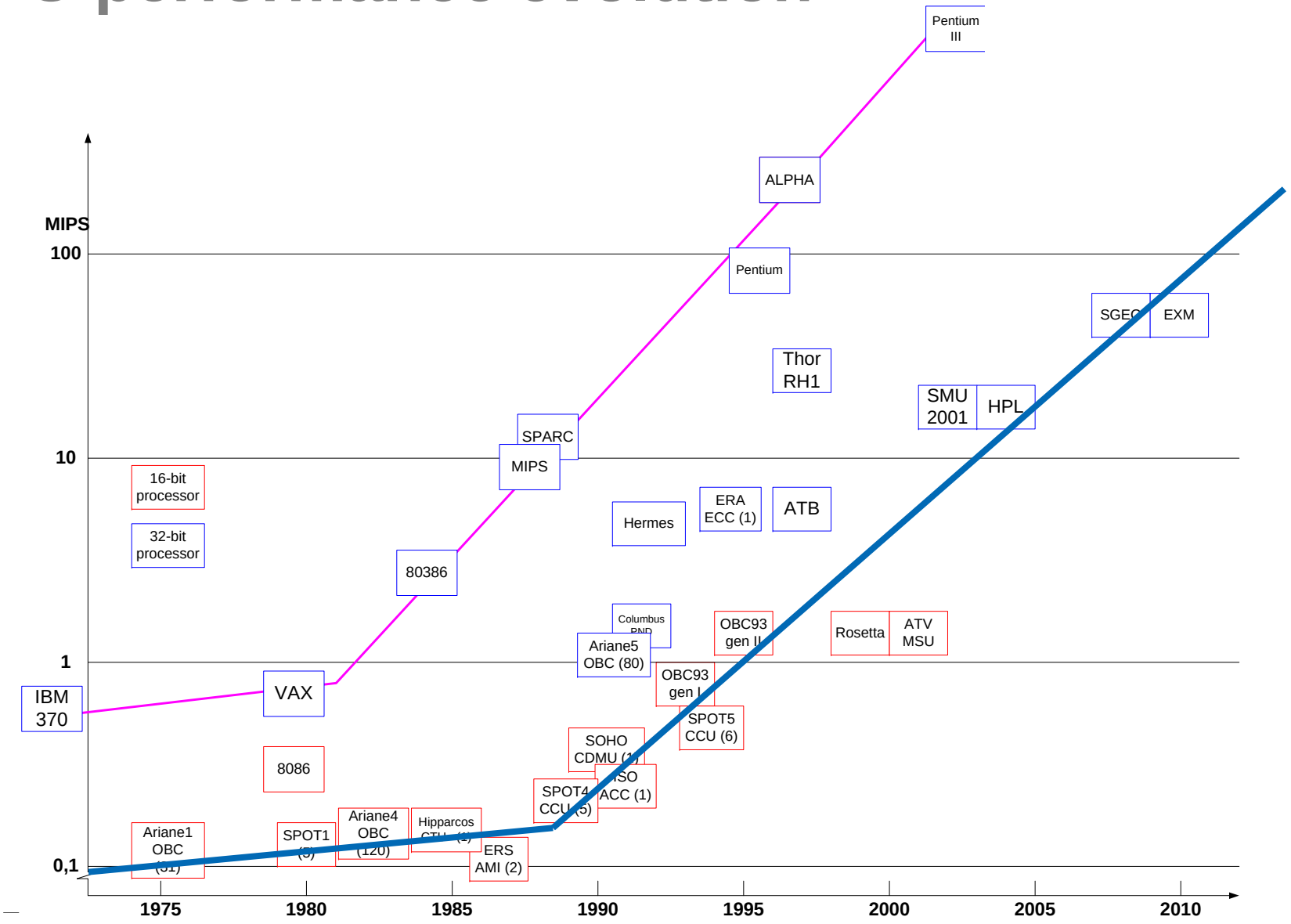


When will we hit this line?

1000
300
100
30
10

1975
1985
1995
2005
2015

CPU performance evolution



How to meet future challenges

Requirements	Developments
☝ Lower mass and power	➢ More integrated ASICs ➢ Work with 3D stacking technology ➢ Work on methods to solve the repair problem
☝ Higher performance	➢ Prepare for multi-core CPU ➢ Fast communication link architectures
☝ Increased functionality	➢ More integrated ASICs ➢ Flexible IP blocks ➢ Support standardisation activities

Investments needed at design house level

- Solve the problem areas, e.g. reliable non-volatile storage
- Master new Deep Submicron technology
  - Design process
  - Fault models and reliability
- Master “rad-hard by design” techniques
- Master spin-in of commercial technology
  - Opportunistic process since we cannot influence the development
- Master more compact packaging

Thank you for your attention!