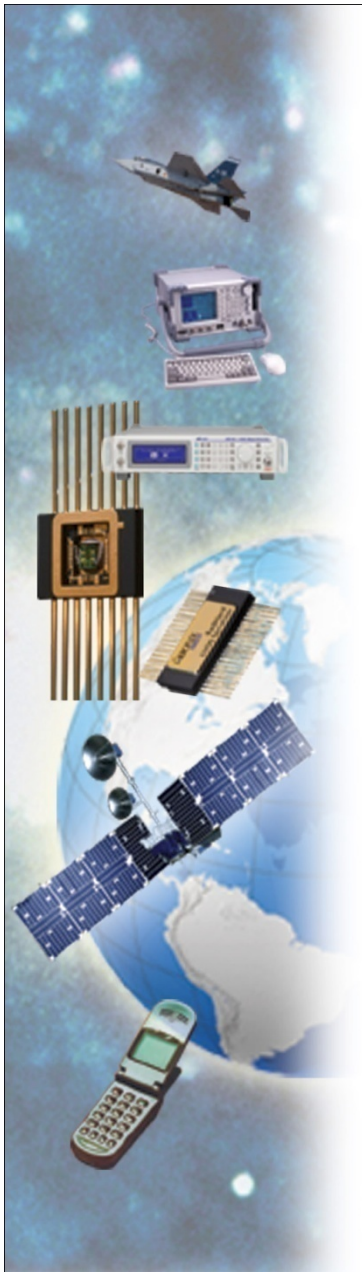


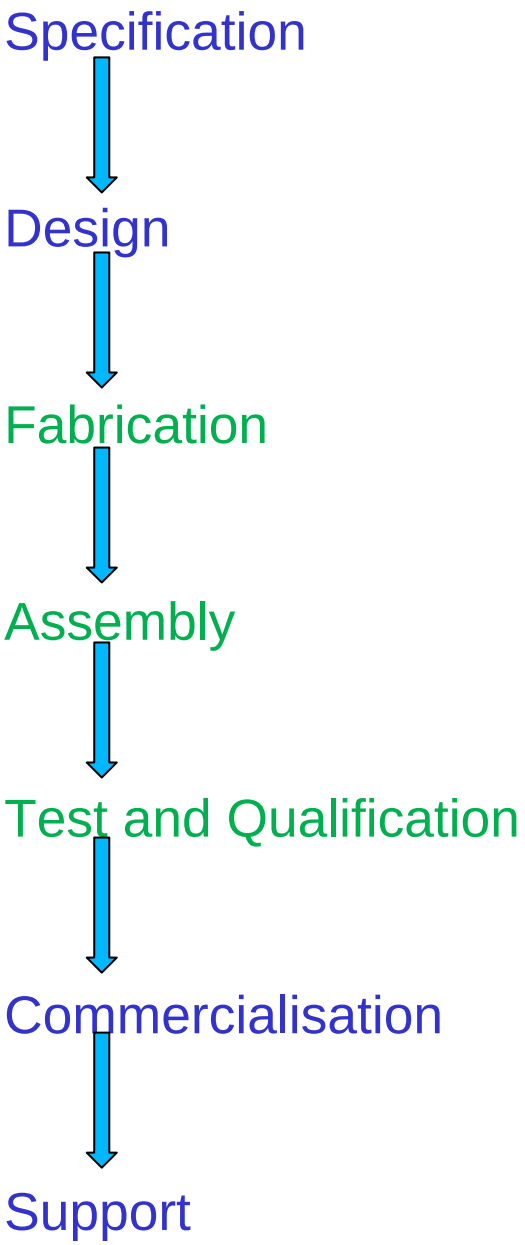
The Business Roadmap, a Design House Perspective

ESCCON, March 16, 2011

Aeroflex Gaisler

- Design house since 2001 focused on microprocessors (LEON)
- Rich IP portfolio with 80 IP cores (GRLIB)
- The IP is provided with test benches, tools, SW drivers and support
- Business model:
  - To license customers IP for inclusion in ASICs and FPGAs.
  - To provide customers with radiation tolerant FPGAs pre-programmed with our IP.
  - To act as an fab-less supplier of space components
  - To provide customers with tools, SW environment and support

Aeroflex Gaisler Fab-less Model



- Aeroflex Gaisler has the capabilty for Specification, Design, Commercialisation and Support

- Aeroflex Gaisler relies on partners for Fabrication, Assembly and Test/Qualification

- Specification to test/qualification must be done outside the US to not be affected by ITAR. If a component designed for space enter the US it can not re-exported outside the US without DoD approval

Specification and Design

- To date Aeroflex Gaisler has performed 100's of ASIC and FPGA designs
- The cost to design/fabricate/qualify of an "Space ASIC" is very high (MEURO)
- It is vital that extensive verification is done to validate the design before fabrication is started:
  - Simulation
  - Full functional validation on FPGA board
  - Analysis
- Understanding of customer requirements is necessary to generate a specification/design that allows multiple customers to purchase the components

Fabrication

- All our IP is technology independent and can be synthesized to any ASIC or FPGA technology. Thus Aeroflex Gaisler can use any foundry.
- Radiation hardened ASIC cell library is a must.
- Today there are (non-US) libraries available from:
  - Atmel (France)
  - IMEC (Belgium)
  - Ramon Chip (Israel)
  - ST Microelectronics (France, under preparation)
- Possible (non-US) foundries are:
  - Atmel (France)
  - ST Microelectronics (France)
  - Tower (Israel)
  - UMC (Taiwan)

Assembly and Test

- Aeroflex Gaisler reuse existing or develop and procure new packages
- Aeroflex Gaisler use external companies for assembly
- Aeroflex Gaisler use external companies for test and qualification
- SEU/SEL testing is performed in Belgium or Finland by Aeroflex Gaisler
- Aeroflex Gaisler use external companies for total dose test

Commercialization and Support

- To get return on investment the world market needs to be addressed (Europe, US and Asia)
- Aeroflex Gaisler have access to the Aeroflex Inc world wide sales organisation
- This world market needs also to be served with competent and timely support
- Today four engineers work full time with support at Aeroflex Gaisler
- Example, the LEON3/RTAX solution is now used by 33 different space projects (Europe 14, US 12, Asia 7). The LEON3 - UT699 is used in 23 projects.

Challenges

- To get a ESCC approved process (from design to qualified chip)
- Access to (non-US) radiation hard libraries for new processes (90, 65, 40 nm)
- Qualified high density packages. Today we are limited to 352 pin quad flat package. Next generation microprocessor will require 600+ pins and possible also flip-chip technology

GR712

- The GR712RC is a high-performance (125 MHz) dual core microprocessor for a wide range of space applications
- Developed in co-operation with Ramon Chips and Tower (Israel)
- Features:
  - High-performance dual-core LEON3FT (300 DMIPS, 250 MFLOPS)
  - Radiation-hard (300 krad)
  - On chip peripherals: SpaceWire, 1553, Can, I2C, SPI, Eth, TM/TC
  - Software compatibility with LEON family
  - Less than 2 W @ 125 MHz,
    two CPU's/FPU's under full load
  - Robust packaging: CQFP-240
  - Class-S (tested according
    Mil-std-883)