ICs packaging: Road Map and Trends for Space applications

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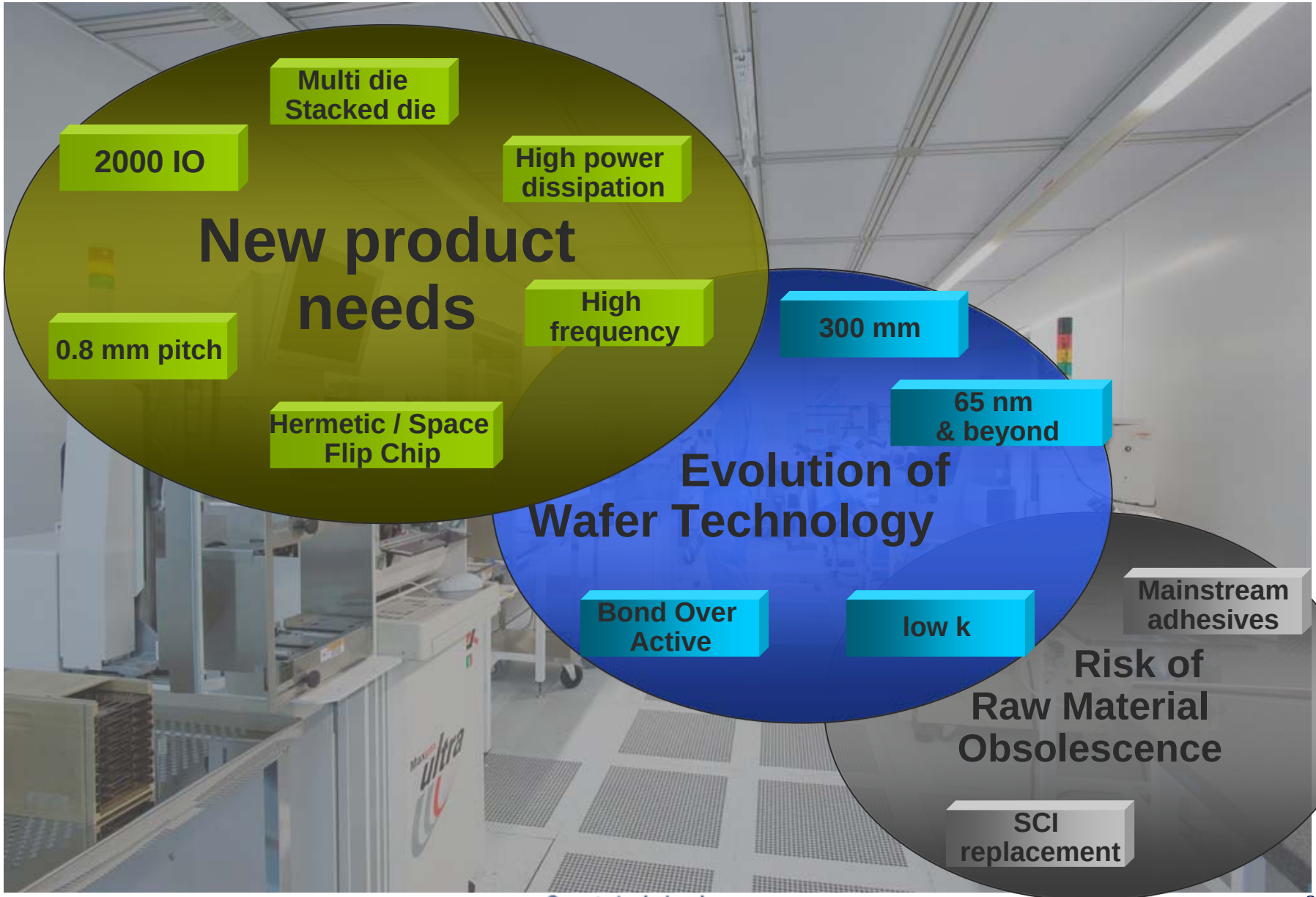
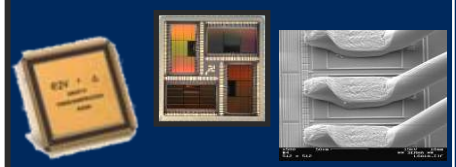
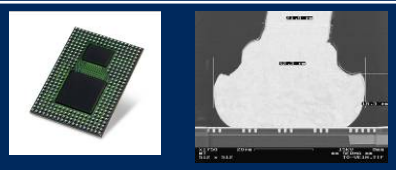
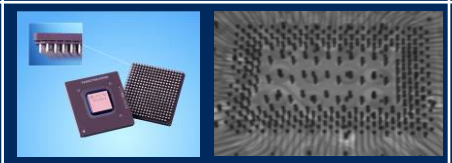
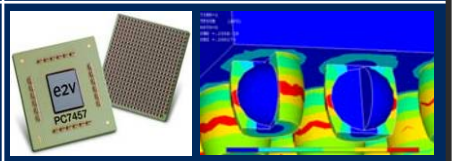
Needs



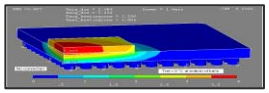
Packaging products & process
Where are we today?

Wire bonding		Flip Chip	
Hermetic	Non hermetic	Al2O3	HiTCE
Ceramic DIL, PGA, QFP, BGA.. ➔ 352 leads (800 wires) 32 µm aluminium wedge	EBGA ➔ 380 I/O Ball bonding SAC balls	High lead bumps ➔ 1 cm² die ➔ 25 x 25 mm LGA Solder column interposer	High lead bumps ➔ 1 cm² die ➔ 33 x 33 mm LGA High lead balls
			

600 m², class ISO5 (100)
500 m², class ISO6 (1000)
nb : preseal in class ISO 4 (10)

Road Map
Package Design & Assembly Process Capabilities

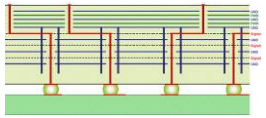
Thermal Interface Material



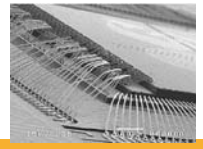
Mainstream adhesive materials (die bond)

Seam welding

High density routing

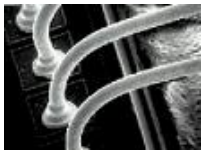


Die stacking

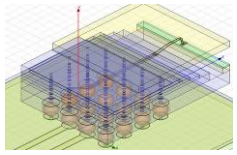


2011 | 2012 | 2013 | …

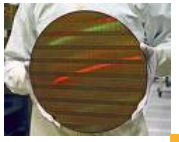
Fine pitch Au ball bonding 50um

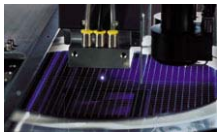


Increased signal / power integrity



300 mm saw & die bond





Laser saw

65 nm | 45 nm | Next technology nodes

Package Road Map

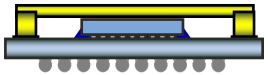
Kovar ring packages (Seam welding)

Stacked die

SIP, WLCSP,..

MCM flip chip

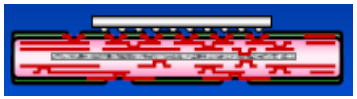
Hermetic flip-chip (Seam Welding)



2011 2012 2013 …

Heatspreader flip chip

Large Hi Rel quasi hermetic flip chip



Hi-rel organic

speed

3 Ghz 6 GHz …

1200 2000 …

I/O count

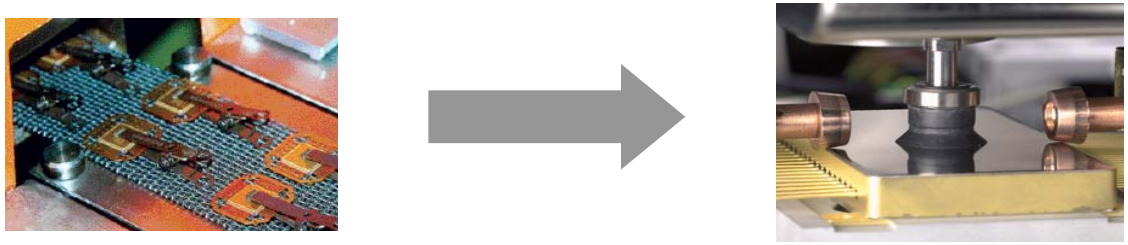
Technical Solutions
Focus on : seam welding

Current seal technology for hermetic packages (AuSn reflow) is performed at more than 300°C.

This temperature is now an important drawback, and seam welding becomes mandatory for :

- ➔ gold wire bonding (condition for very fine pitch)
- ➔ hermetic flip chip / underfill
- ➔ use of mainstream die attach adhesives (epoxies,..) instead of high temperature specific materials, such as silver glass
- ➔ and, more generally, use of organic materials in the cavity for specific applications (getters, stacked die, Thermal Interface..)
- ➔ compatibility with some wafer technologies which cannot withstand high temperature

For future products, this will lead to the addition of a kovar ring on package.

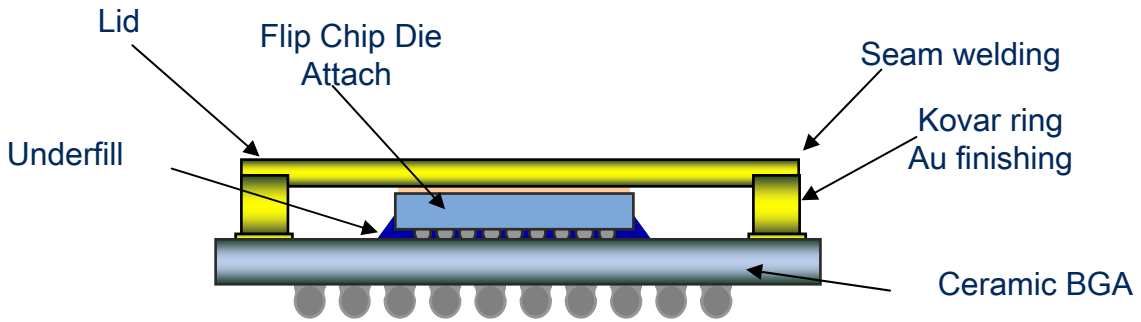


Technical Solutions
Focus on : Extended flip chip – Hermetic flip chip

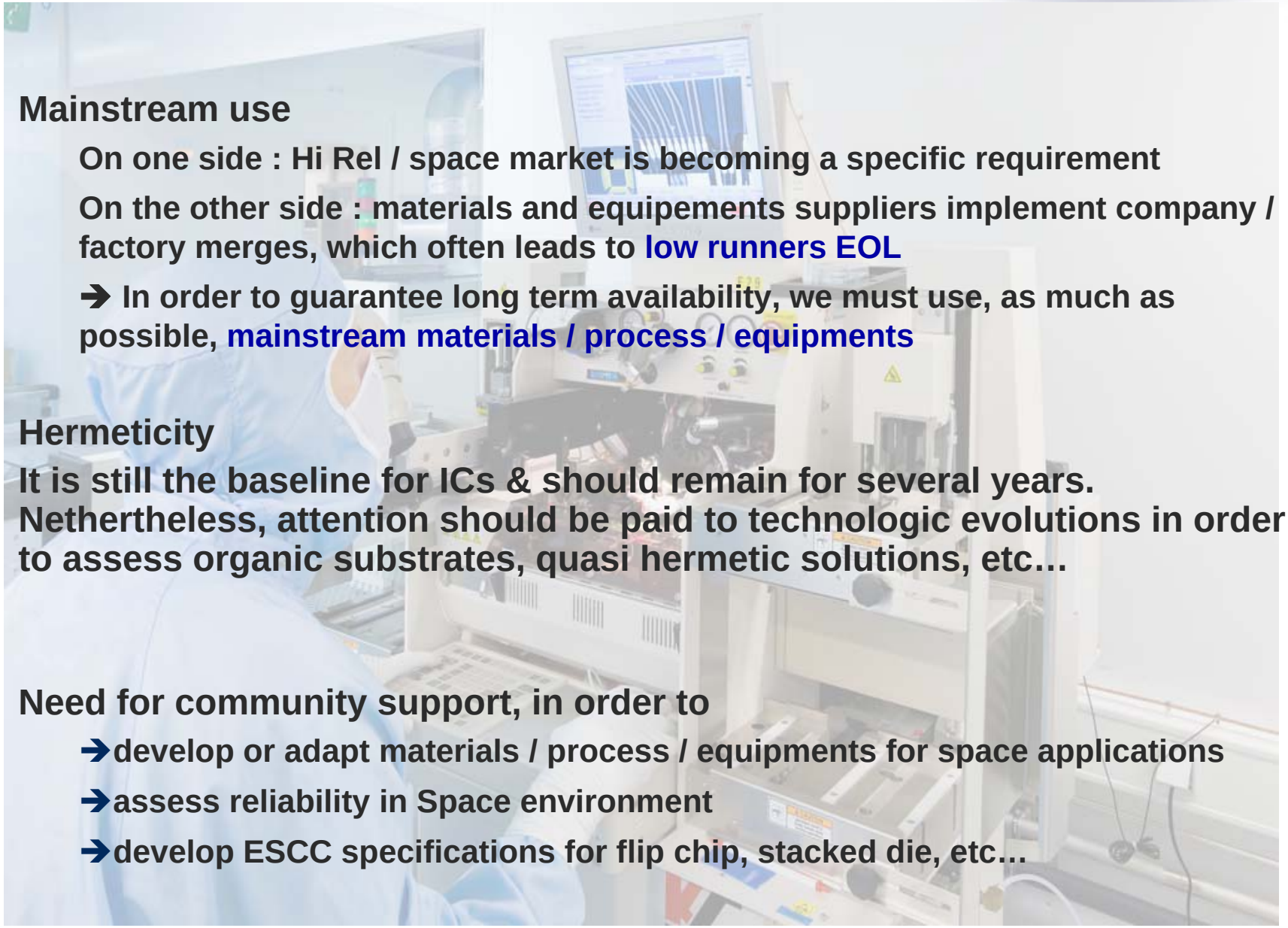
Flip chip assembly has been performed at e2v for more than 10 years for military grade, up to 1 cm², 1200 bumps.

In the next years, this capability shall extend to :

- Larger dice (up to 2 cm²), high pin count
- Smaller bump pitch
- Low k wafers
- Hermetic flip chip or Quasi hermetic (HiTCE ceramics)



Global trends - Discussion



Mainstream use

On one side : Hi Rel / space market is becoming a specific requirement

On the other side : materials and equipements suppliers implement company / factory merges, which often leads to **low runners EOL**

➔ In order to guarantee long term availability, we must use, as much as possible, **mainstream materials / process / equipments**

Hermeticity

It is still the baseline for ICs & should remain for several years. Nethertheless, attention should be paid to technologic evolutions in order to assess organic substrates, quasi hermetic solutions, etc…

Need for community support, in order to

➔develop or adapt materials / process / equipments for space applications

➔assess reliability in Space environment

➔develop ESCC specifications for flip chip, stacked die, etc…