European Space Components Conference.

Challenge for Advanced Payloads: Next generation ASICs, FPGAs and advanced Conversion components needs.

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Introduction

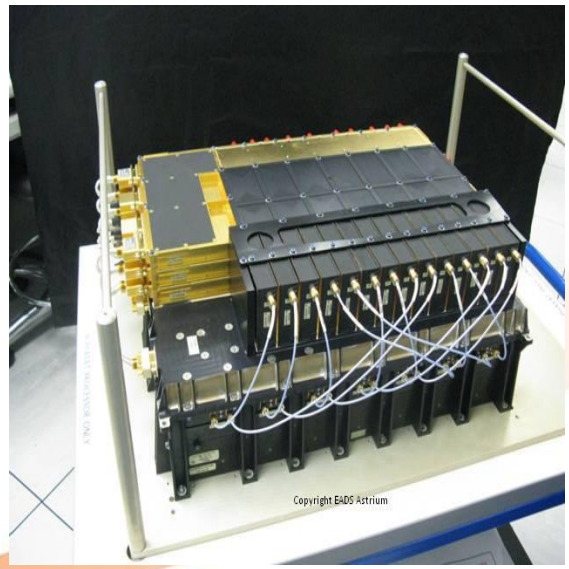
- Many extremely valuable and highly strategic European capabilities are dependant upon space borne systems to deliver telecommunications, navigation, civil and military observation and television services.
  - These systems have become ever more complex and this trend will continue into the future.
  - This trend requires ever more complexity in the electronics and this can only be achieved in flight payloads efficiently by deploying highly integrated ASICs and FPGAs, as well as high end standard components such as ADC, DAC.
  - Unfortunately, many of these technologies are subject to ITAR restrictions and the most advanced of these may be difficult to access by European satellite manufactures.

- The purpose of this presentation is to highlight the required performances of these components and to emphasise the technology gap to be achieved.
  - If this gap can be closed, or even surpassed, in a reasonable timescale, this would significantly advantage the European space industry.

State-of-the-art

- Both companies AST & TAS are involved in telecom domain building telecommunication systems based upon Integrated processors either in OBP or Transparent processors

- ASIC main features used in Processors
  - One ASIC implementing main required functions for transparent processors such as Demux, Mux ….
  - Implementation
    - ATMEL ATC18RHA 0.18 µm
    - 132 mm^2 core area, Packages up to 625 LGA
    - Complex Logic embedding RAMs, meaning up to 5 M equivalent gates with system frequency over 300 Mhz
    - Power: up to 8W depending upon configuration



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ASIC

- Extremely large and complex ASIC development
  - Stretching the technology in all parameters: area, speed and I/O.
  - Recent ASICs at limits of qualified European 180nm technology
- New applications will require Deep Sub Micron ASICs as an enabling technology in the coming years.
  - Particularly in Telecom to improve bandwidth and channels to be handled, but also in High Performance Data Handling, both demanding
    - Higher integration, lower power/gate, higher interconnection.
- Main requirements are:
  - Up to 20 million equivalent gates integration capabilities
  - Implementation of embedded HSSL (High Speed Serial Links) up to 10 gbps
  - Implementing macros such as RAMs and PLLs as a minimum
  - System frequency capability in the range of 3 to 400 Mhz

ASIC

- ASIC technology offerings from US companies will include 90nm from 2012 - but access will be restricted.
- In 2008 ESA started a project to develop European ASIC technology
  - STMicroelectronics - KIPSAT
    - Supported by Astrium and Thales Alenia Space.
    - Radiation hardened 65nm ASIC libraries
    - Multi Gbps HSSL are a key requirement of any DSM offering. Multiple HSSL inside ASICs and stand alone chips
    - High PIN count packaging with high power dissipation capabilities will be a key enabler.
- Secondary users of DSM 65nm technology
  - A move to DSM ASIC is not compulsory for many applications.
    - However, there may be considerable performance, power, integration and test benefits.
    - Price is critical for this market segment.

FPGA

- FPGAs are preferred over ASICs in some cases
  - Smaller missions that do not have highly parallel architectures.
  - Missions with low or moderate processing rates.
  - Functions where the power and gate density overhead of the FPGA technology is manageable.
  - Functions that are control and configuration orientated.
  - Functions that might be subject to late changes.
  - Missions that cannot afford the ASIC costs or timescales.
- Many recent equipments have used anti fuse based FPGA.
  - MicroSemi RTAX, ~10K cells, ITAR restricted.
- Within Europe, comparative FPGAs are expected to be available soon.
  - Atmel ATF280K, ~14K cells in 2011. ATF450K, ~23K cells in 2012
- Offerings from US companies will include high density FPGAs (>80K cells) from 2011/13.
  - Xilinx Virtex5 SIRF, MicroSemi ProASIC4

FPGA

- In 2009, a consortium lead by Atmel proposed a new high density FPGA development to the EC.
  - Atmel RAHDHIFFS FP7 proposal based on Abound Logic architecture targeting 65nm technology.
  - Supported by Astrium and Thales Alenia Space.
  - Unfortunately, this development has not started.
  - European satellite manufacturers continue to encourage the development of ITAR free, very large cell count FPGAs.
- Emerging US FPGA technologies might be used in future if their suitability is established.

Conversion

- *ADCs/DACs are key components of digital satellite payloads.*
- *Without ADCs/DACs, payload processors for telecommunication, navigation, Earth observation and space science satellites would simply not exist.*
- *ADCs and DACs have been flown on all missions where digitalization equipments are used .*

ADC/DAC specification requirements to fulfil future customer needs

- *Single power supply rail devices*
- *Low power consumption, i.e. < 2W*
- *ENOB performance > 11 bits*
- *The ability to synchronise multiple devices*
- *The ability to null part-to-part spreads*
- *No in-band, non-carrier related spurs*
- *Wideband ADCs*
- *Return-to-zero DACs*

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Conversion

- *European ADC/DACs must offer technical and commercial advantage to European satellite manufacturers when competing for global satellite contracts.*

- *European ADC/DACs which offer comparable performance to existing parts and enter the market late will never succeed as there is no added value for European payloads and the cost to re-design is too expensive.*

Summary

- There is a clear need for DSM ASIC technology with HSSL to enable:
  - Next Generation Telecom Payload and High Performance Data Processing Products
    - Attractive pricing would further broaden the application scope and subsequent part quantities.
- FPGA
  - For moderate cell count devices (>10K) US parts are available now.
    - Comparative European FPGA parts are expected in 2011/12.
  - For very large cell count devices (>80K) US providers have indicated availability in 2011/13.
    - European satellite manufacturers continue to support the development of ITAR free, very large cell count FPGAs.
- ADC/DAC
  - European parts must offer a technical and commercial advantage.
- Questions?

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