CENTRE NATIONAL D'ÉTUDES SPATIALES

ESCCON 2011
European Space Components Conference

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Challenge for advanced payloads :
Next generation ASICs, FPGAs
and
Advanced Conversion components Development

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Outline

- **Introduction**
- DSM Technologies
- DSM Program
- Data Converters
- ASIC technology
- FPGA
- Conclusion and way forward

Introduction

- Space needs DSM technology
  - The availability and performance of European components is a key issue for European Industry to deliver the next generation of digital payloads

- The Deep Sub Micron (DSM) initiative, coordinated within the frame of the CTB, identified critical technologies for next generation telecommunication satellites :
  - Broadband ADC and DAC
  - HSSL
  - digital ASICs
  - FPGA.
- ESA TRP, CNES Strategic components and European Community FP7 budgets have been used to develop and evaluate, according to ESCC standards, these strategic components and technologies, with requirements :
  - Rad-hard (100Krad), SEL immune,
  - Reliable (20 years lifetime)
  - Operating in military temperature range (-55°C/+125°C)

Those programs will improve satellites manufacturers competitiveness by enabling an independent European components procurement

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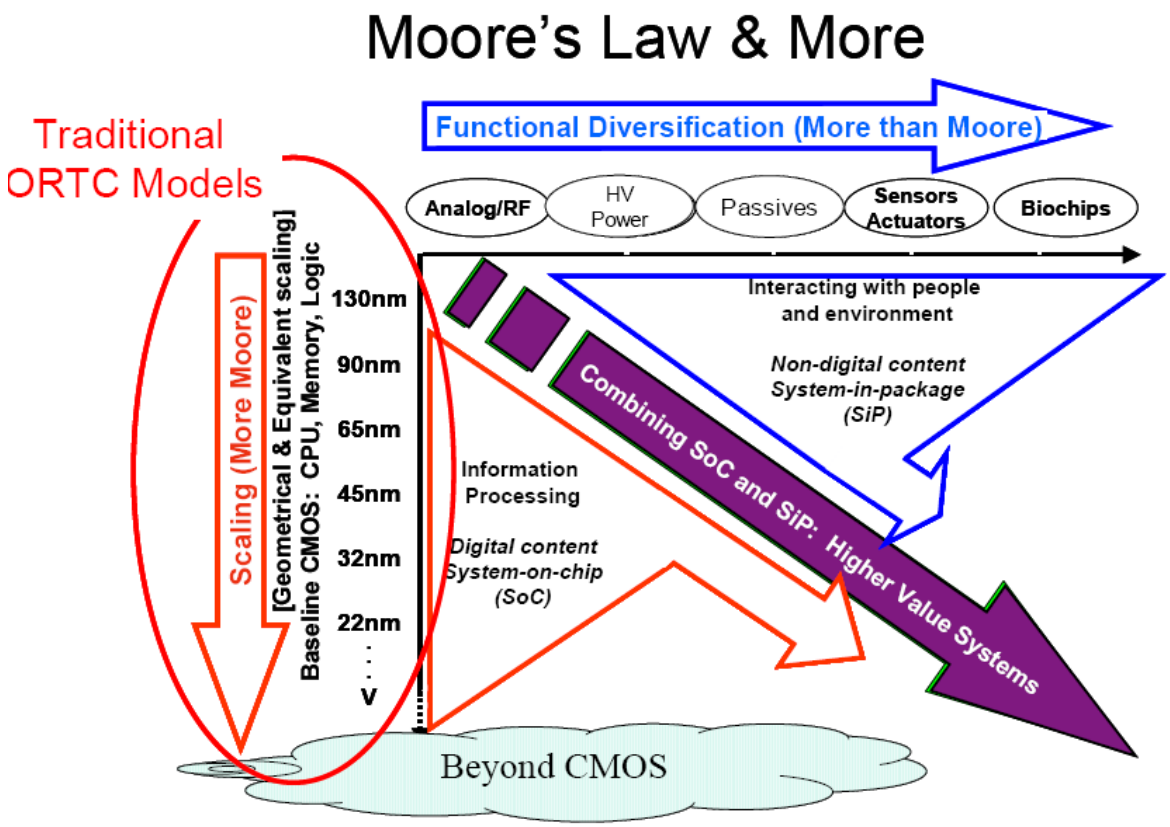
Moore law

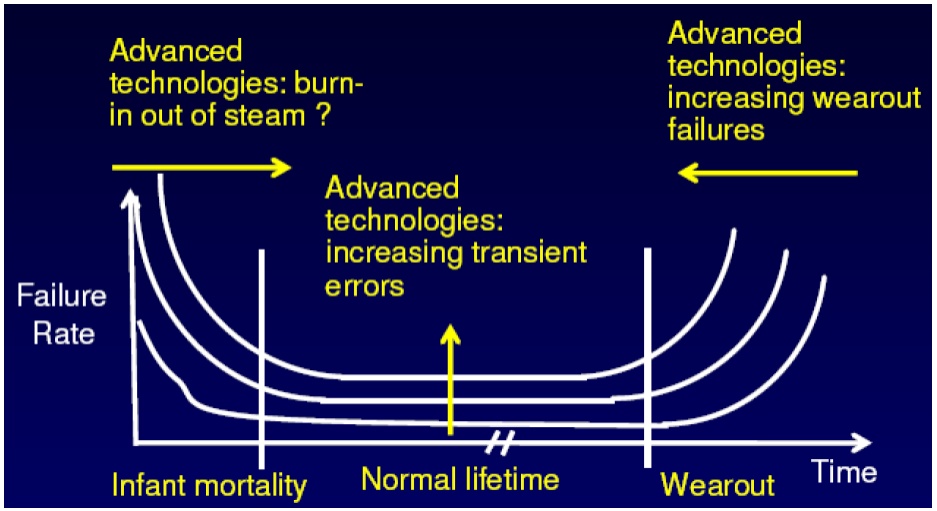
- According to Moore's Law, technology are still speedily evolving
- The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip
- DSM technology = 90nm and beyond
- Payload Processor ASIC requirements (10-30 Millions gates, 6Gbit/s Serial I/Os, Low dissipation …) and Next Generation general purpose ICs (NG-Microprocessor, NG-FPGA) are only achievable with Deep Sub Micron



Source: 2009 ITRS Executive summary

Reliability

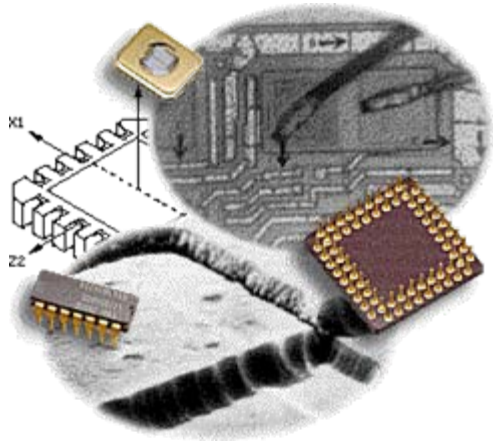
- Process development of DSM technologies is becoming more and more challenging
- The rising reliability concerns are closely related to :
  - the reduction of critical dimensions,
  - the increase in electrical field strength and in interconnections current densities
  - and to the use of new materials/processes.
- New preponderant Failure mechanisms :
  - Hot Carrier Injection (HCI)
  - Negative Bias Temperature Instability (NBTI)
  - …



Source : Subhasish Mitra (Stanford University),2005

Mandatory

- To insure Reliability for space DSM technology :
  - DSM lifetime has to be early taken into account
  - DSM reliability parameters have to be correctly chosen and modeled for lifetime simulation purpose
  - Manufacturer involvement is a critical issue : close relationship is needed



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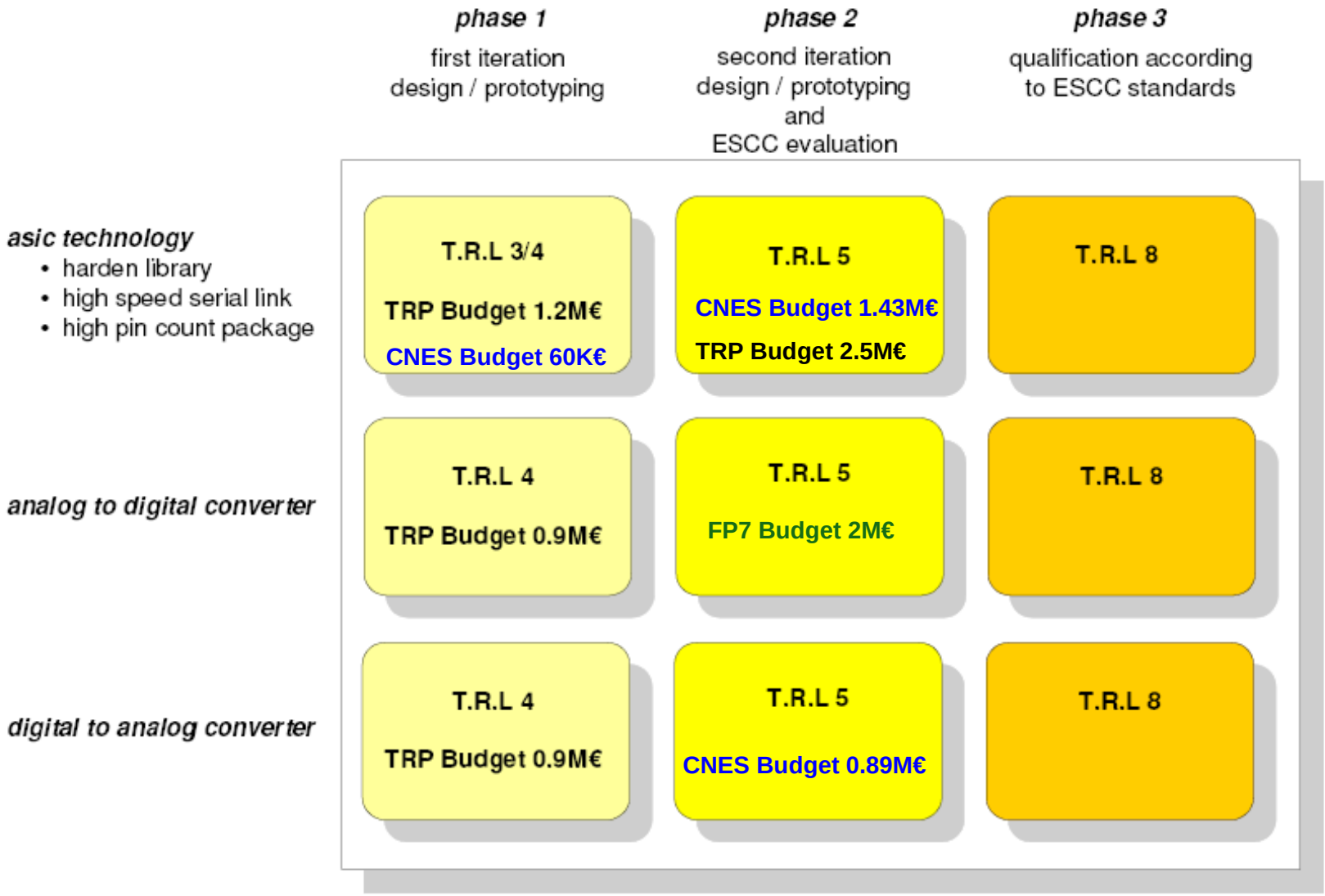
Combining ESA and CNES efforts and budgets



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E2V EV10AS180
Low power 10-bit 1.5 Gsps ADC

ESA TRP - 900K€ + COMETS - European Community's 7th FP under grant agreement n° 242521 - 2M€

- **Objective : Development and ESCC evaluation of the E2V EV10AS180 1.7W L-Band 10-bit 1.5 Gsps ADC**
- **Consortium : E2V(F), INFINEON (G) , TAS (F), ASTRIUM (UK), CNES (F), CNRS IEMN, Xlim (F)**
- **Schedule :** T0 = Feb 2008 – End = Q3/12

- **Main Features**

  1.5 Gsps Guaranteed Conversion Rate Selectable 1:1/2/4 DEMUX
  LBand 1.7 W Power Dissipation
  CI-CGA255 Package B7HF200 SiGeC technology from Infineon (G)
  100Krad Radiation tolerant
  Low latency < 4 cycles times

- **Key Performances**
  - **2.2 GHz Full Power Input Bandwidth (-3 dB)**
  - **Single Tone Performance @ Fs=1.5Gsps :**
    - SFDR = -60 dBFS, ENOB = 8.5 Bit; SNR = 55 dBFS at Fin = 750 MHz @-12 dBFS
    - SFDR = -60 dBFS, ENOB = 8.4 Bit; SNR = 53 dBFS at Fin = 1800 MHz @-12 dBFS
  - **Broadband Performance:**
    - NPR = 44 dB at -13 dBFS Optimum Loading Factor in 1st Nyquist
    - NPR = 43 dB at -13 dBFS Optimum Loading Factor in L-band
- **Status :**
  - **Design Completed with First prototypes showing very good dynamic performances but still some improvements needed design respin**
  - **Design respin completed**
  - **Final Silicon under electrical characterization by E2V**
  - **ESCC evaluation will start in Q2/2011**

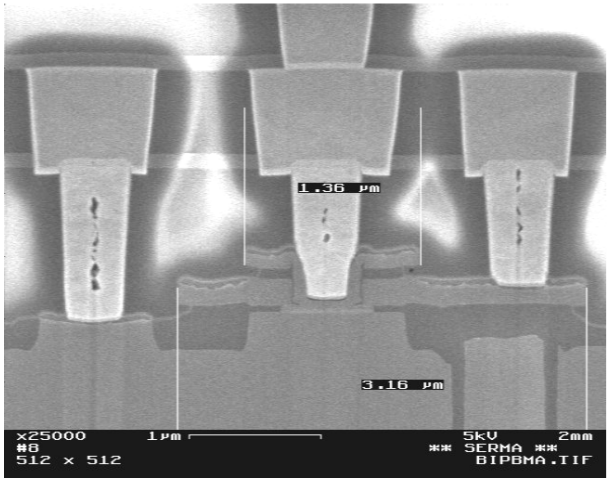
EV10AS180 ADC in EPPL in Q3/12

E2V Low power 12-bit 1.5 Gsps ADC

COMETS - European Community's 7th Framework Programme under grant agreement n° 242521 - 2M€

- **Objective : Design and Characterization of the 12-bit ADC by E2V and end-users**
- **Consortium : E2V(F), INFINEON (G) , TAS (F), ASTRIUM (UK), CNES (F), CNRS IEMN, Xlim (F)**
- **Schedule :** T0 = May 2010 – Duration : 36 months

- **Key Features :**
  - **1.5Gsps conversion rate (no on-chip interleaving)**
  - **L band application**
  - **Selectable ratio DMUX output (1:1/1:2)**
  - **Low latency**
  - **User friendly feature**
  - **LVDS compatible**
  - **B7HF200 SiGeC technology from Infineon (G)**
- **Status :**
  - **Ongoing characterization work for improved B7HF200 technology device modeling by IEMN and XLIM**
  - **Test chip under validation with encouraging preliminary results**
    Single Tone Performance @ Fs=1.5Gsps :
    - **SFDR < -70 dBFS, ENOB = 9.4 Bit; at Fin = 750 MHz @-12 dBFS**
    - **SFDR < -70 dBFS, ENOB = 9.3 Bit; at Fin = 1800 MHz @-12 dBFS**



SiGeC B7HF200 technology cross-section

12-bit ADC validated prototypes in Q2/13

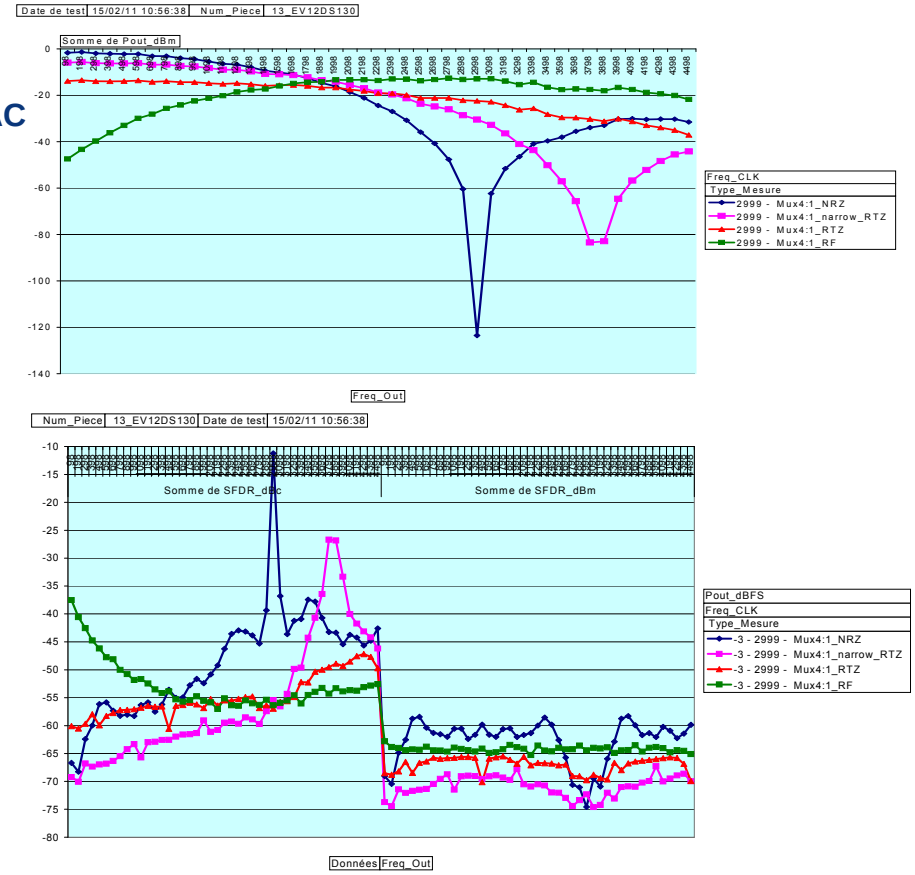
E2V EV12DS130
Low Power 12-bit 3 Gsps DAC with 4/2:1 MUX

CNES Strategic Component Plan – 890K€

- **Objective : Development and ESCC eval. of the 12-bit 3 Gsps DAC**
- **Contractor : E2V(F)**
- **Schedule :** T0 = Nov 2009 – End = March Q3/12

- **Main Features :**
  - **12-bit resolution** **3 Gsps Conversion rate**
  - **4:1 or 2:1 built in MUX (selectable)** **1.3 Watt Power Dissipation**
  - **NRZ, Narrow RTZ, 50% RTZ, RF modes** **100Krad**
  - **Ci-CGA255 Package, B7HF200 SiGeC technology from Infineon (G)**

- **Key Performances (charact. results):**
  - **Time domain: Full swing Rise Time=60ps**
  - **Broadband : NPR at -14dB loading factor, and Fs=3Gsps**
    - 1st Nyquist (NRZ or NRTZ): NPR= 47.4 dB ➔ 9.4 Bit equivalent
    - 2nd Nyquist (RTZ or RF): NPR= 40 dB ➔ 8.2 Bit equivalent
    - 3rd Nyquist (RF): NPR= 38.5dB➔ 7.9 Bit Equivalent
  - **Single tone (see plots of the four modes):**
    - Pout for Fout from 100MHz to 4.5GHz at 3Gsps
    - SFDR (dBc) and HSL(dBm) four Fout from 100MHz to 4.5GHz Aout=-3dBFS, 3Gsps (Bottom plots)
- **Status :**
  - **Design completed in March 2010**
  - **Silicon under electrical characterization to assess that is the final one**
  - **ESCC evaluation will start in April 2011**



EV12DS130 DAC in EPPL in Q3/12

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65nm CMOS technology

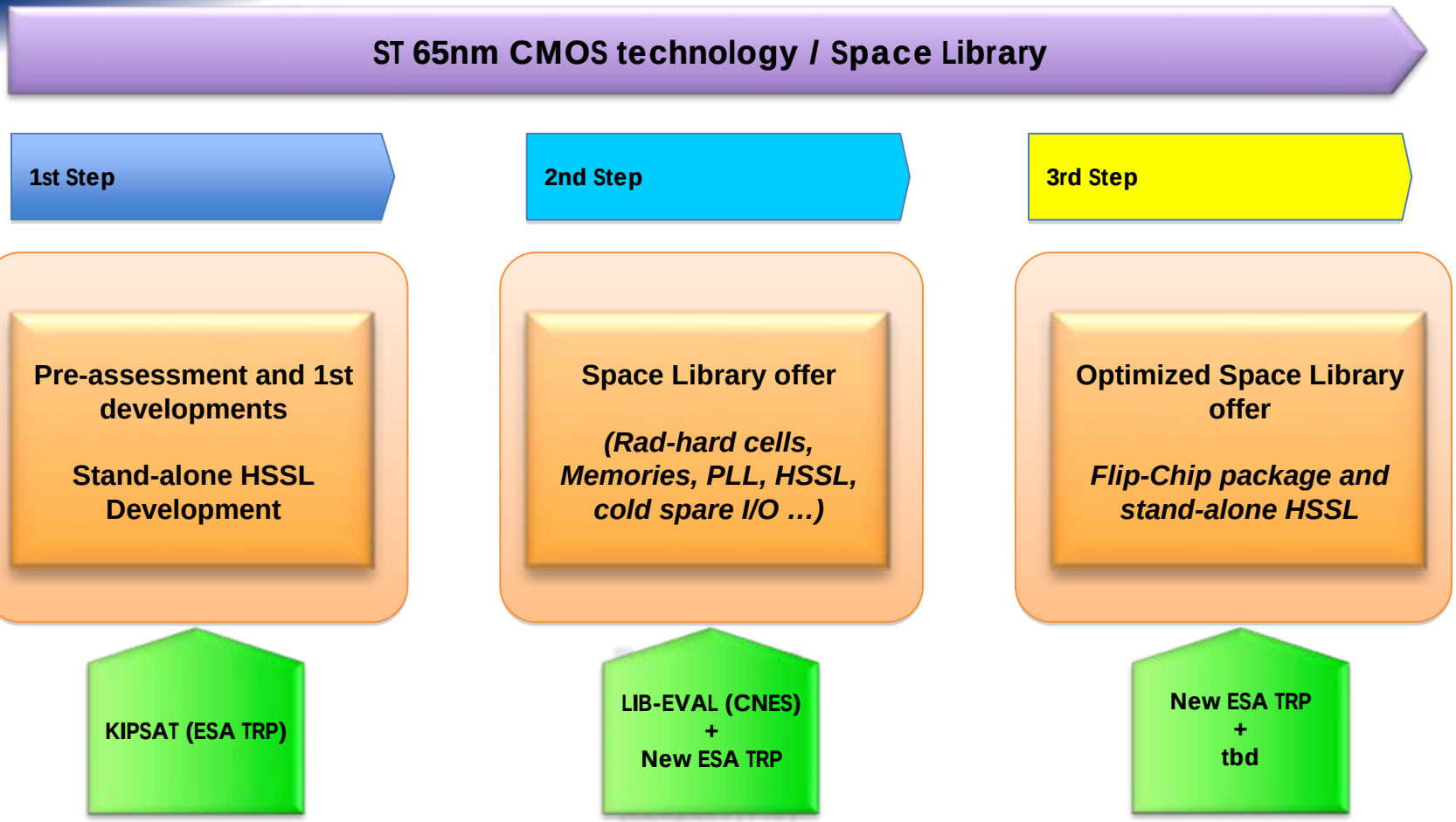
- 65nm-LP CMOS from ST France : European technology, ITAR free
- Payload Processor ASIC requirements (10-30 Millions gates, 6Gbit/s Serial I/Os, Low dissipation …) are only achievable with Deep Sub Micron
- Next Generation general purpose ICs also need DSM: NG-Microprocessor, NG-FPGA

- 65nm CMOS commercially qualified in 2007
- 65nm CMOS Core Process :
  - Dual / Triple Gate Oxides
  - Dual / Triple Threshold Voltages for MOS Transistors
  - 7-9 Full Copper Dual Damascene Interconnect Levels
  - 0.20µm metallization pitch
  - Low K (dielectric)
- Characteristics :
  - 750 kgates/mm2
  - 2GHz stdcells
  - 5.7nW/(MHz x gates)
  - 1.25-7.5GBit/s High Speed Serial Link (HSSL) modules
  - Flip-Chip packaging needed

❖ST proposed its CMOS 65nm-LP process for space

❖Reliability maximization and Radiation hardening at process and design stages

ASIC technology



ASIC technology

Activity to be funded or performed/started

Q1/08 | Q1/11 | Q3/11 | Q3/12 | Q2/13

Work already done
(Mainly under KIPSAT ESA contract)

- Space library design
- Reliability & Radiation data analysis
- Feasibility of Flip-Chip package
- Definition of the standard cells library
- HSSL Quatuor design and IP

ST-ASIC vendor partnership

65nm Space library design
<---ESA Dvlpt---------><--CNES complement--->

CAD tool, Design kit,
CAD flow eval. by End Users
Flip-Chip Assembly Dvlpt
ESA TRP (1.5M€)

1st Space Lib Beta use

Test Chips

Flip-Chip Assembly ESCC Eval.

Package for ASIC in EPPL

ESCC Eval. 65nm Space library + die (incl.HSSL)
Electrical charac, Reliability, Rad tests & Construction analysis

Total cost : 2.86M€
- ST (1.43M€)
- CNES (1.43M€)

65nm Space Library in EPPL

HSSL Quatuor design

Total cost : 3.1M€
- ST (1.84M€)
- KIPSAT TRP ESA (1.2M€)
- CNES (60K€)

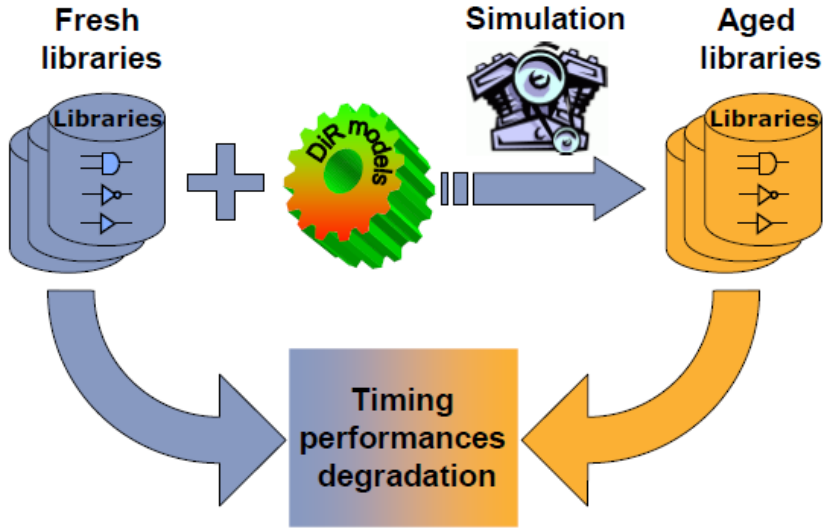
1st HSSL

HSSL redesign + ESCC Evaluation of stand-alone HSSL *ESA TRP (1M€)*

Stand-alone HSSL

Reliability maximization

- Systematic application of ST Design in Reliability (DiR) methodology :
  - focusing HCI and NBTI with dedicated tools for ageing simulations
  - Eventual specific layout rules for reliability enhancement
- Application of ST Design for Manufacturing (DfM) :
  - Study of tighter controls at process level
  - Analysis of reliability figures from Std qualification



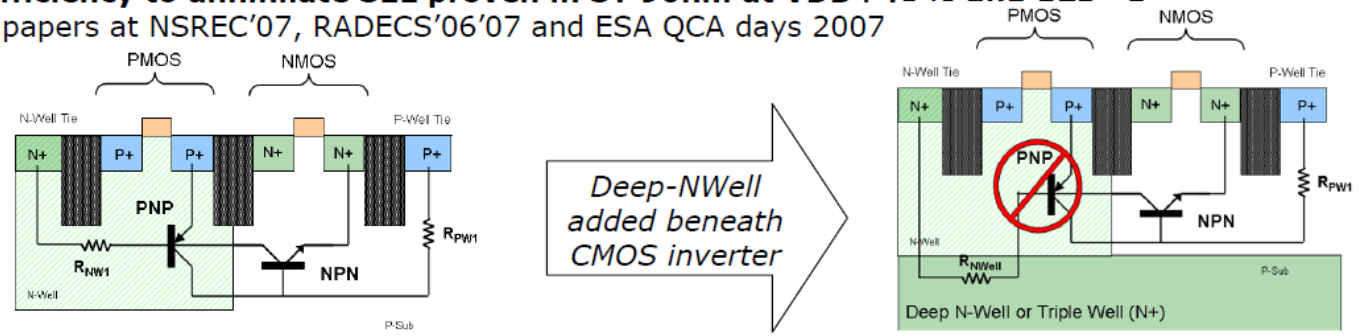
- ST has built an industrial flow which allows a full coverage of reliability effects all along the product value chain
- Reliability tests will be also performed during ESCC evaluation

Radiation hardening

- Rad-hard capabilities measured under ESA contracts (ST 130nm, 90nm, 65nm and 45nm)
  - No current increase seen up to 300krad(Si) TID
- SEL-free with Deep-N well process option

DNW efficiency to annihilate SEL proven in ST 90nm at VDD+40% and 125 °C

ST papers at NSREC'07, RADECS'06'07 and ESA QCA days 2007



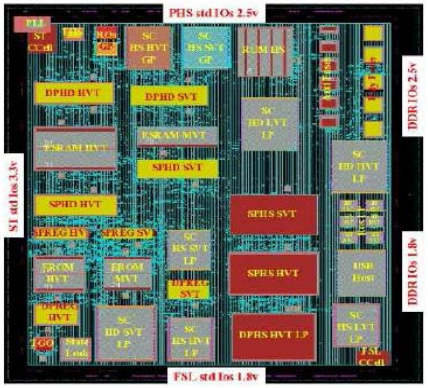
- SEE/SETs fault injection techniques for Digital and Analog blocks sensitivity analysis
- Usage of existing Robust cells, TMR
- Hardening of clock-trees against SETs
- Shadowing of configuration registers + scrubbing
- Development of Rad-Hard new cells
- Layout techniques

ESCC Evaluation

- **Evaluation Test Programme :**
  - Representative Test chips manufacturing of the Space library
  - Electrical characterization of representative the Test chips
  - Reliability tests addressing NBTI and HCI to confirm life time of 20 years @ Tj=110°C
  - Radiation tests : TID, SEE under heavy ions and protons
  - Construction analysis

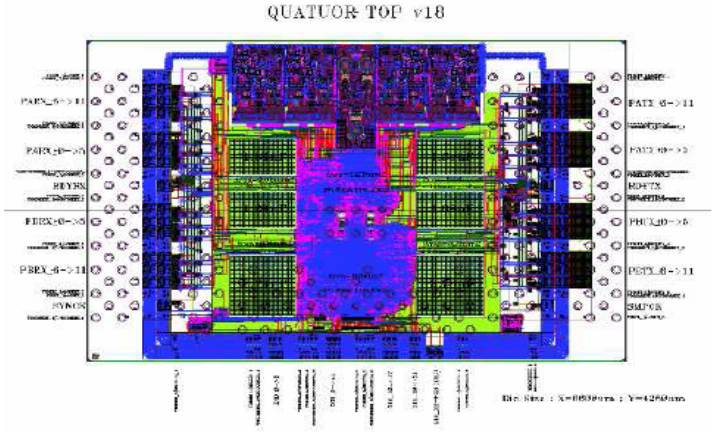
TC1 (rad hard library):

TC4 (commercial library subset):



TC2 (PLL + IOs cold spare)

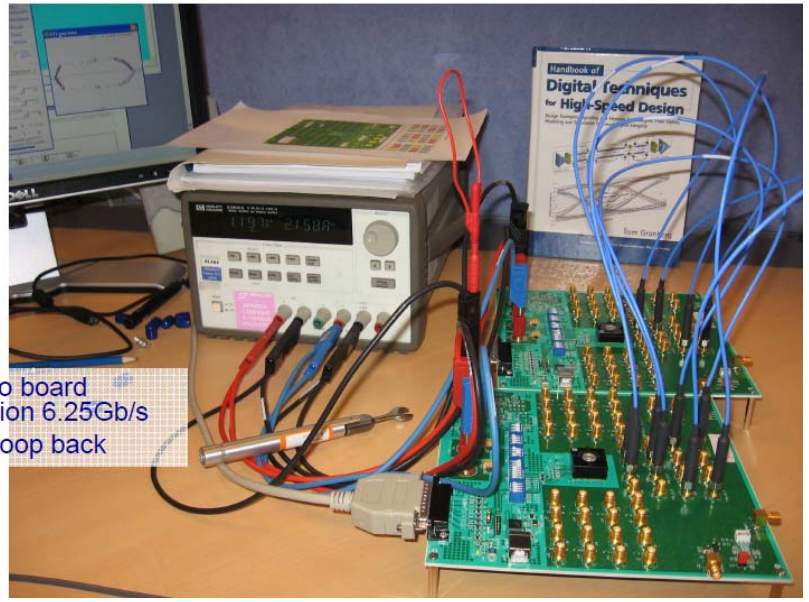
TC3 (HSSL) **Quatuor / 4 x 6.25 Gbps**



65nm space library in EPPL in Q3/12

Quatuor HSSL

- **Functional specification :**
  - **1 clock slice + 4 data slices**
  - **24 // LVDS port in + 24 // LVDS port out at 375Mhz DDR max**
  - **24 digital IOs to support I²C, SPI, UART, JTAG, TIC, MDIO protocols**
  - **Max Serdes rates are :**
    - 25Gbps Tx simplex
    - 25Gbps Rx simplex
    - 50Gbps full duplex with 4 active lanes (25Gbps Tx / 25 Rx). Full duplex mode limited to 2 active lanes due to power dissipation. 12.5Gbps Tx / 12.5Gbps Rx
- **Statuts :**
  - **Design completed under KIPSAT ESA TRP**
  - **1st silicon available in Q3/10**
  - **Electrical characterization on going :**
    - Functionality validated, some minor bugs identified
  - **Heavy ions tests report and Preliminary reliability test on going**
- **HSSL + IP completion is planned under new ESA TRP**



Board to board
Communication 6.25Gb/s
Remote loop back

4 x 6.25Gbps HSSL prototypes available

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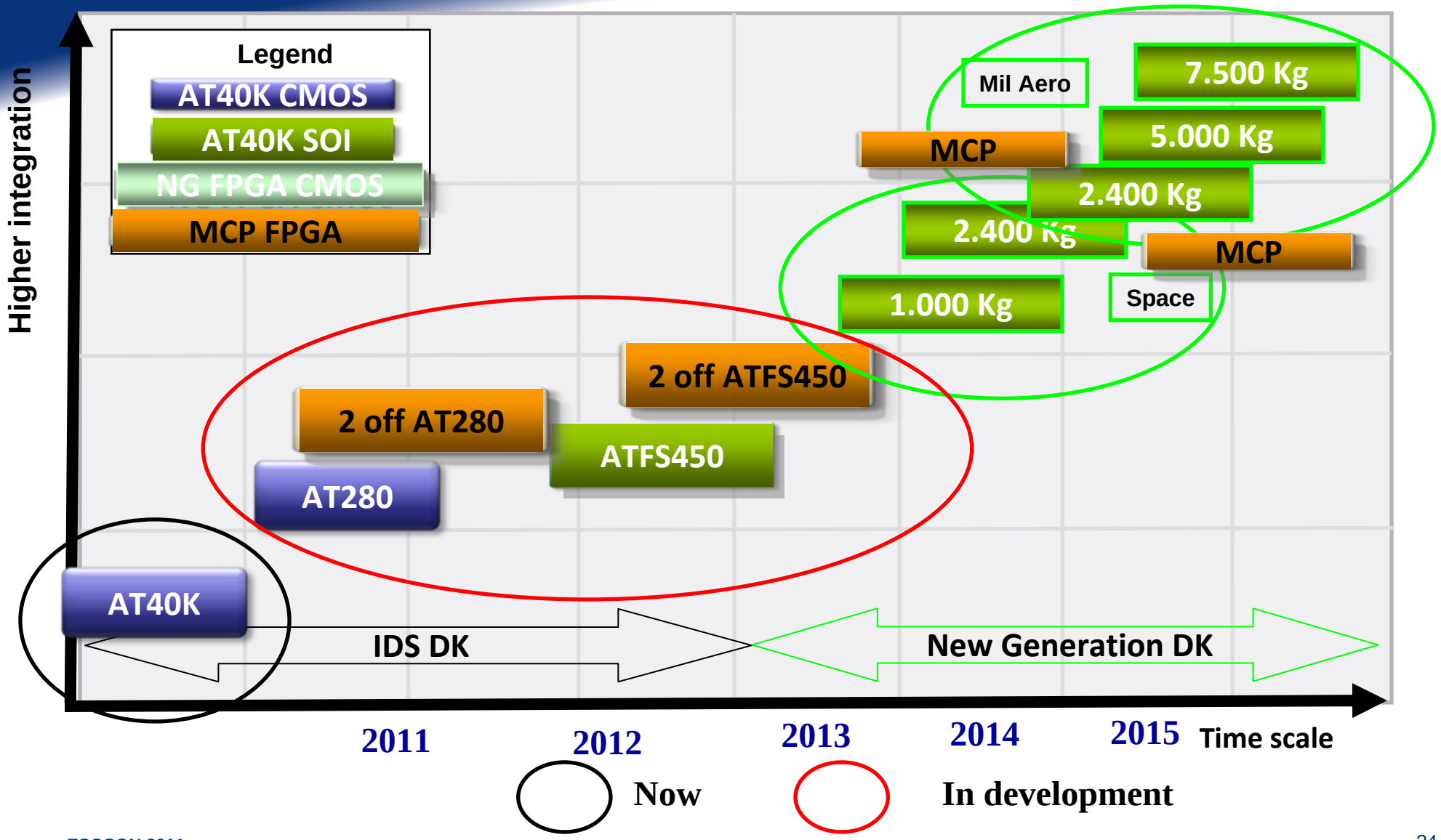
FPGA

- **Current status :**
  - **ACTEL is the leader but without reconfiguration capabilities with up to 500Kg/100MHz, process 150nm**
  - **ATMEL is coming with ATF280F and ATF450, SRAM based, for a complexity of 280Kg/50MHz and 450Kg/75MHz.**

- **The needs for the Next Generation European reprogrammable FPGA are :**
  - **a DSM technology,**
    - such as the specific 65 nm CMOS process technology currently developed at ST
    - current US FPGA space program is the " SIRF " from Xilinx (SEU Immune Reconfigurable FPGA) based on their Virtex-5 family.
  - **a new field reprogrammable logic architecture with the associated tools,**
    - such as already existing (ex-)Abound Logic FPGA architecture developed in Europe and whose main features are :
    - a highly hierarchical architecture allowing for very deterministic propagation times, gates utilization ratio as high as 90%, low operating power and half the bit stream size of any of their competitors,
    - a good trade off between programmable logic, on one side, and memory and mathematical function blocks, on the other side.

Xilinx Virtex5 SIRF	ATF280F	ATFS450	NG-FPGA
450 MHz	50 MHz	75 MHz	tbd
844 IOs	308 IOs	214 IOs	tbd
1.3 Mgates	280 Mgates	450 Mgates	1-2.4 Mgates
65nm (TSMC)	180nm (LFoundry)	150nm SOI (OKI)	90nm/65nm (UMC/ST)
Mature HW architecture	Old, limiting HW	Old, limiting HW	Advanced new HW IP
Mature SW	Old, limiting SW	Old, limiting SW	Advanced new SW IP


Higher integration
Legend
AT40K CMOS
AT40K SOI
NG FPGA CMOS
MCP FPGA
Mil Aero
7.500 Kg
5.000 Kg
MCP
2.400 Kg
2.400 Kg
MCP
Space
1.000 Kg
2 off ATFS450
2 off AT280
ATFS450
AT280
AT40K
IDS DK
New Generation DK
2011
2012
2013
2014
2015
Time scale
Now
In development

ATMEL/OKI/HIREC ATFS450E
450Kg FPGA on OSC 0.15µm SOI technology

CNES Strategic Component Plan – 800K€

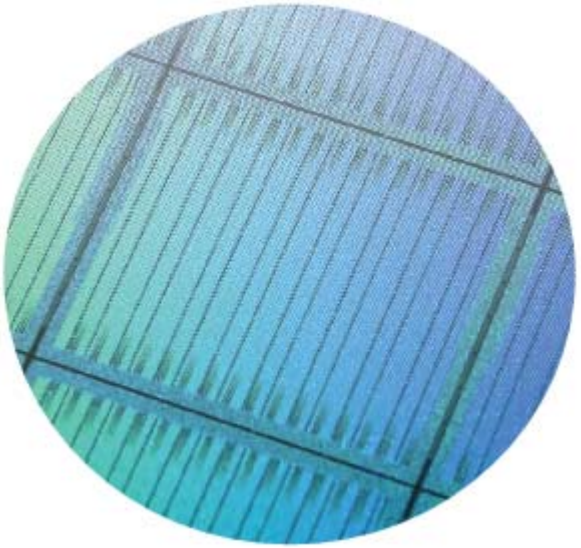
- **Objective : 450Kg FPGA Development (Joint ATMEL and HIREC development with CNES and JAXA support)**
- **Contractor : ATMEL (F)**
- **Schedule :** T0 = Q4/08 – End = Q3/12
- **Key Features :**
  - 450K equivalent ASIC gates☐ 152x152 core cells
  - 75 MHz internal performance ☐
  - 3.3V and 1.8V programmable IO and 1.5V array bias voltages
  - 8 Global SEU/SET immune Clocks
  - OSC 150nm SOI process☐
  - Package MQFPF256 (118 IOs), MQFPF352 (214 IOs)
  - Latch-up free SEU/SET free at LET of 64 MeV/mg/cm² ☐ 100 krad
- **Status :**
  - Design completed in Q4/10
  - Silicon under assembly for electrical characterization
  - Prototypes availability : Q3/11
  - ATMEL industrialization and internal Qual : Q3/12
  - ESCC evaluation report (Activity to be funded): Q1/13

ATFS450E FPGA in EPPL in 2013

1Mg – 2.4Mg Rad-Hard reconfigurable FPGA based on a new architecture

ESA TRP- High density European rad-hard SRAM-based FPGA :
Abound-Logic-based first validated prototypes – 2M€
+ European Community's 7th Framework Programme – RADHIFFS – 2M€
+ Necessary complementary fundings are needed

- **Objective : Develop a reconfigurable rad-hard by design FPGA based on Abound Logic architecture**
- **FP7 Consortium :** ATMEL (F), Abound Logic (F), ASTRIUM (G, F et UK), CNES (F), EADS IW (F), Politecnico torino (I), Space Research Center PAS (Poland), Surrey University (UK), TAS (F), Tubitak Uzay (T), University of Padova (I), AICIA Sevilla (Spain)
- **Schedule :** T0 = not started, duration : 3 years
- **Status :**
  - Abound Logic FPGA IP has been sold to Meta Systems subsidiary of Mentor. ATMEL is in negotiation with Meta Systems,
  - ATMEL proposes to proceed in 2 steps (TBC) :(1tile = ATF280F capacity)
    - a 1Mg FPGA (4 tiles) : Space rad-hard FPGA manufactured in UMC 90nm technology (TBC)
    - a 2.4Mg FPGA (9 tiles) : Space rad-hard FPGA manufactured in ST 65nm technology (TBC)



2.4Mg FPGA in EPPL in 2015

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  - Reliability
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Conclusion and way forward (1/2)

- The DSM initiative, initially driven by next generation telecommunication satellites, and coordinated within the frame of the CTB, identified critical technologies, namely Broadband ADC and DAC, HSSL, digital ASICs and FPGA for for high integration and processing power applications.
- Strong efforts from ESA, CNES and European Community to support the development and ESCC evaluation of these strategic technologies.
- First ADC, DAC and HSSL prototypes and First 65nm Space Library test-chip are available showing Encouraging results
- Development and ESCC Evaluation on-going
- Highlights :
  - End-users involvement and European harmonisation efforts
  - Close relationship with manufacturers
  - DSM reliability was early taken into account in technology selection and design phases

Conclusion and way forward (2/2)

- **Technical and Business Challenges ahead:**
  - **Establish advance space-quality packaging solutions for DSM ICs**
  - **Secure more institutional funds (EEE critical components) to complete developments and qualification**
  - **Establish sustainable business models for European DSM supply chain.**
  - **Partnerships between manufacturers or key vendors (Foundries, Assembly and Test houses) and institutional support (ESA, Agencies, EC) are a must to succeed and maintain a small volume / expensive technology market, always driven by big volume commercial technology and products.**
  - **Though always low volume, general purpose converters and DSM ICs such as Microprocessors, reprogrammable FPGAs, DSPs should help sustain the business model, in addition to dedicated high-end ASICs for NG Telecom and Scientific payloads.**

We should continue our efforts to give access to European DSM technologies to ensure the competitiveness of European equipment manufacturers

Thank you !

Any questions ?

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