

CNES final presentation

Radiation Characterization of various FRAM, SRAM and Flash memories

Frédéric LOCHON, Hirex Engineering

CNES contacts: Hirex Engineering contact: David DANGLA, Françoise BEZERRA François-Xavier GUERRE



FINGINEERIN^G

Tested parts

Part type	Manufacturer	Package	Function	Testing
R1WV6416RSA	Renesas	TSOP 48	SRAM 4 Mi x 16	SEE
CY7C10612DV33	Cypress	TSOP 44	SRAM 1 Mi x 16	SEE
IDT70V658	IDT	PQFP 208	DPRAM 64 Ki x 36	SEE + TID
FM22L16	Ramtron	TSOP 44	FRAM 256 Ki x 16	SEE + TID
K9WBG08U	Samsung	TSOP 48	Flash 32 Gbit	SEE + TID
MT29F32G08	Micron	TSOP 48	Flash 32 Gbit	SEE + TID
72V2113L10PFI	IDT	TQFP 80	FIFO 256 Ki x 18	SEE
SN74V293-EP	TI	TQFP 80	FIFO 64 Ki x 18	SEE



SRAM/FRAM/DPRAM testing methodology

3/26

₩ SEL

- Supply current monitoring
- Current threshold is about 5 to 10 times the current under dynamic condition
- Hold time is 1 ms
- Power off time is 1 s

₿ SEU

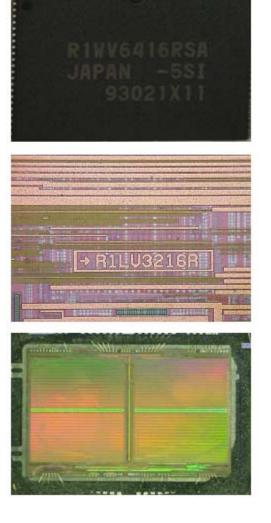
- Dynamic access while beam is on
- □ Full algorithm to detect and flag error type (read error, upset, stuck bit, write error, ...) over the full memory space
- △ No wait time, no lost beam time during the run

SRAM memory Renesas 4 Mi x 16 (1/2)



4/26

- **#** Part type: R1WV6416RSA-5SI
- # Part description: 64 Mibit static RAM organized as 4,194,304 word x 16 bit - 2 die of 32 Mibit
- **#** Manufacturer: Renesas
- ₭ Package: 48 pin TSOP I
- **#** Date code: 0930
- ₭ Die dimensions: 9750 x 6080 µm
- SEE Testing: RADEF (Jyväskylä / Finland), April 2010*, 2 parts

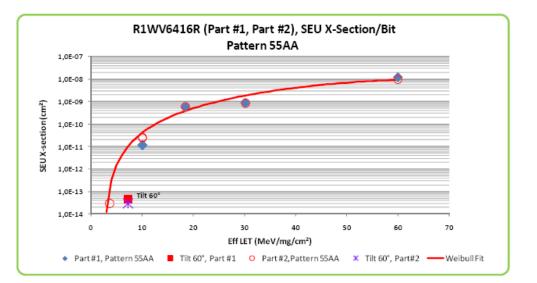


* no ash cloud inside chamber



SRAM memory Renesas 4 Mi x 16 (2/2)

- Second Second
- Some MBU observed (most MBU are 2 bits MBU)
- Hanks to descrambling analysis, MCU have been observed (worst case is 9 cells)



- SEU saturation cross-section
 △ 1.2E-8 cm².bit⁻¹
 LET threshold
 - 2.5 MeV.cm².mg⁻¹

SRAM memory Cypress 1 Mi x 16 (1/2)

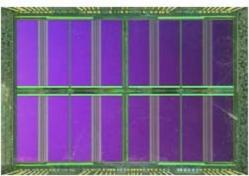


6/26

- **#** Part type: CY7C10612DV33-10ZSXI
- **#** Part description: 1 Mi x 16 bit static RAM
- **#** Manufacturer: Cypress Semiconductor
- ₭ Package: 54 pin TSOP II
- **#** Date code: 1001
- **#** Die dimensions: 6.4 x 4.6 mm
- SEE Testing: RADEF (Jyväskylä / Finland), April 2010^{*}, 2 parts







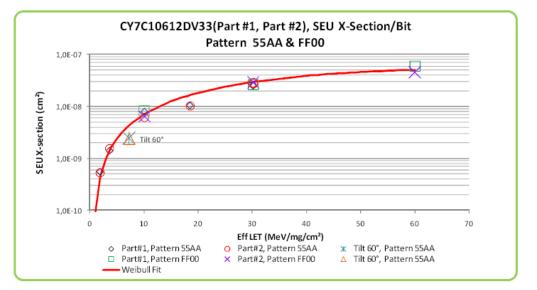
* no ash cloud inside chamber

CNES final presentation



SRAM memory Cypress 1 Mi x 16 (2/2)

- ₭ Few SEL at Xe and 60° angle (LET of 120 MeV.cm².mg⁻¹)
 △ Cross-section: 3E-7 cm²
- Some MBU observed (most MBU are 2 bits MBU)
- % MCU have been observed (worst case is 15 cells wide)



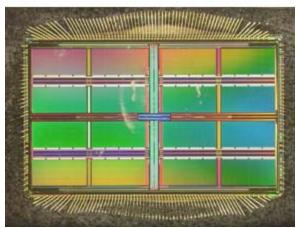
- **#** SEU saturation cross-section
- **#** LET threshold
 - △ 0.5 MeV.cm².mg⁻¹



DPRAM memory IDT 64Ki x 36 (1/3)

- ₭ Part type: IDT70V658
- # Part description: Asynchronous dual-port static RAM, organized as 64Ki x 36 bits
- **#** Manufacturer: IDT
- ₭ Package: 208 pin PQFP
- **#** Date code: 0930
- **#** Die dimensions: 10.843 x 6.885 mm
- **#** SEE Testing: RADEF (Jyväskylä / Finland), July and November 2009, 2 parts
- # TID Testing: ENEA-Calliope (Rome), 5 parts ON, 3 parts OFF, 1 Ref.

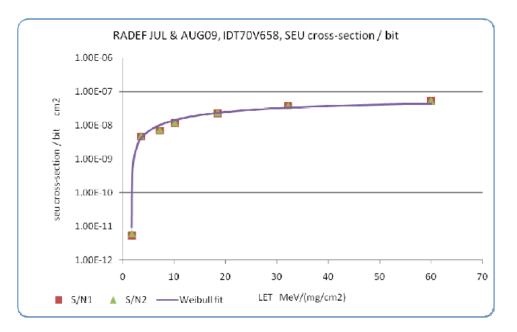




DPRAM memory IDT 64Ki x 36 (2/3)



- Second Second
- **#** SEU results:
- # equivalent sensitivity for 0 to 1
 and 1 to 0 upsets
- **#** No MBU observed
- # LET threshold
 - △ 1.8 MeV.cm².mg⁻¹
- Cross-section saturationM 3.5E-8cm²



DPRAM memory IDT 64Ki x 36 (3/3)



10/26

TID: dose rate 200 rad(Si).h⁻¹

% No significant drift observed up to 100 krad(Si)

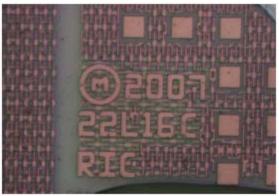
Irradiation Steps	Dose rate	Annealing steps	Temperature
krads	krads/h	Hours	°C
0			
4.6	0.2		Room
8.6	0.2		Room
12.5	0.2		Room
16.7	0.2		Room
49.7	0.2		Room
67.6	0.2		Room
100.6	0.2		Room
		24	Room
		168	100

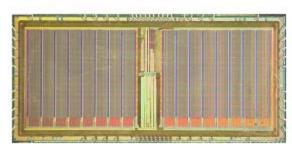


FRAM memory Ramtron 4 Mibit (1/3)

- ₭ Part type: FM22L16-55TG
- # Part description: 256 Ki x 16 non-volatile ferroelectric RAM
- **#** Manufacturer: Ramtron
- ₭ Package: 44 pin TSOP II
- **#** Date code: 0849
- **#** Die dimensions: 6.3 x 2.9 mm
- **#** SEE Testing: RADEF (Jyväskylä / Finland), April 2010^{*}, 2 parts
- **#** TID Testing: ENEA-Calliope, Rome, 5 parts ON, 5 parts OFF, 1 Ref.





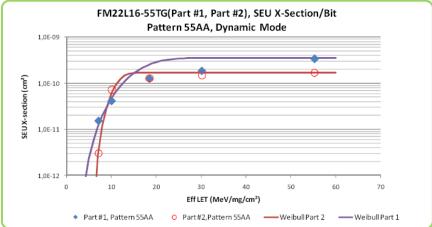


^{*} no ash cloud inside chamber



FRAM memory Ramtron 4 Mibit (2/3)

- SEL at LET of 120 MeV.cm².mg⁻¹ up to a fluence of 1E7 part.cm⁻²
- Under static condition, only few errors observed at Xe
- With dynamic condition, errors from Ne up to Xe



- **#** 0 to 1 upsets are more common
- Some SEFI have been observed from Ar to Xe
 - 11 SEFI, for a cumulated fluence of 5.07E7 part.cm-2
- SEU saturation cross-section
 ∑ 5.9F-8 cm².bit⁻¹
- # LET threshold
 - △ 0.5 MeV.cm².mg⁻¹



FRAM memory Ramtron 4 Mibit (3/3)

- **#** TID dose rate about 212 rad(Si).h-1
- Sleep mode current failed for ON components between 72.2 and 96.6 krad(Si)
- **#** Complete healing after annealing
- **#** Other parameters OK up to 96.6 krad(Si)

Irradiation Steps	Dose rate	Annealing steps	Temperature
krads	krads/h	Hours	°C
0			
6	0.212		Room
9.6	0.212		Room
14	0.212		Room
18.5	0.212		Room
32.5	0.212		Room
52.3	0.212		Room
72.2	0.212		Room
96.6	0.212		Room
		24	Room
		168	100

FIFO testing methodology



14/26

₩ SEL

- Supply current monitoring
- Current threshold is about 5 to 10 times the current under dynamic condition
- Hold time is 1 ms
- \square Power off time is 1 s

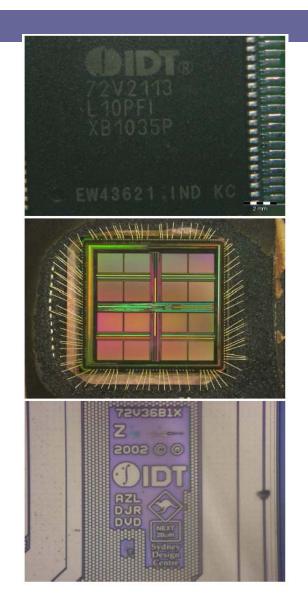
೫ SEU

The memory is fully filled, then fully emptied after a wait period
 During read and write operations, the flags are monitored
 Any flag or data error is time stamped and recorded

FIFO memory IDT 256 Ki x 18 (1/2)



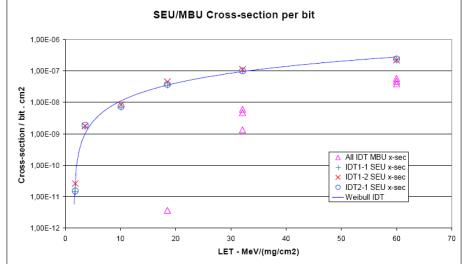
- **#** Part type: IDT72V2113
- # Part description: 4Mbit FIFO organized as 256Ki x 18 bits
- **#** Manufacturer: IDT
- ₭ Package: 80 pin TQFP
- **#** Date code: 1035
- **#** Die dimensions: 7.6 x 7.6 mm
- **SEE Testing: RADEF (Jyväskylä / Finland)**, December 2010, 2 parts





FIFO memory IDT 256 Ki x 18 (2/2)

- SEL have been observed at Xe (LET of 60.0 MeV.cm².mg⁻¹)
 △ Cross-section: 1E-5 cm²
- SEL have been observed at Kr (LET of 32.1 MeV.cm².mg⁻¹) up to a fluence of 1.2E5 part.cm⁻²
- ✗ MBU at Fe (LET of 18.5 MeV.cm².mg⁻¹) and above
 ☑ Worst case MBU is 6 bits
- **#** MCU most likely occured
- # PAF and PAF registers are sensitive
- **SEFI** at Xe. Master reset not OK.

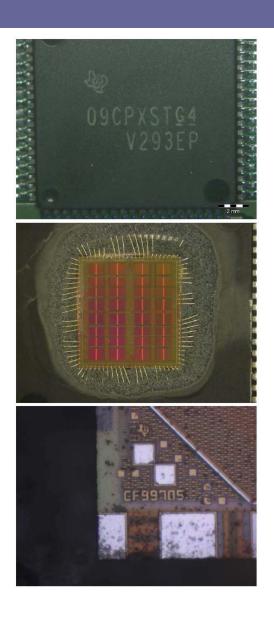


- SEU saturation cross-section
 △ 2.4E-7 cm².bit⁻¹
- **#** LET threshold
 - △ 1.5 MeV.cm².mg⁻¹

FIFO memory TI 64 Ki x 18 (1/2)



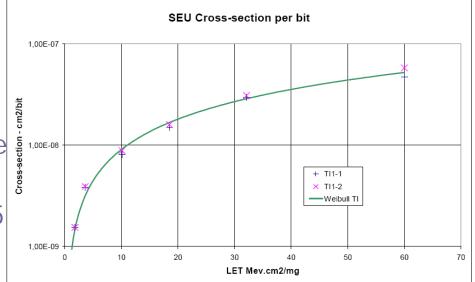
- **#** Part type: SN74V293-EP
- **#** Part description: 64Ki x 18 FIFO
- **#** Manufacturer: Texas Instruments
- **#** Package: 80 pin TQFP
- **#** Date code: 1035
- **#** Die dimensions: 5.7x 6.4 mm
- SEE Testing: RADEF (Jyväskylä / Finland), December 2010, 2 parts



FIFO memory TI 64 Ki x 18 (2/2)



- SEL observed at Xe (LET of 60.0 MeV.cm².mg⁻¹), cross-section is about 5.3E-6 cm²
- SEL observed at Kr (LET of 32.1 MeV.cm².mg⁻¹), with fluence up to 5E5 part.cm⁻²
- ✗ MBU observed at Fe (LET of 18.5 MeV.cm².mg⁻¹) and above
 ☑ Biggest MBU: 2 bits
- Cone flag error associated to a possible upset in PAE register
- **#** One upset in read pointer ?
- **#** SEFI at Fe. Partial reset OK



- % LET threshold
 - □ 1 MeV.cm².mg⁻¹
- **%** Saturation cross-section

Flash testing methodology



19/26

₩ SEL

- Supply current monitoring
- Current threshold is about 5 to 10 times the current under dynamic condition
- Hold time is 1 ms
- \square Power off time is 1 s

₩ SEU

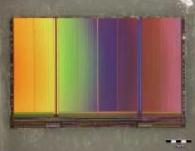
- Different test sequences may be used to get statistics on read/write/erase operations
- Few commands used (Read Page, Page program, Block erase, Read Status)



Flash memory Samsung 32 Gbit (1/3)

- **#** Part type: K9WBF08U1M
- Part description: SLC 4 die stack 32Gbit NAND
 Flash, organized as 4 die x 4096 blocks x 64 pages
 x (4096+128) words x 8 bits
- **#** Manufacturer: Samsung
- ₭ Package: 48 pin TSOP I
- **#** Date code: 0816
- **#** Die dimensions: 15.17 x 9.59 mm
- **#** SEE Testing: UCL (Belgium), June 2009, 3 parts
- # TID Testing: ENEA-Calliope (Rome), 5 parts ON, 3 parts OFF, 1 Ref



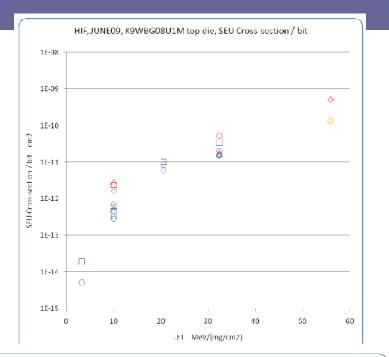




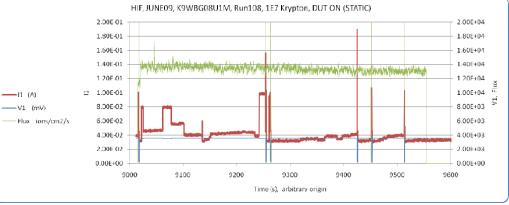


Flash memory Samsung 32 Gbit (2/3)

- Host likely, SEL have not occured or have been hidden by current steps.
- # "block erase" and "page program" errors have been reported by the DUT (via "read status" command)
 - ☑ No such events on S/N1
 - S/N 2 and 3 got more events along the runs up to device failure



- **#** LET threshold
 - △ 3 MeV.cm².mg⁻¹



Flash memory Samsung 32 Gbit (3/3)



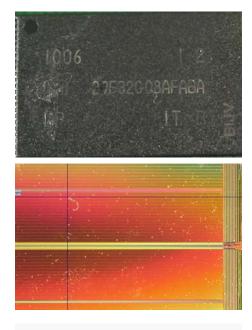
- Stand-by current failed between 20 and 53 krad(Si), complete healing after annealing
- **#** Others parameters OK up to 100 krad(Si)

Irradiation Steps	Dose rate	Annealing steps	Temperature
krads	rads/h	Hours	°C
0			
5.6	200		Room
9.6	200		Room
14.8	200		Room
20	200		Room
53.6	200		Room
68.7	200		Room
96.1	200		Room
		24	Room
		168	100

Flash memory Micron 32 Gbit (1/3)



- **#** Part type: MT29F32G08
- Part description: 3.3V 32 Gbit Flash memory, organized as 2 die x 4096 blocks x 128 pages x (4096+224) words x 8 bits
- **#** Manufacturer: Micron technology
- ₭ Package: 48 pin TSOP
- **#** Date code: 1006
- **#** Die dimensions: 10.7 x 12.8 mm
- **SEE Testing: RADEF (Jyväskylä / Finland), August** 2010, 3 parts
- **#** TID Testing: UCL (Belgium), 5 parts ON, 5 parts OFF, 1 Ref.

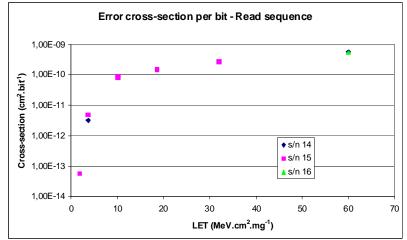


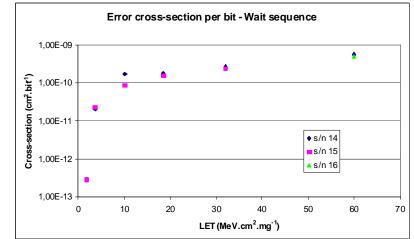


Flash memory Micron 32 Gbit (2/3)



- SEL at Xe (LET: 60 MeV.cm².mg⁻¹) up to a fluence of 9.6E6 cm⁻²
- SEU have been observed from N (LET: 1.8 MeV.cm².mg⁻¹) to Xe
- **%** SEU may only be temporary
- # MBU have been observed, biggest MBU is 5 bits
- # Failure modes may concern addresses, pages, blocks or iterations as soon as Ne (LET of 3.6 MeV.cm².mg⁻¹)
- # "block erase" failures observed only when Fluencerun > 4E5 cm⁻²





Flash memory Micron 32 Gbit (3/3)



25/26

- **#** ON devices failed "stand by current" above 46 krad(Si)
- # Failed parameters after 68 krad(Si): VOH, VIL/VIH, tPROG, tBERS, tWP, tWH, tAR, tCLR, tRP, tREH, tWW, tADL and functionnality

SN11

SN10

SN9

SN8

SN7

SN6

SN5

SN4

SN3

SN2

SN1

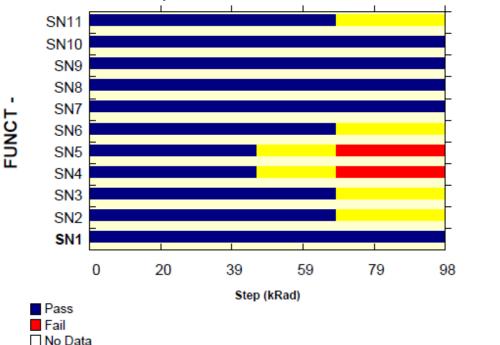
0

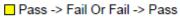
12

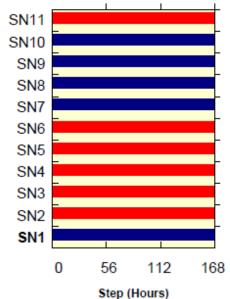
Step (Hours)

24

Other parameters (more than 20) OK up to 98 krad(Si)









Radiation Characterization of various FRAM, SRAM and Flash memories

Thank you !

