P-channel Power MOSFET SEGR Sensitivity to Heavy Ion Range

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Introduction

- **An abundant literature exists & the impact of different parameters are identified**
  - normally incident beam
  - flux and fluence of heavy ion beam
  - test temperature
  - voltage bias during irradiation: VDS et VGS
  - gate oxide thickness

- **SEGR sensitivity and combined impact of :**
  - the surface linear energy transfer (LET),
  - ion species, ion energy and penetration depth,
  - power MOSFET process and EPI layer thickness.

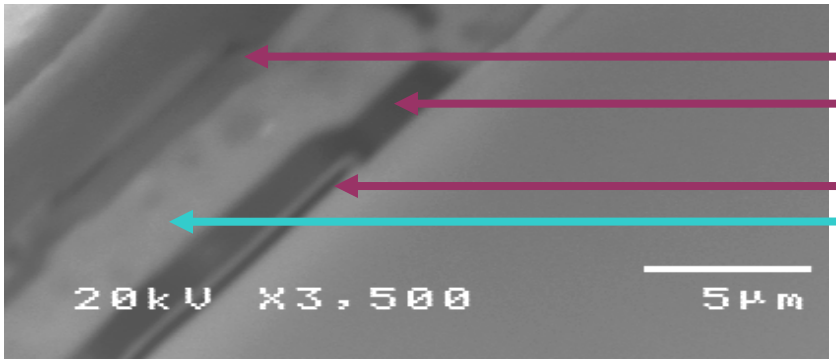
- **A question remains non totally solved**
  - What are the worst-case test conditions for SEE testing of Power MOSFETs ?

Part selection and preparation

- **P-channel COTS power MOSFET from various manufacturers, with different technology and EPI layer thicknesses.**

Reference	Manufacturer	Channel	VDS (V)	VGS (V)	Package
Type 1	Vendor A	P HEXFET	-100	+/-20	TO3
Type 2	Vendor B	P HEXFET	-200	+/-20	TO3
Type 2	Vendor A	P HEXFET	-200	+/-20	TO3
Type 4	Vendor C	P DMOS	-200	+/-30	TO220

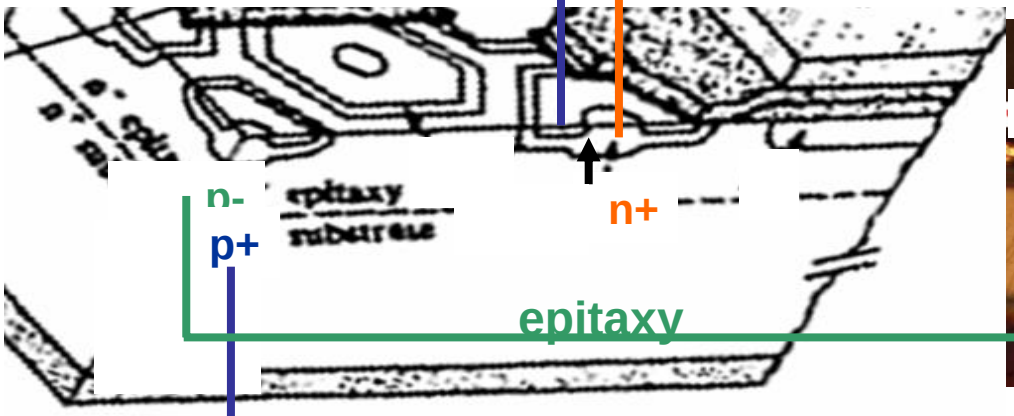
Cross sectioning

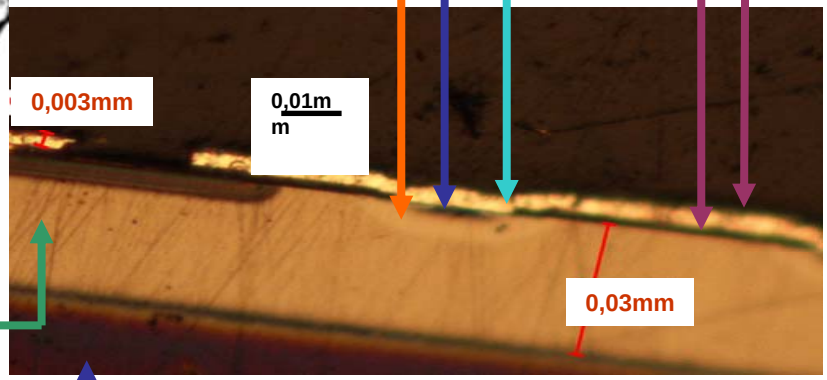


SiO2
~1 to 1.2 µm

Oxyde de grille (SiO2)

Al
~3 µm





HEXFET structure

Microsection

Cross sectioning

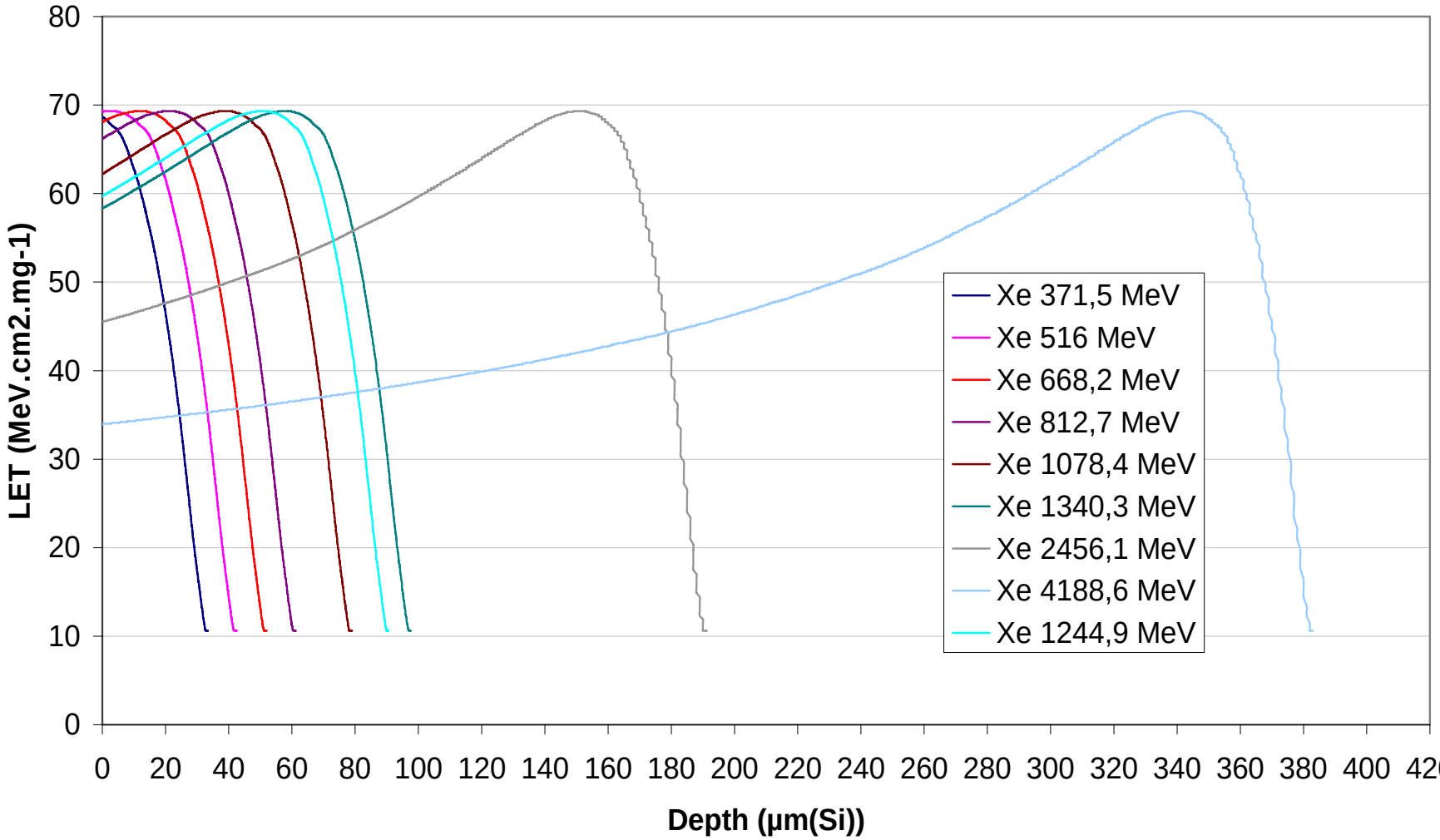
- **Epitaxial layers depths and thicknesses**

Type	Manufacturer	VDS(max) (V)	Passivation (µm)	Epitaxial Depth (µm)	Epitaxial Thickness (µm)	Die thickness (µm)
Type 2	Vendor B	200	5.5	35.5	30	400
Type 2	Vendor A	200	8.95	37.95	29	400
Type 1	Vendor A	100	5.8	17.8	12	400
Type 4	Vendor C	200	6.2	27.2	21	280

Tests campaigns

- **2 test campaigns at the UCL (Belgium)**
  - Xe, Kr (high range and high LET cocktails)
- **3 test campaigns at the GANIL (France)**
  - Xe, Kr
  - Irradiations performed in air.
  - surface LET and range adjusted by tuning the air thickness and the aluminium degrader thickness between beam output and DUT.
  - parts irradiated with different charge deposition across the sensitive layer

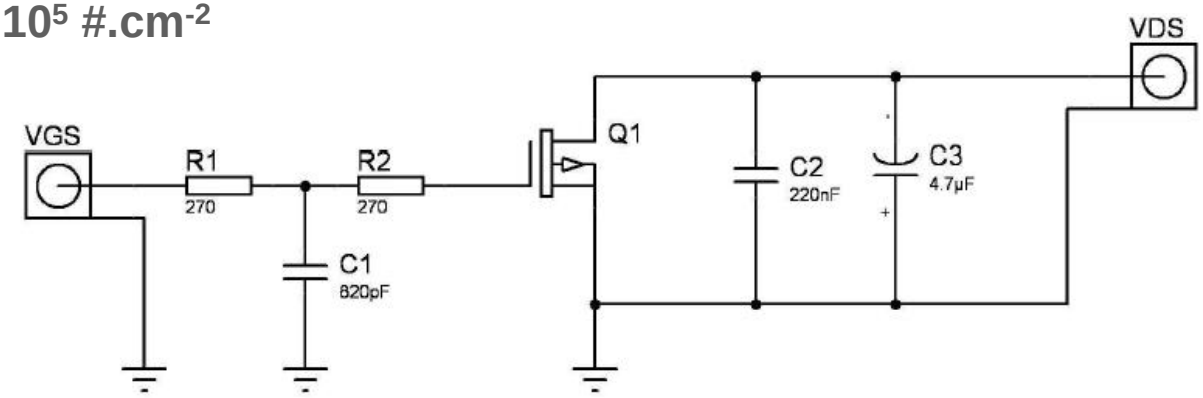
Xe energy and Range used in GANIL experiment



Ploted with SRIM Code as implemented in **OMERE** (http://www.trad.fr/OMERE-Software.html)

Tests description

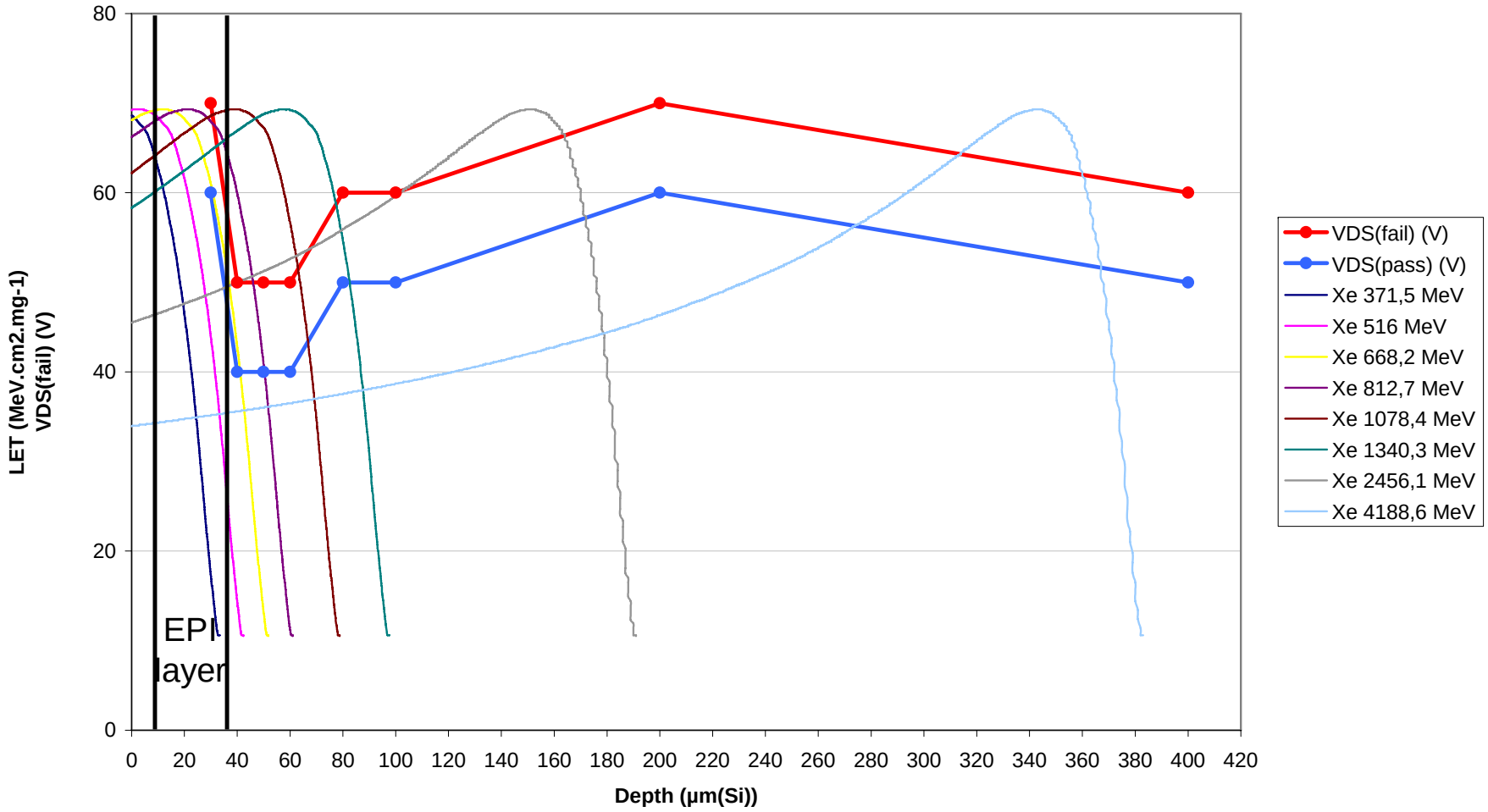
- **Tests Conditions**
  - Constant flux : 10^3 #.cm^{-2}.s^{-1}
  - Constant fluence : 3.10^5 #.cm^{-2}
- **SEGR if Igs> 100nA**
- **New part at each run**
- **VGS voltage is fixed**



- **VDS threshold determination for different Ranges**
  - « VDSpass » confirmed on 2 parts
  - PIGS if no SEGR during irradiation

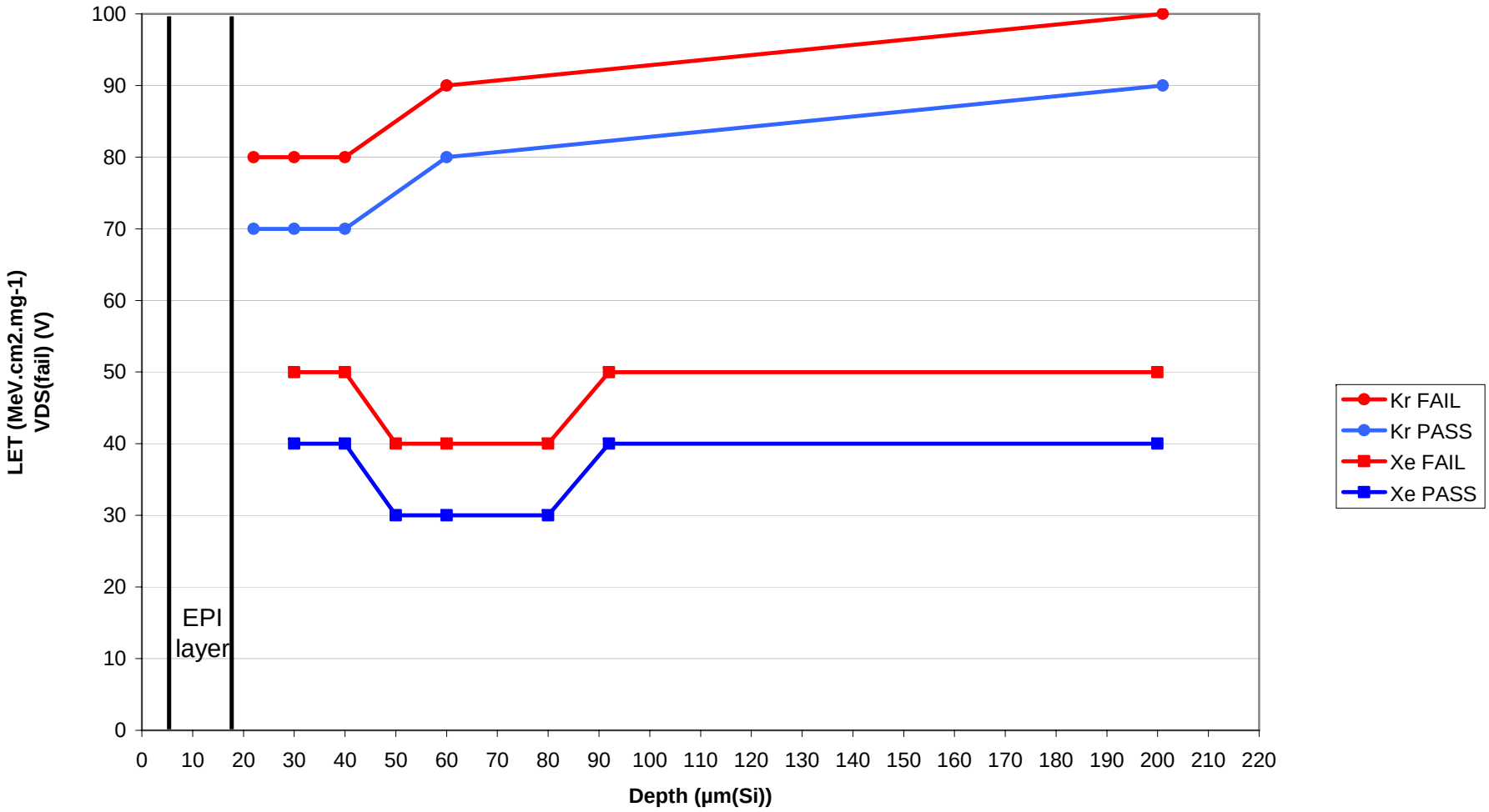
Test results

- Type 2 Vendor A (200V), VDS thresholds @ VGS=16V (80% VGS max)



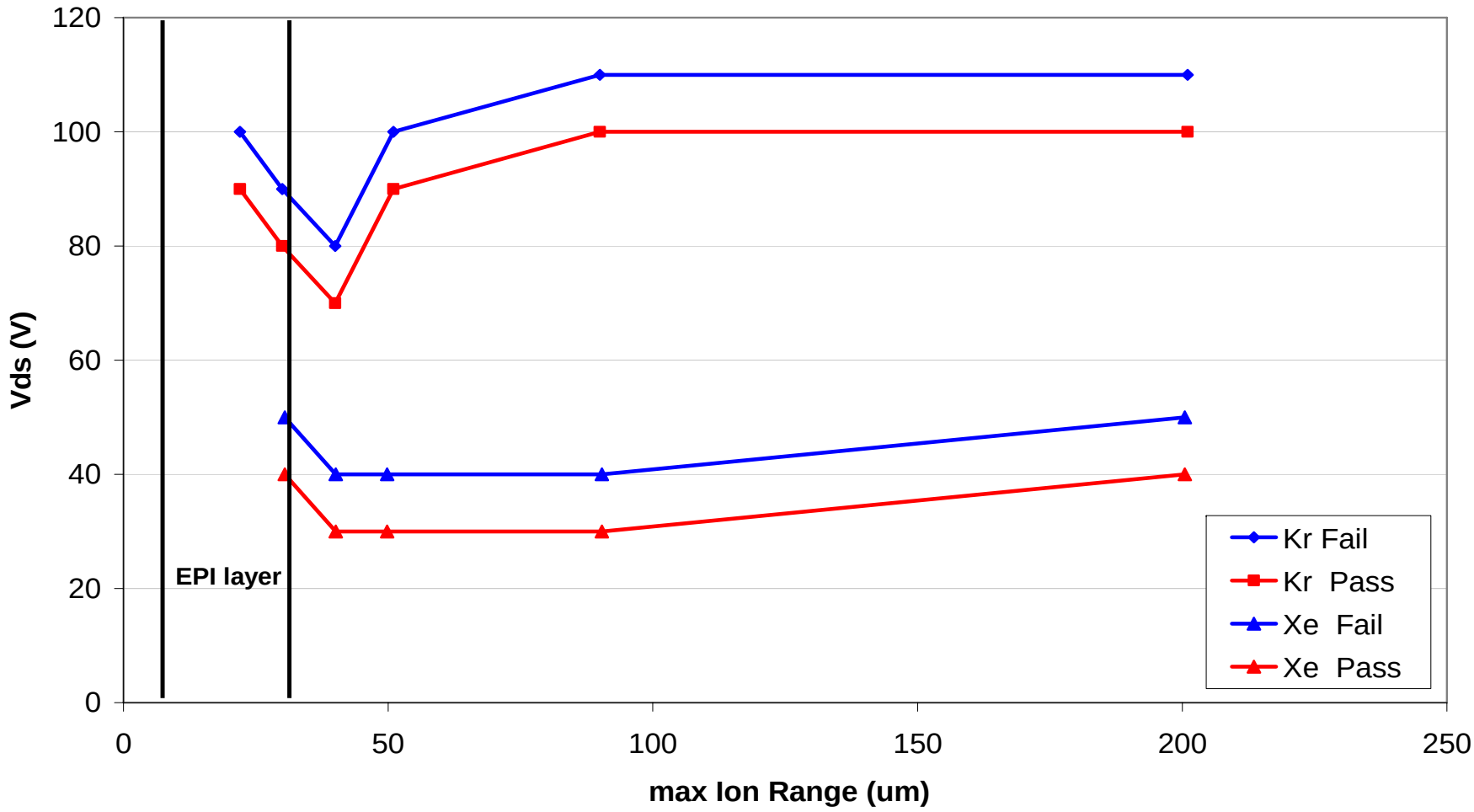
Test results

- Type 1 Vendor A (100V), VDS thresholds @ VGS=8V (40% VGS max)



Test results

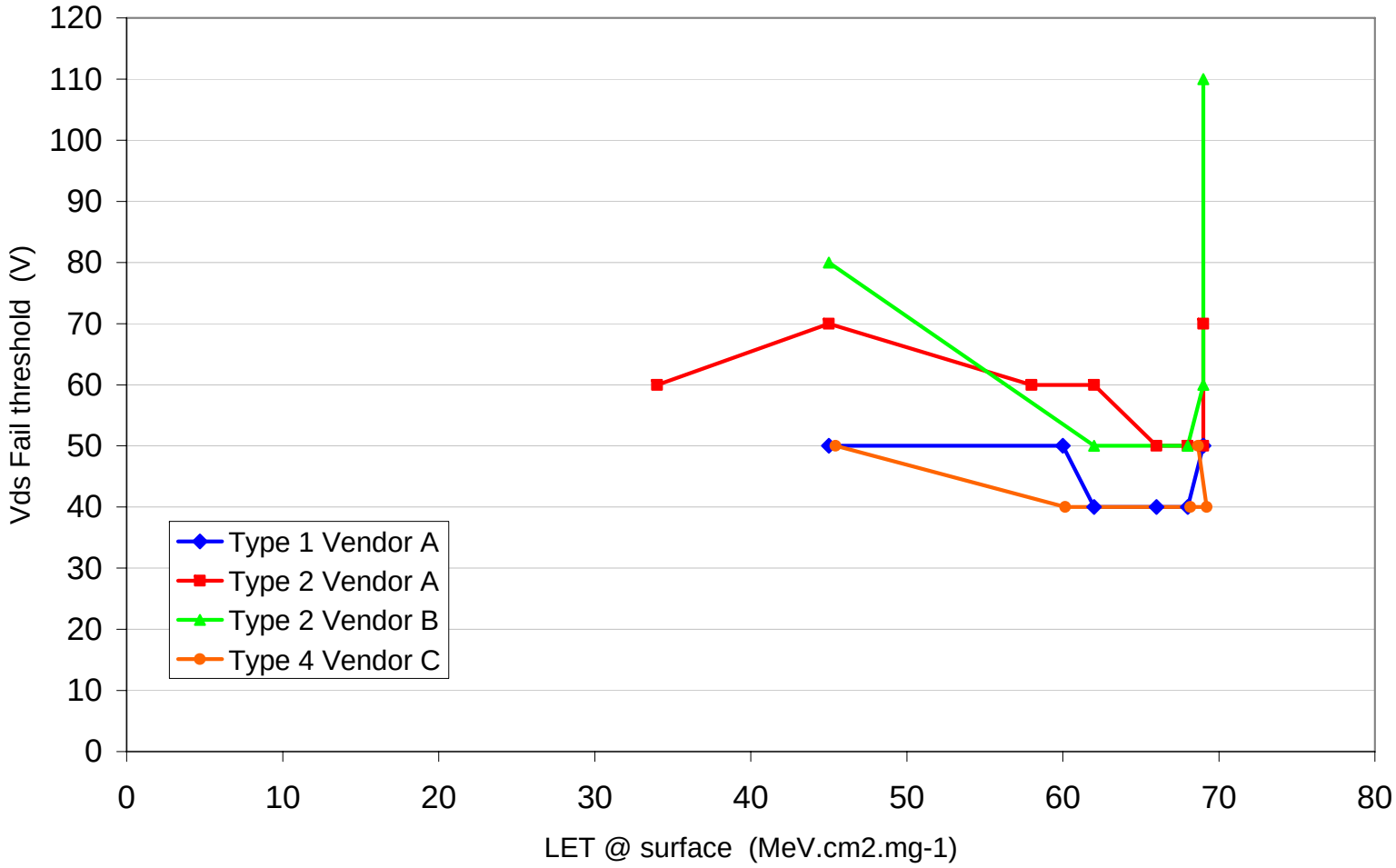
- Type 4 Vendor C (200V), VDS thresholds @ VGS=18V (60% VGS max)



Test results

- **All the results confirm**
  - **the existence of a worst case range corresponding to the worst SEGR part sensitivity.**
    - neither obtained with the short-range ion
    - nor with the long-range ion.
  - **The worst-case range is an intermediate value close to the depth of the epitaxial layer.**
  - **the worst case range depends on the ion species, that is to say the surface LET value.**

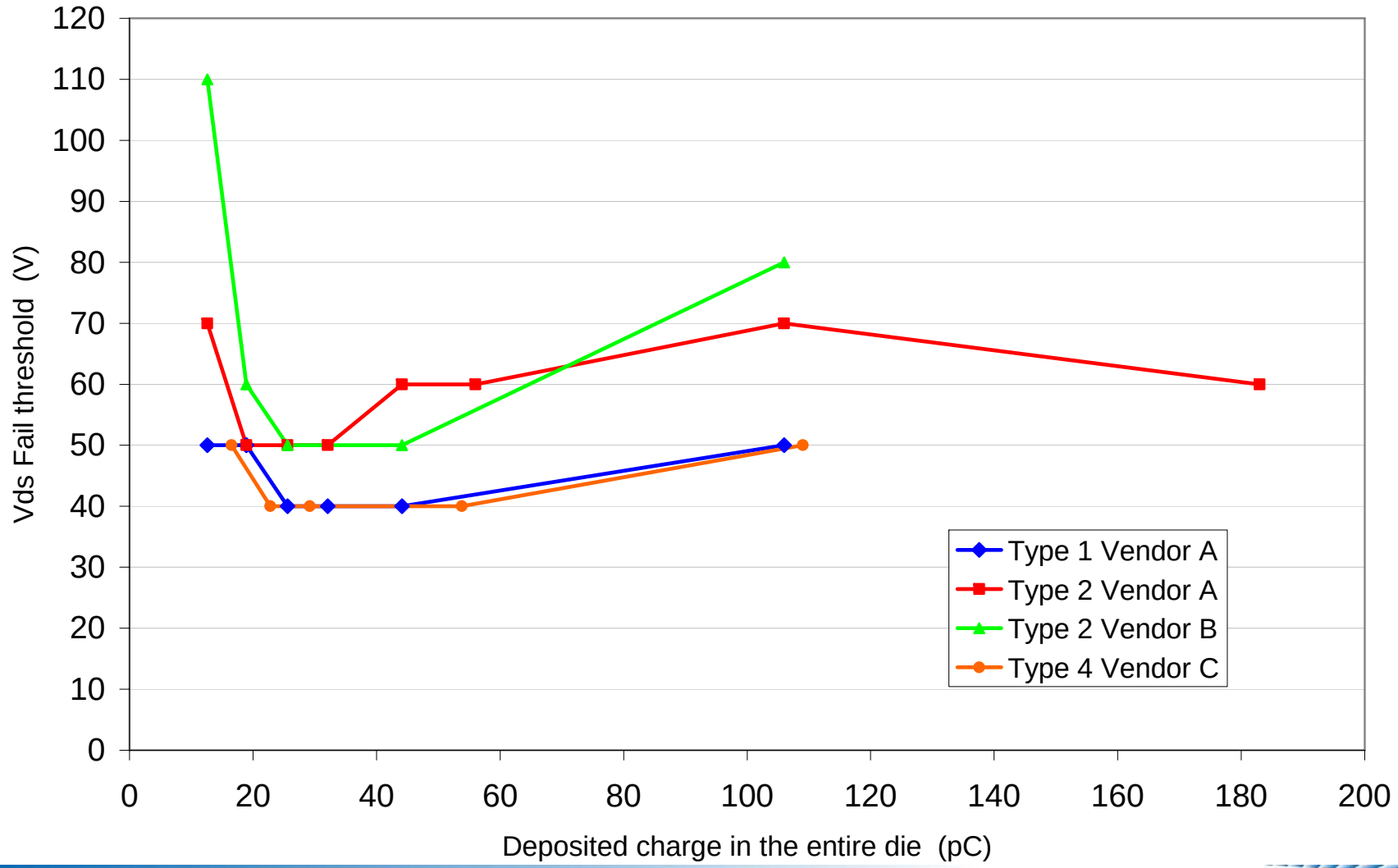
LET @ surface



- **surface LET is not a sufficient criteria to estimate the sensitivity.**
  - it remains as an important parameter to take into account when choosing an ion type for a test

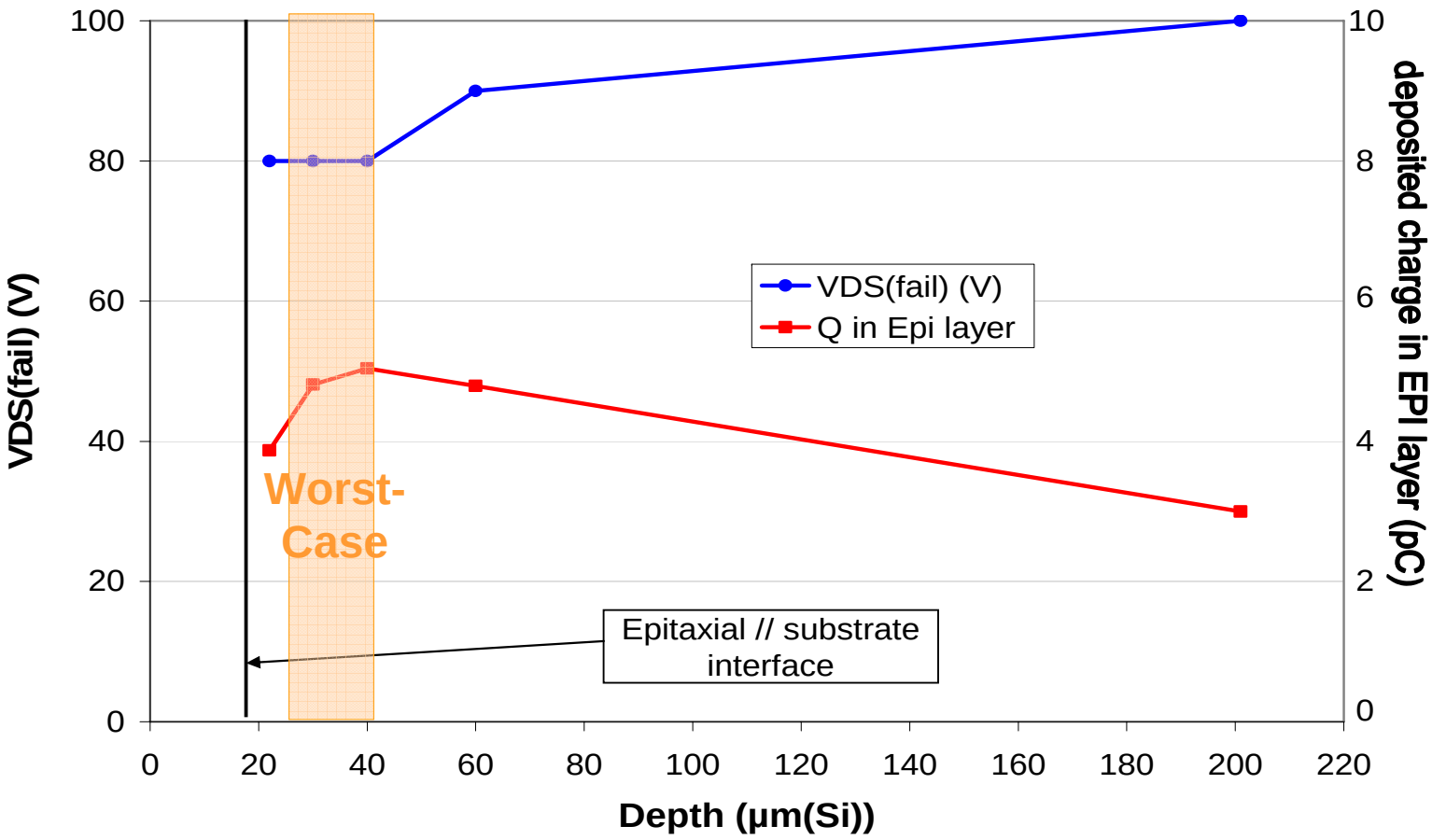
Deposited charge in the entire die

VDS fail threshold versus deposited charge in the entire die for Xe (GANIL)



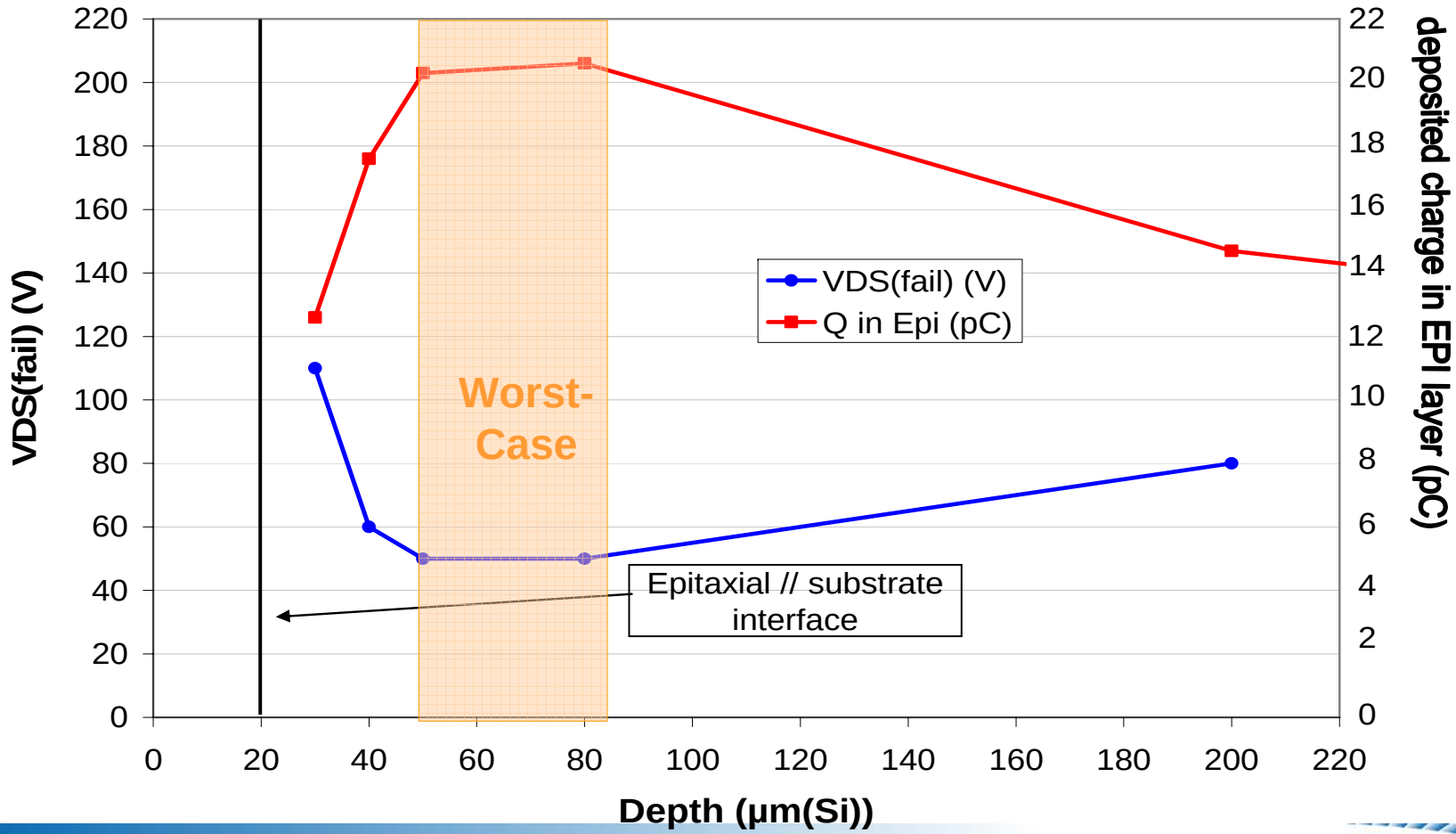
Deposited charge in the epitaxial layer

- VDS fail threshold and energy deposition in Epi layer versus Kr range
  Type 1 Vendor A



Deposited charge in the epitaxial layer

- VDS fail threshold and energy deposition in Epi layer versus Xe range
  Type 2 from Vendor B



Worst-case range domain

- **Bragg peak located near the interface of the epitaxial and substrate layers**

- **the shape of the charge deposition seems to be an important parameter.**
  - **A constant charge deposition along the ion track associated to relatively high surface LET leads to the worst VDS threshold**

Worst-case heavy ion characteristics

- High surface LET
- A constant charge deposition along the ion track in the epitaxial layer
- Complete penetration of the epitaxial layer and Bragg peak near the interface of the epitaxial and substrate layers
- Maximum charge deposition in the epitaxial layer

SEGR test method

- **(1) Part sectioning to measure the layer thicknesses**
- **(2) Possible beam characteristics: list the available ion characteristics (species and energy)**
- **(3) Test preliminary calculations : surface LET, mean LET in sensitive area, range and deposited charge in EPI layer calculations**
- **(4) Estimated worst-case beam determination:**
  - **the worst-case configuration is the one that maximizes the deposited charge in the EPI layer**
    - High surface LET
    - A constant charge deposition along the ion track in the epitaxial layer
    - Complete penetration of the epitaxial layer and Bragg peak near the interface of the epitaxial and substrate layers

Conclusions & Perspectives

- **Conclusions**
  - The objective : to analyze the impact of the parameters involved in SEGR sensitivity on different COTS MOSFET
  - surface LET value as total deposited charge in the entire die
    → not sufficient criteria to estimate the sensitivity
  - The deposited charge in EPI layer
    → the most meaningful criteria.
  - The range of the particle needs to be long enough to completely cross the EPI layer.
  - Bragg peak located near the interface of the epitaxial and substrate layers
- **Perspectives**
  - similar study on N channel power MOSFETs, to extend our observations to SEGR / SEB combined phenomena.
  - SEGR rate calculation improvement, taking into account the deposited charge into the epitaxial layer instead of the surface LET.