A3PE3000L - ACTEL FLASH FPGA - IRRADIATION TEST RESULTS

ESA contract No 22327/09/NL/SFE – ProASIC3L Family Flash Based FPGA

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Reference Documents

- RD1

  S. Rezgui & al., “New Reprogrammable and Non-Volatile Radiation Tolerant FPGA: RTA3P,” presented at RADECS 2007, Deauville, France, September 2007

- RD2

  S. Rezgui & al., “New Methodologies for SET Characterization and Mitigation in Flash-Based FPGAs,” IEEE Trans. Nuc. Sci., vol, 54, n°6, pp. 2512-2524, Dec. 2007

- RD3

  ECSS Q 60-02, “Space Product Assurance, ASIC and FPGA development,” July 2007

Summary

- Background and Objectives
- Device overview
- Statement Of Work (SOW) requirements
- Test Vehicle designs
- Test conditions
- Radiation test results
- Conclusion

Steps

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Background and Objectives

- ProASIC3 Flash Based FPGA (ACTEL)
- Reprogrammable and Non-Volatile
- > 1 Millions gates
- Previous ACTEL test results (RD1 and RD2)

=> Very attractive for space applications

Steps

- Background and Objectives
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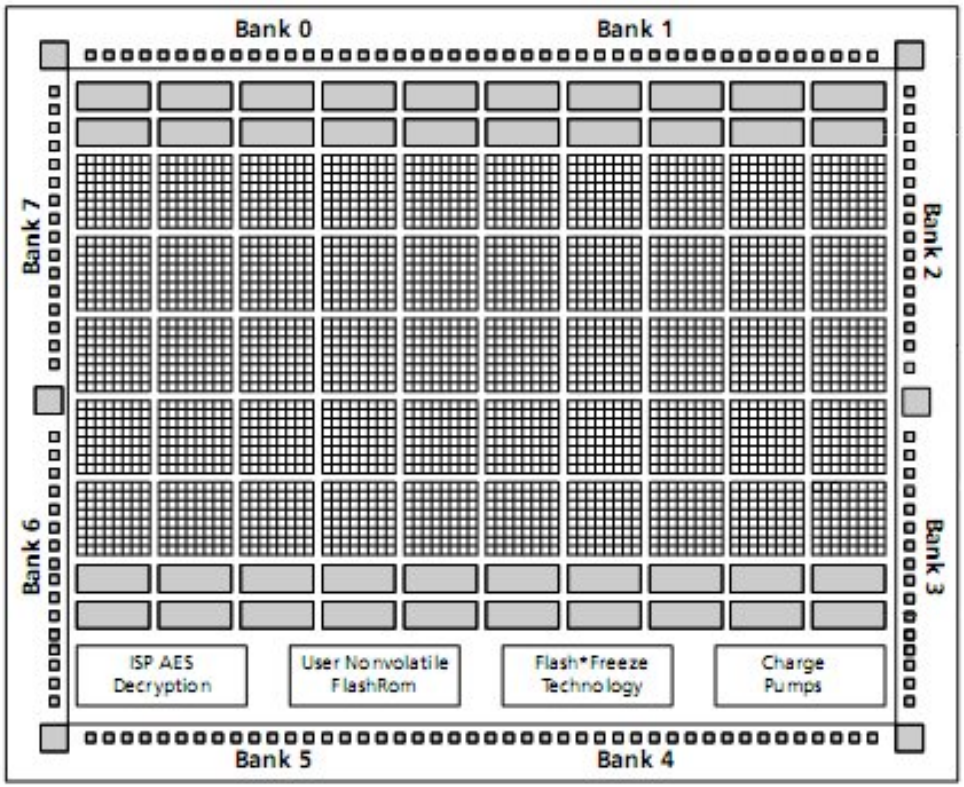
Device overview

- A3PE3000L
  ProASIC3L Family
- Commercial
- 0.13 µm Technology
- PQ 208
- Radiation-Tolerant
  RT ProASIC3L
- RT3PE3000L / A3PE3000L same silicon



Steps

- Background and Objectives
- Device overview
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- Test conditions
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SOW - Requirements (1/2)

- A3PE3000L radiation test (Hls, protons, TID)
- SEL, SEFI, SEU, SET and SEGR sensitivities
- Temperature: room up to 125 °C
- Frequencies: 2, 50, 100 and 200 MHz
- 2 Test Vehicle (TV) Designs:
  - TV1 - Characterization of the FPGA
  - TV2 - Characterization of SEE mitigation methods

Reference Documents: RD1, RD2, RD3

SOW - Requirements (2/2)

- TV1
  - 14 SRs (1024 R-cells) with different I/O standards
  - SRAM, UFROM
  - CCC/PLL
- TV2
  - SRs (1024 R-cells) with SEU & SET mitigation methods

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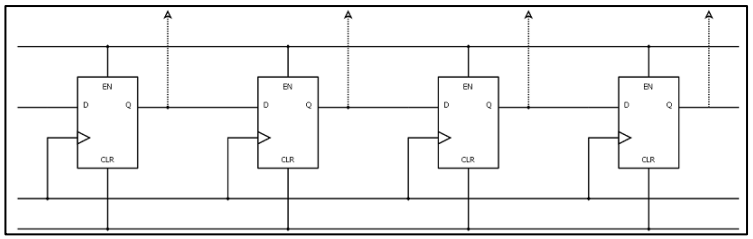
TV1 - Shift Registers

- 14 SRs
- Different clock sources and I/O Types
- Frequency up to 200 MHz

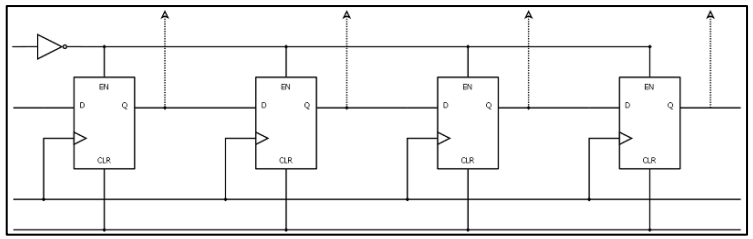
Shift Register	Clock source	I/O Type	Singularity
1	External	3.3 V LVCMOS	Reference
2	External	3.3 V LVCMOS	Enable C-cells
3	External	3.3 V LVCMOS	Clear C-cells
4	External	3.3 V LVCMOS	C-cells in-between R-cells
5 to 8	External	3.3 V LVCMOS DDR	DDR registers
9 to 10	External	2.5 V LVDS	LVDS buffers
11 to 14	Internal PLL	3.3 V LVCMOS	PLL Clock

TV1 - SR 1 to 4

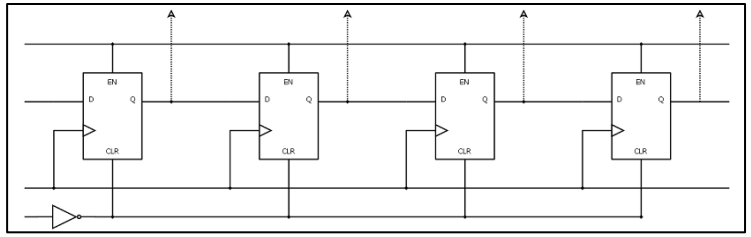
HIREL EXPERTISE HIREX ENGINEERING a company of Alter Technology Group



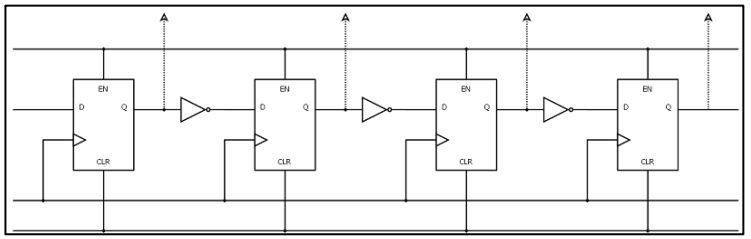
SEU on registers



SEU on registers
SET on enable signal



SEU on registers
SET on clear signal



SEU on registers
SET on C-cells

TV1 - SR 5 to 14

- Cores are identical to the SR 1
- 4 Channels with DDR I/O registers
  - SEU on registers and on DDR I/O registers
- 2 Channels with LVDS I/O buffers
  - SEU on registers
  - SET on LVDS I/O buffers
- 4 Channels clocked by the PLL output
  - SEU on registers
  - SEU and SET on the CCC / PLL

TV2 - Shift Registers

- 6 SRs including SEE mitigation methods
- Frequency up to 75 MHz

Shift Register	Sequential Cell Triplication	I/O Block Triplication	SET Filtering	Combinational Cell Duplication	Combinational Cell Triplication
1	×				
2	×	×			
3			×		
4	×	×	×		
5	×	×		×	
6	×	×			×

SRAM & UFROM

- Only on the TV1
- SRAM
  - 112 Blocks of 512 Words of 9 Bits
  - Frequency up to 20 MHz
- UFROM
  - 8 Banks of 16 Words of 8 Bits
  - Frequency up to 10 MHz

Miscellaneous Parts

- CCC / PLL:
  - Only on the TV1
  - Static mode (single frequency) set on 200 MHz
  - Output clock used to clock 4 SRs (TV1)
  - Lock signal supervised
- Configuration Flash, Charge pump and ISP
  - Verification of the functionality
  - Verification of the re-configurability

TVs - Design Results

- TV1

  14 SRs, 100 % of the Memories, 1 CCC with PLL, several I/O standards

  => 32 % of the logic core, 93 % of I/O

- TV2

  6 SRs, no memory, no PLL, LVCMOS 3.3V

  => 97 % of the logic core, 52 % of I/O

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Power Supplies

- 13 power supplies
  - VCC: 1 x Core supply - 1.5 V nom
  - Vbanks: 8 x Banks supplies - 2.5 or 3.3 V nom
  - VPLLs: 2 x CCC / PLL supplies - 1.5 V nom
  - VJTAG: 1 x JTAG supply - 3.3 V nom
  - VPUMP: 1 x PUMP supply - 3.3 V nom

- V nom + 10 % for SEL tests

Test set-up

- Heavy ions: RADEF 2 campaigns
- Protons: PIF 1 campaign
- TID: design process is running
- Test sequence: fill / expose / check
- Dynamic, static and flash-freeze tests
- Selectable frequencies (up to > 200 MHz)
- Standard patterns (checkerboard and static)
- Specific algorithms

Configuration Flash Set-up

- Configuration sequence under beam:

  erase / program / check - using ACTEL tool

- Status declared by:
  - Success of operation (program passed / failed)
  - Design functionality
  - Verification of the re-configurability

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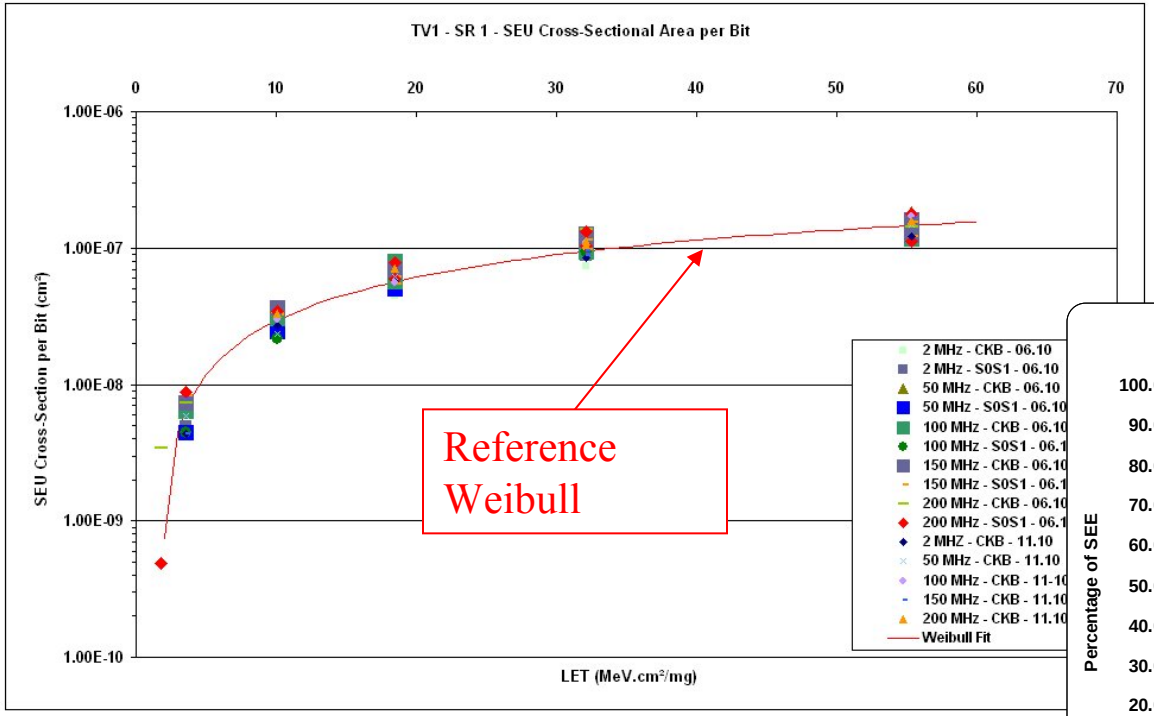
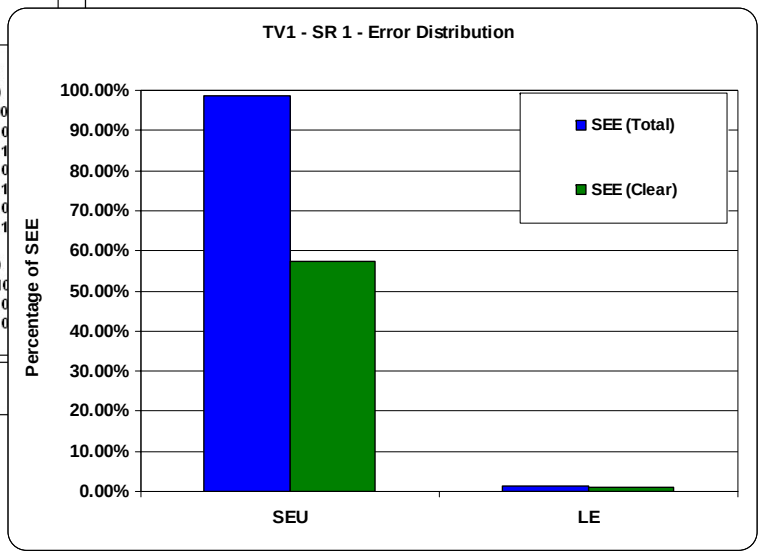
(1/14) - TV1 - SR 1

Reference channel - standard shift register



Reference Weibull parameters:

- K = 1
- λ = 80
- X_0 = 1.8 MeV.cm²/mg
- **CSsat = 3E-7 cm²**

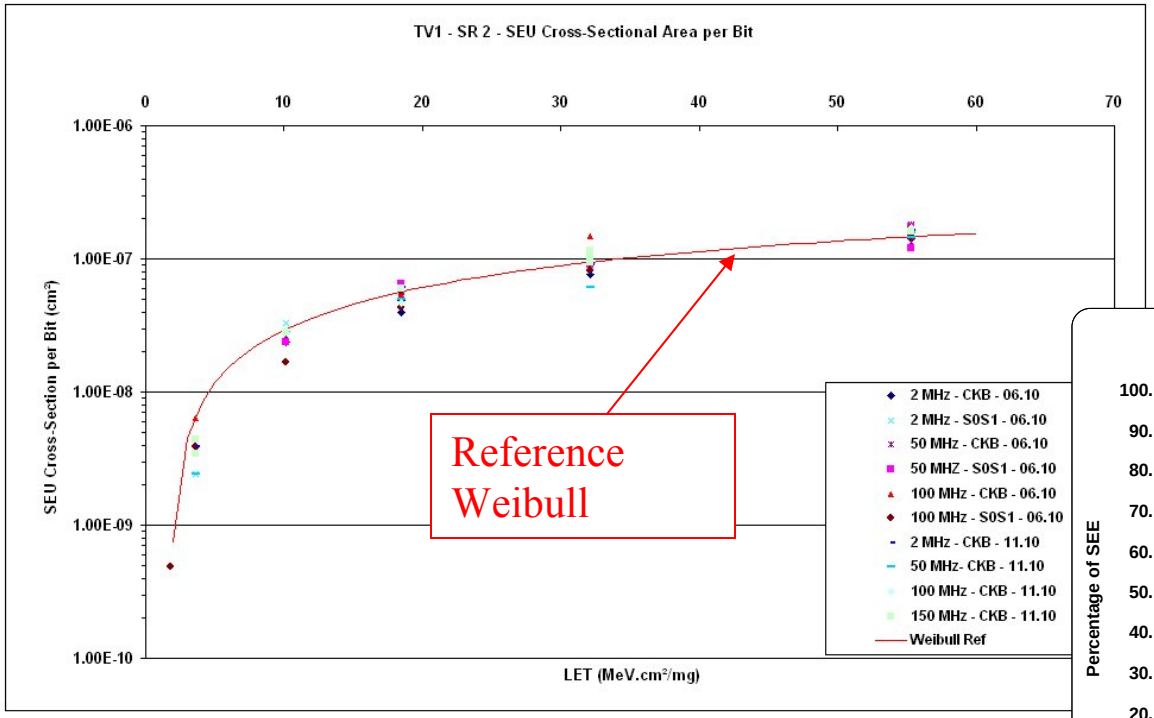


Proton: @230 MeV, CSsat < 1E-13 cm²

Low sensitivity => 1E11 p/cm² => Large dose => limits the characterization => 230 MeV

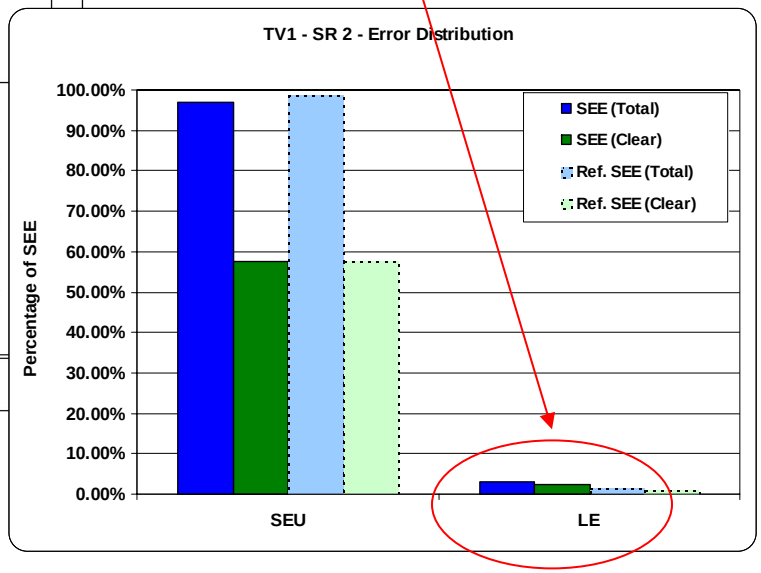
(2/14) - TV1 - SR 2

Channel with C-cells in the enable signal



Reference Weibull

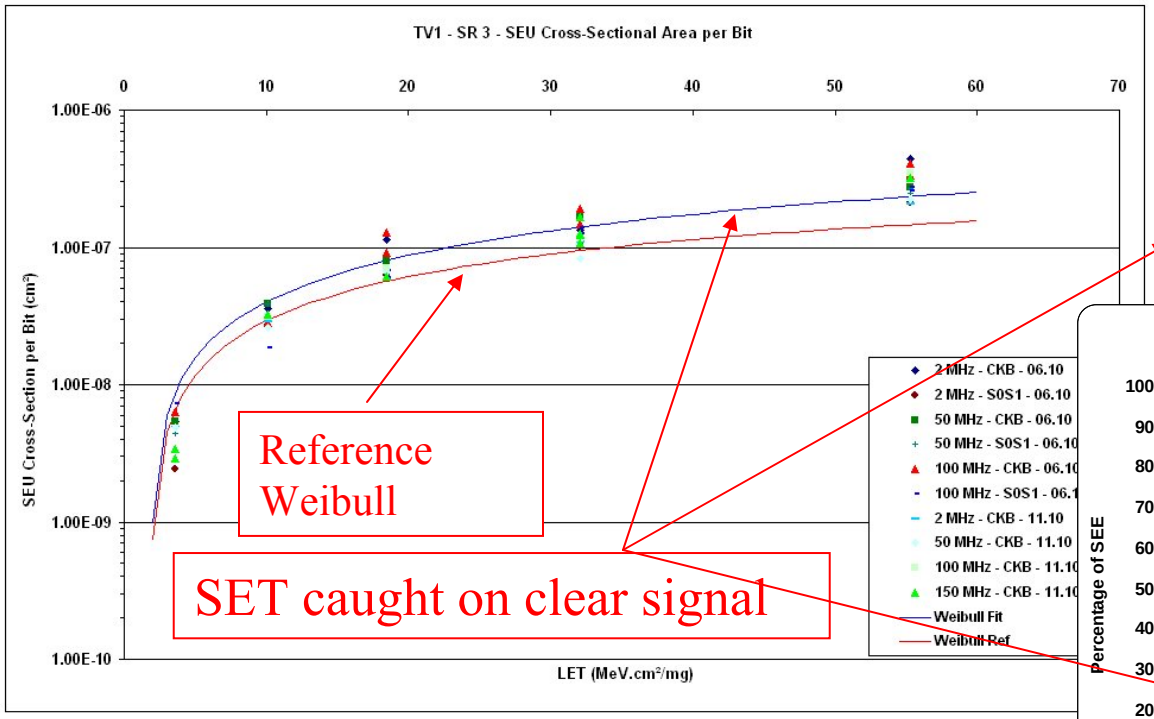
SET caught on enable signal



Proton: @230 MeV, CSsat < 1E-13 cm²

(3/14) - TV1 - SR 3

Channel with C-cells in the clear signal



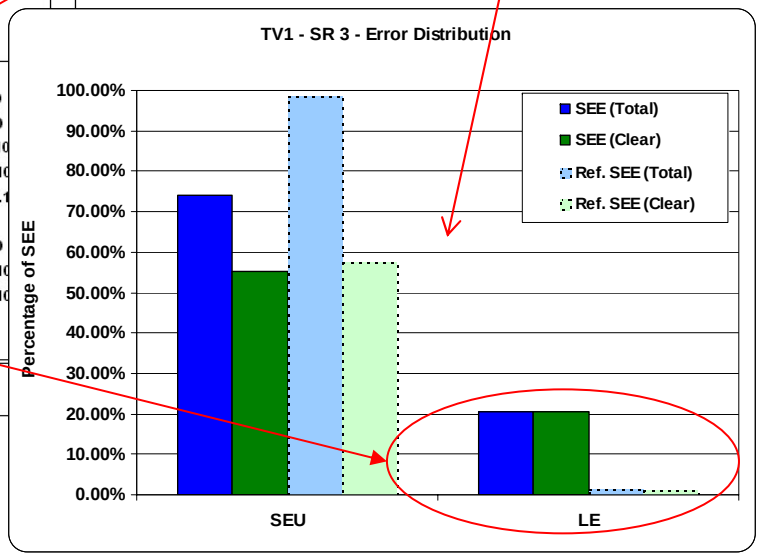
Reference Weibull

SET caught on clear signal

SEU Vs. LE ratio

Weibull fit parameters:

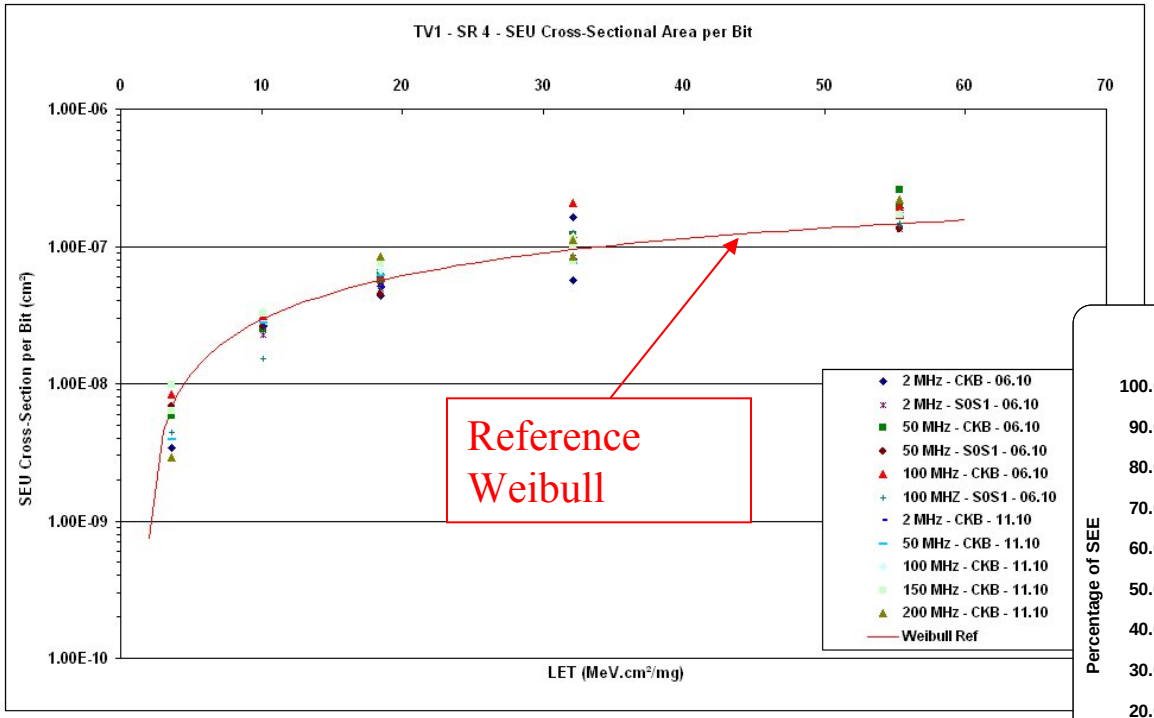
- K = 1
- λ = 200
- X_0 = 1.8 MeV.cm²/mg
- **CSsat = 1E-6 cm²**



Proton: @230 MeV, CSsat < 1E-13 cm²

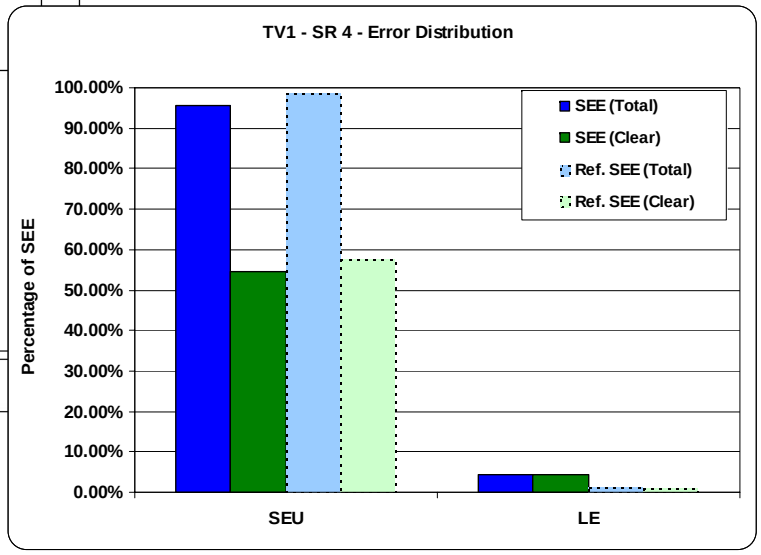
(4/14) - TV1 - SR 4

Channel with C-cells in-between registers



Reference Weibull

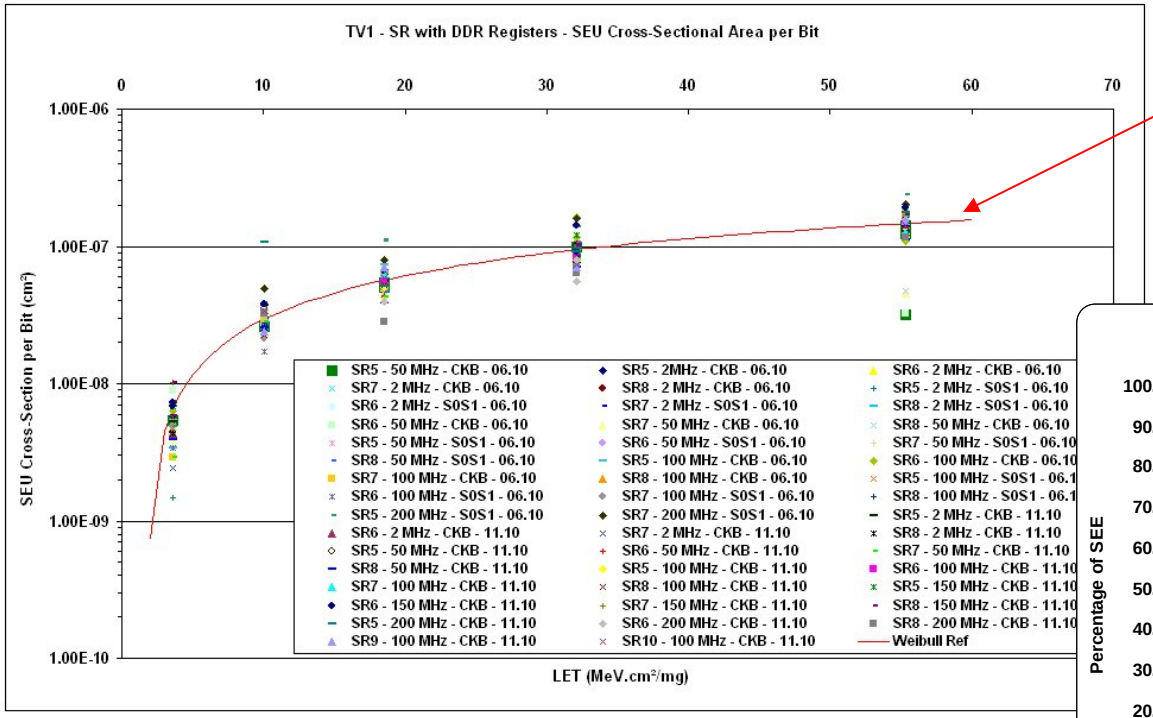
Few SETs caught



Proton: @230 MeV, CSsat < 1E-13 cm²

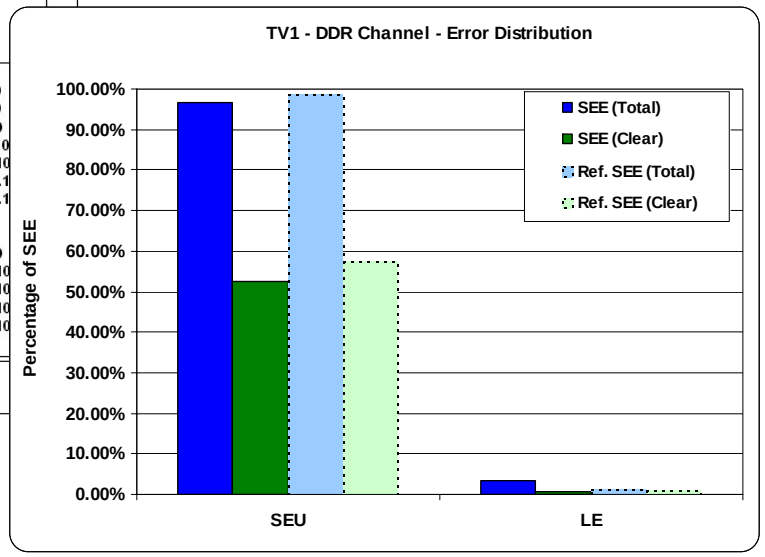
(5/14) - TV1 - SR DDR

Channels with DDR registers



Reference Weibull

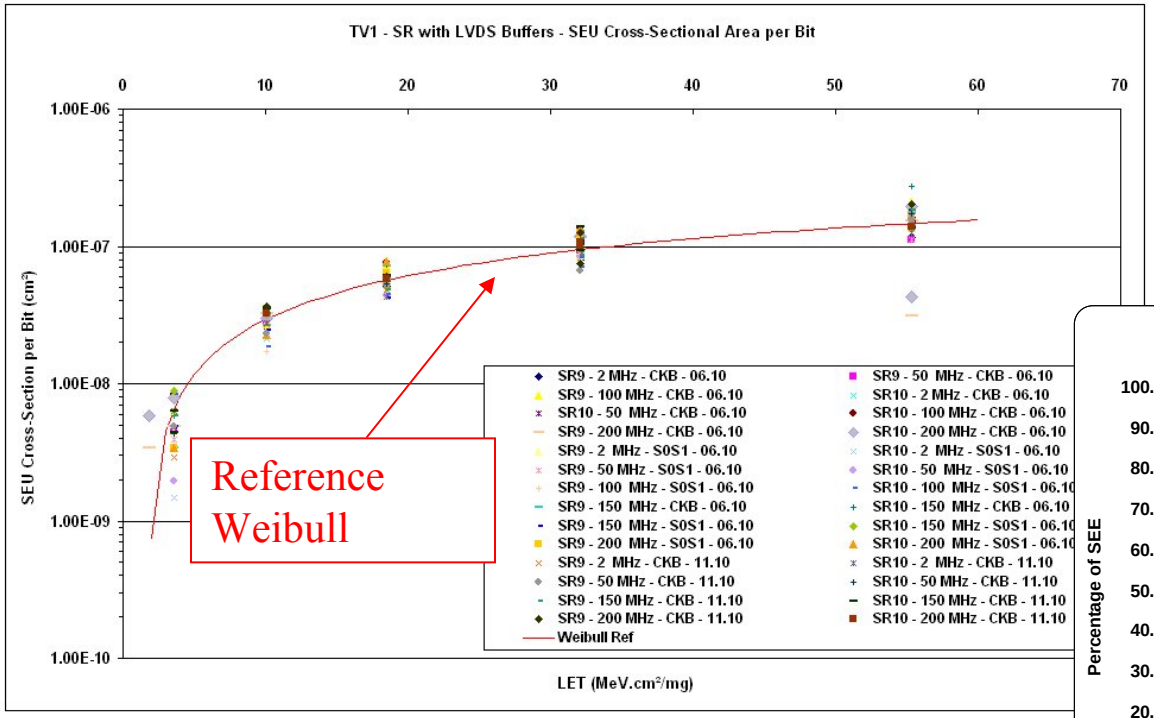
Very similar



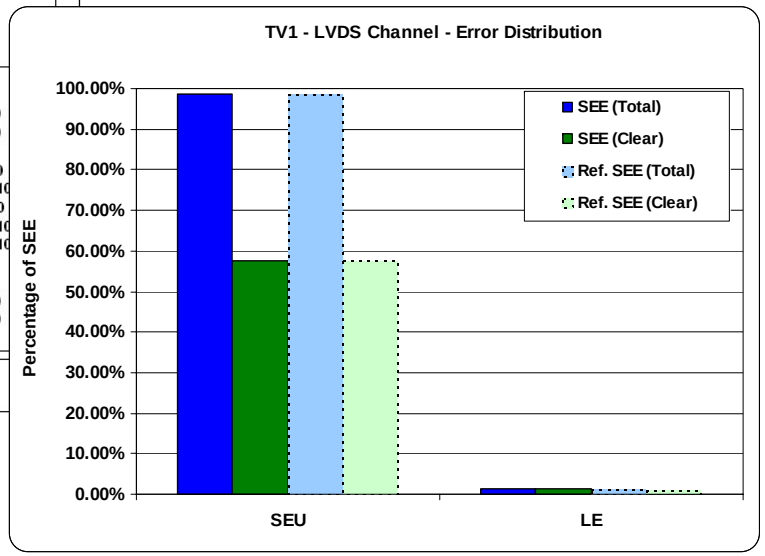
Proton: @230 MeV, CSsat < 1E-13 cm²

(6/14) - TV1 - SR LVDS

Channels with LVDS buffers



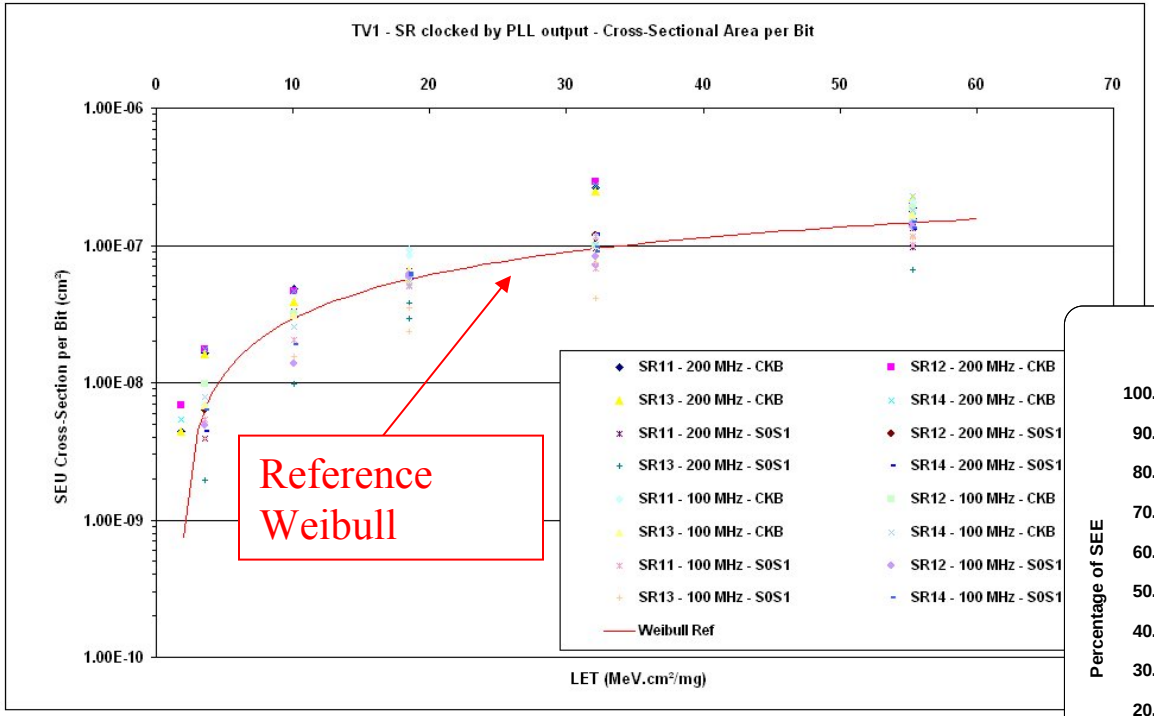
Very similar



Proton: @230 MeV, CSsat < 1E-13 cm²

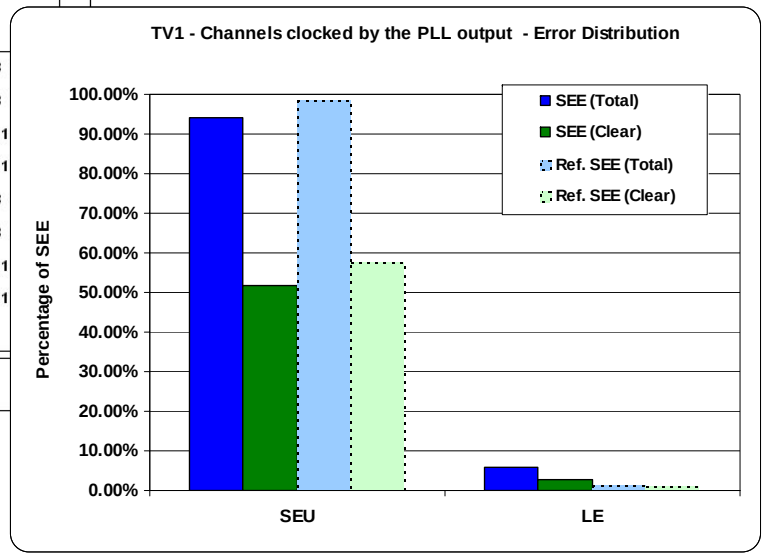
(7/14) - TV1 - SR PLL

Channels clocked by the PLL output



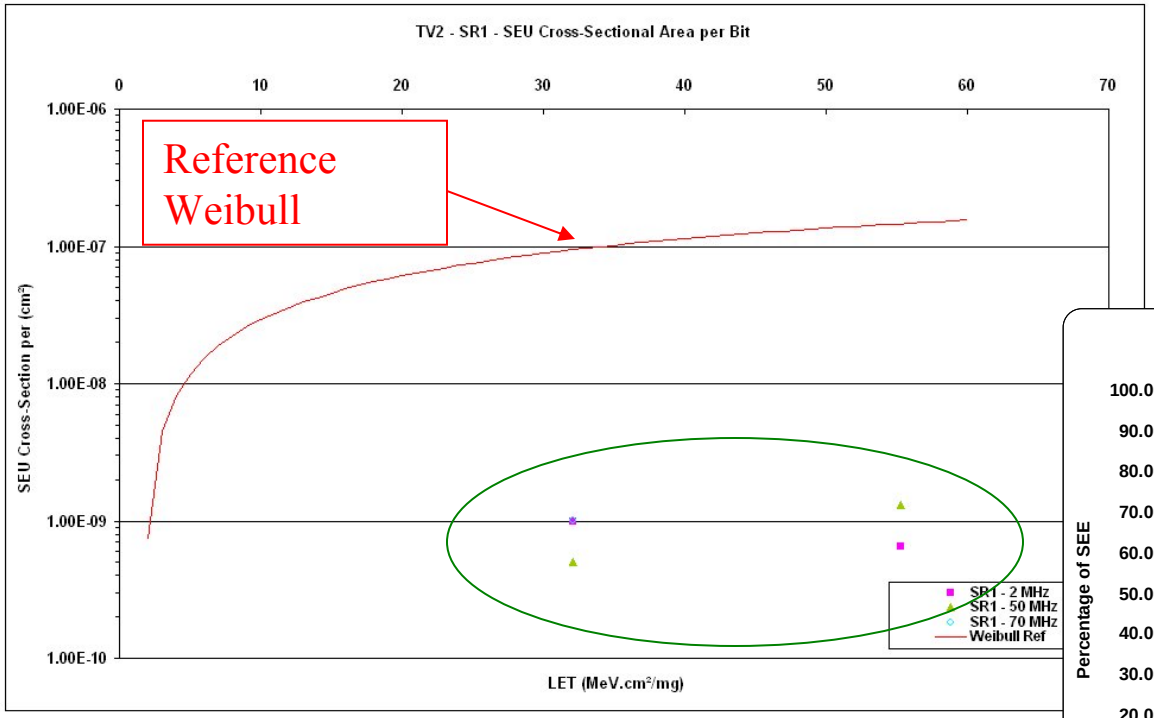
Few PLL clock errors:

Locally several bits flipped



(8/14) - TV2 - SR 1

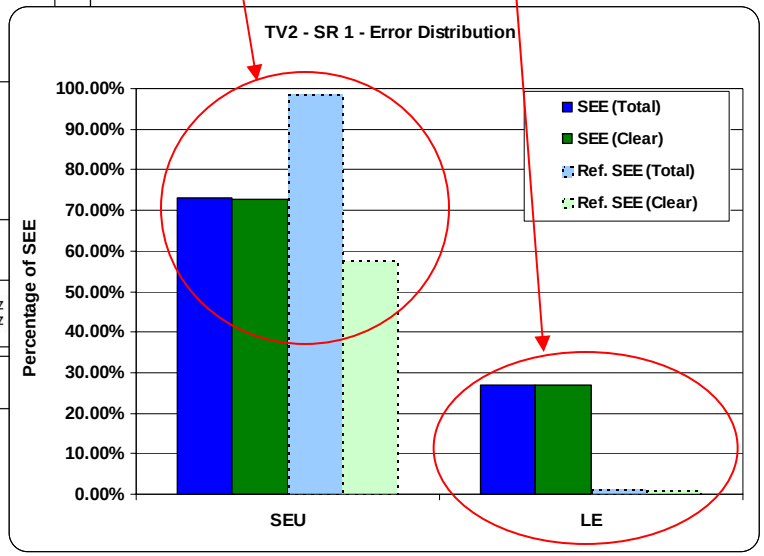
Channel with triplication of sequential cells



SEU Vs. LE ratio

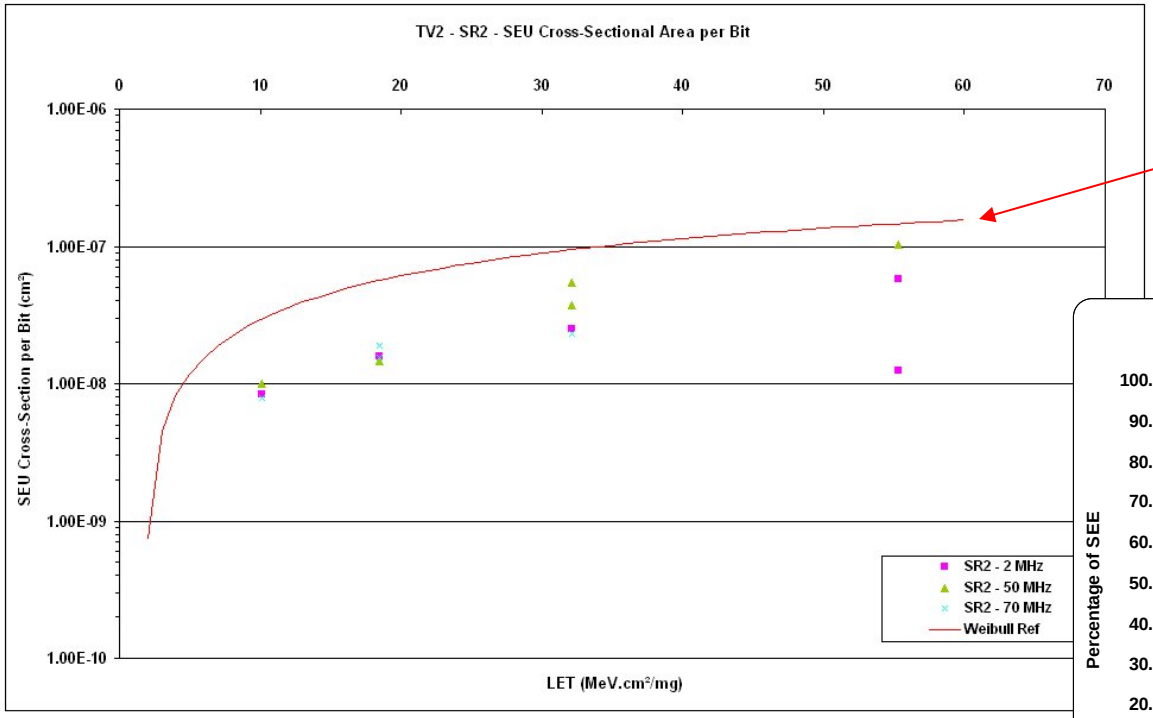
SEU: Clear

LE: Clear

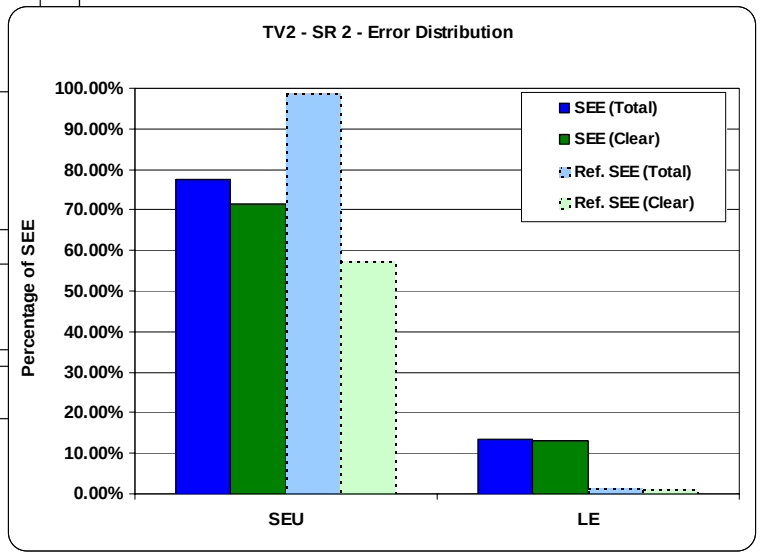


(9/14) - TV2 - SR 2

Channel with triplication of sequential cells and I/O Blocks



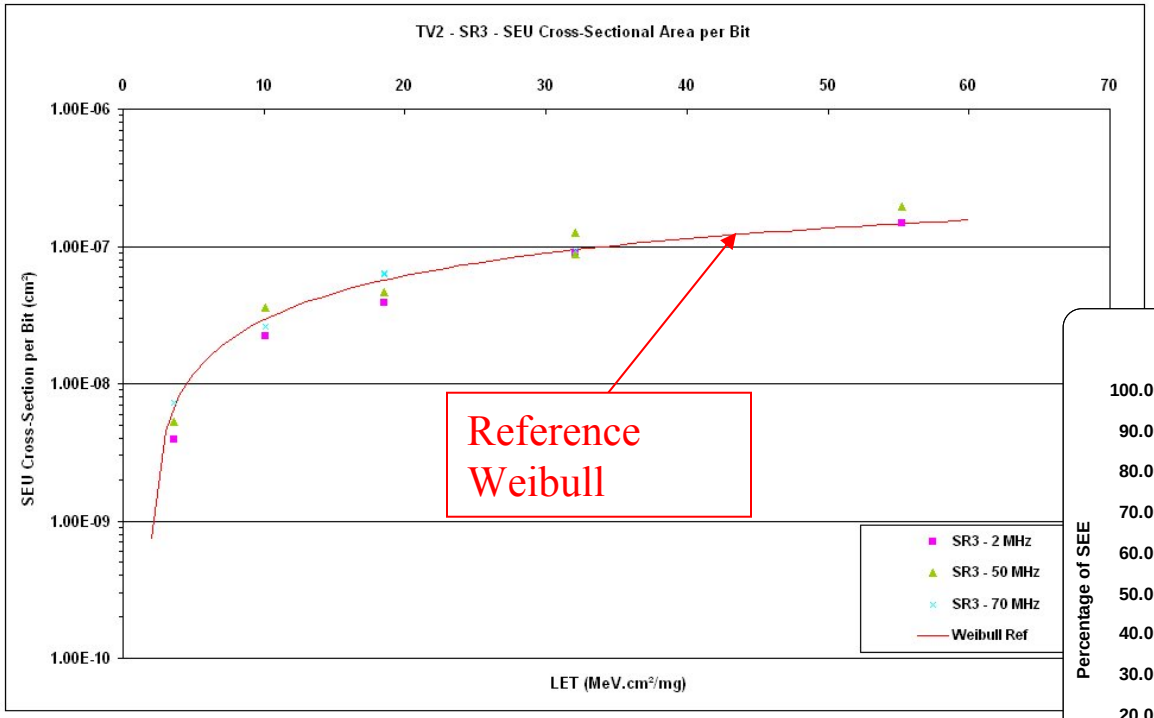
Reference Weibull



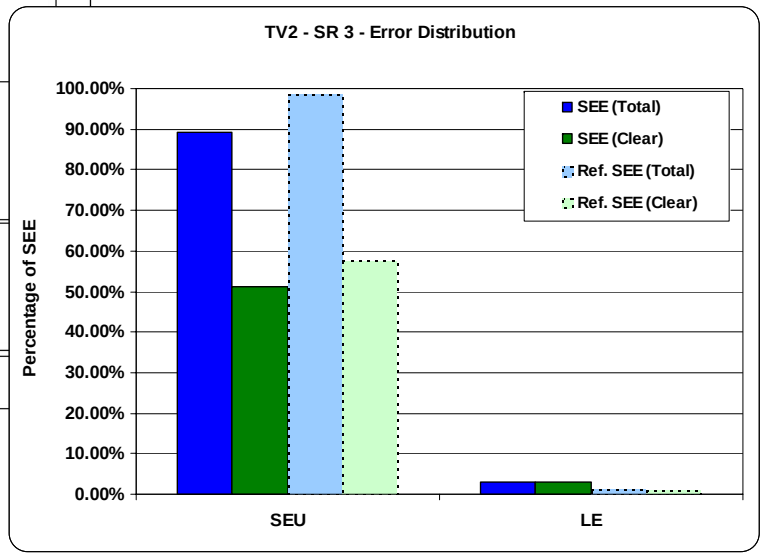
CSsat value under analysis

(10/14) - TV2 - SR 3

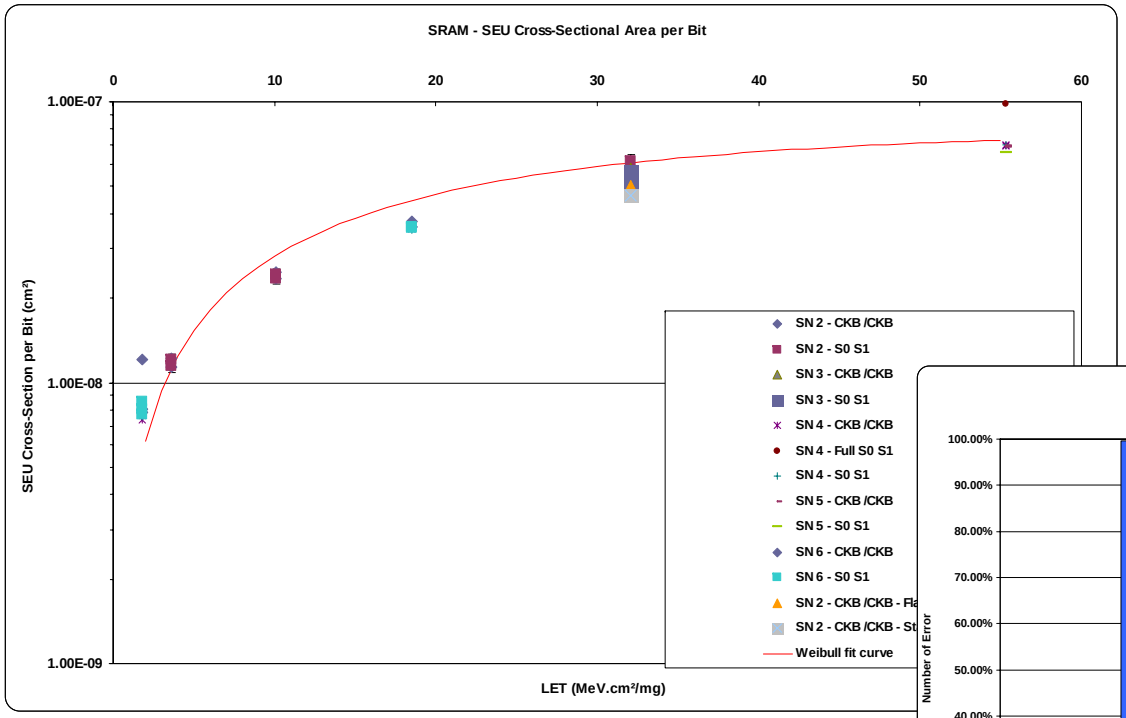
Channel with SET filtering (2 ns)



Very similar

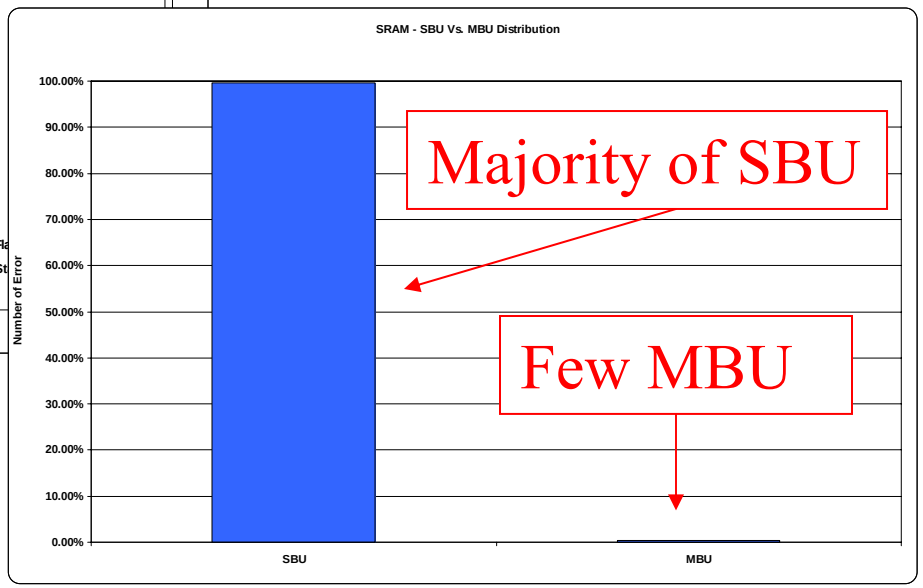


(11/14) - SRAM - HI



Weibull fit parameters:

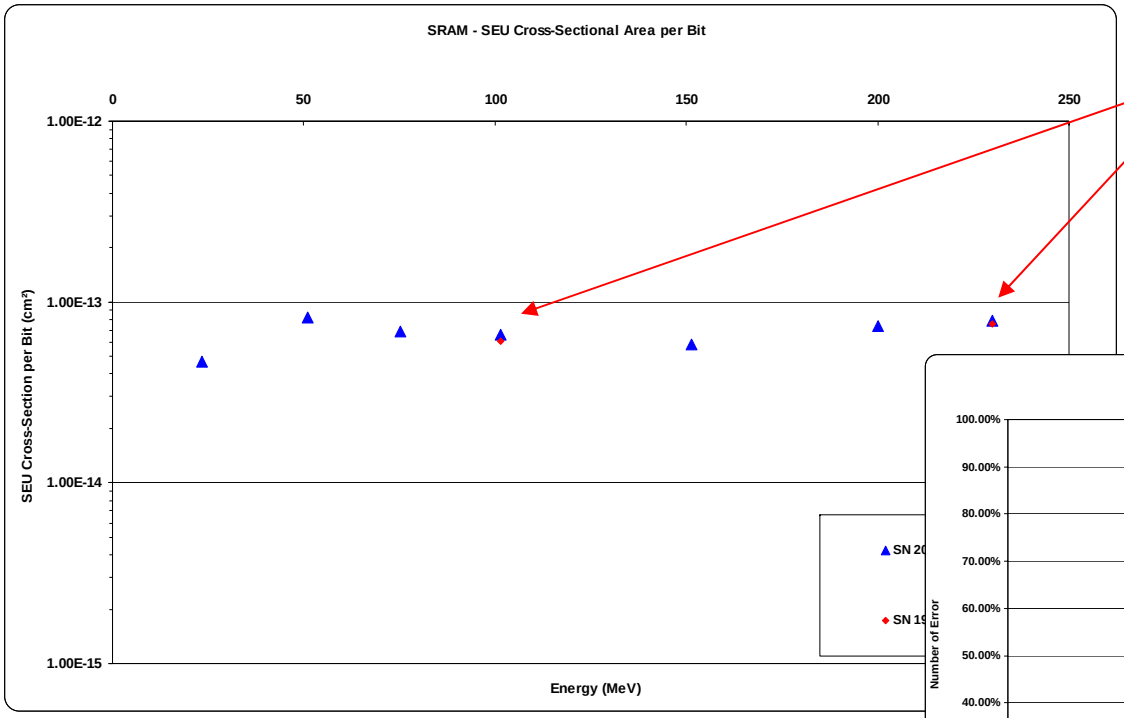
- K = 1
- λ = 22.5
- X_0 = 0.2 MeV.cm²/mg
- **CSsat = 8E-8 cm²**



Only upsets

47 % Set / 53 % Clear

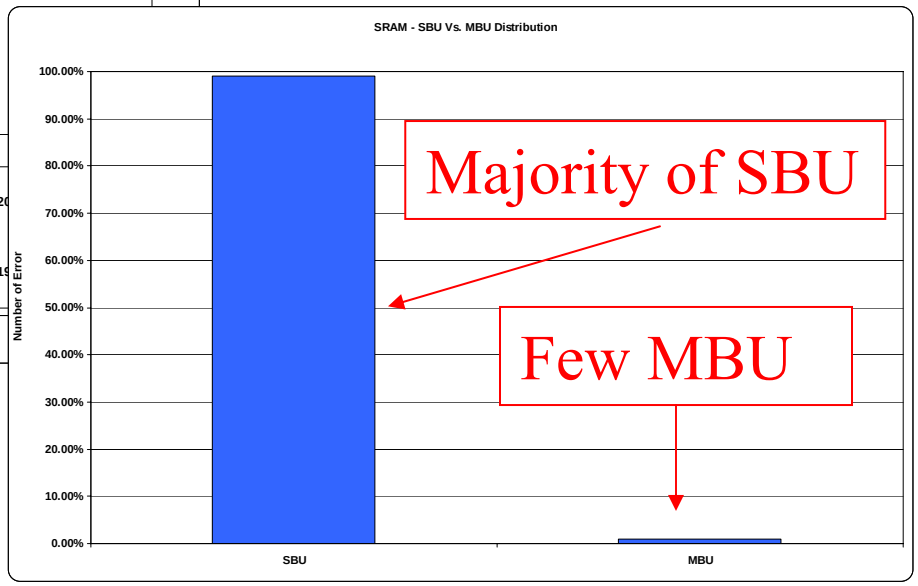
(12/14) - SRAM - Protons



2 Devices tested:

Very similar

CSsat < 1E-13 cm²



Majority of SBU

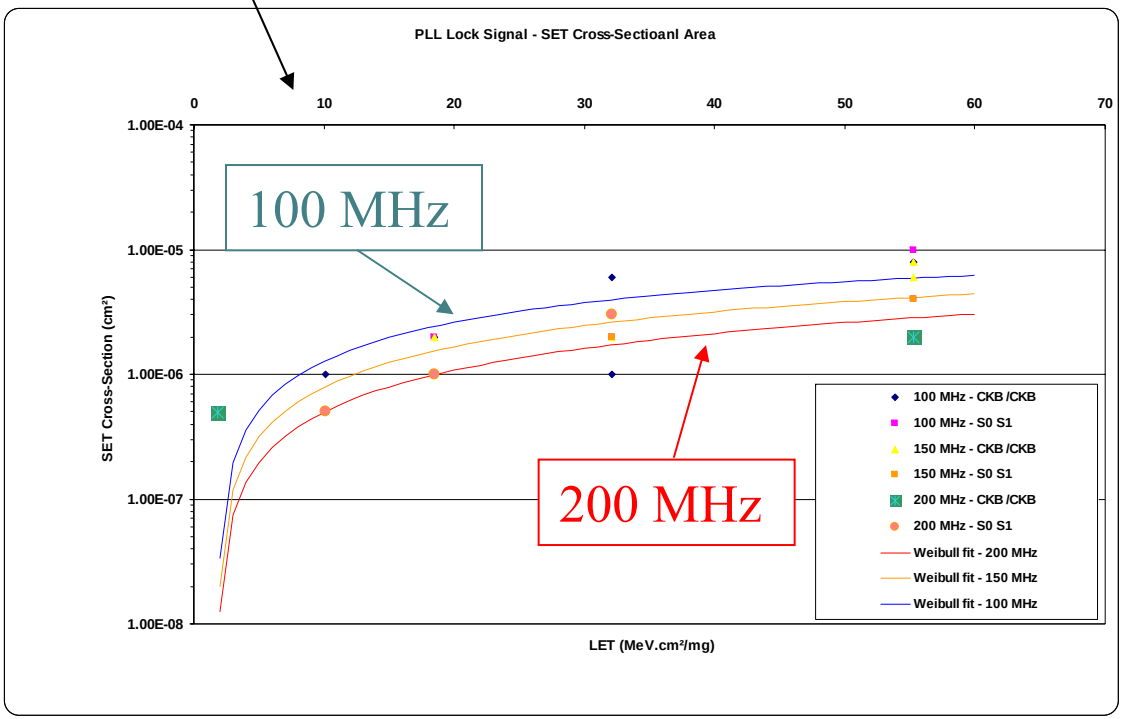
Few MBU

Only upsets

58 % Set / 42 % Clear

(13/14) - PLL

- Output clock is lightly sensitive to SEE
- Lock signal is sensitive to SEE (SEFI, SET)



Weibull fit parameters:

- K = 1
- λ = 60
- X_0 = 1.8 MeV.cm²/mg
- **CSsat = 1E-5 cm²**

The clock output never stopped

(14/14) - SEL & Flash

- **NO SEL**

  Vnom +10%, 125 °C, 55.3 MeV.cm²/mg, 5E6 p/cm²

- **Flash is NOT sensitive** to SEE
  - Configuration and User flash remained intact
- The Flash **programming part** is sensitive to:
  - SEE
  - SHE
  - Cumulated dose deposited by the cumulated fluence

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Conclusion (1/2)

- Irradiation characterization made on:
  - A3PE3000L
  - SEE mitigation methods (flash based FPGA)
- No SEL up to 55.3 MeV.cm²/mg, Vnom +10%, 125°C, 5E6 p/cm²
- Flash is not sensitive to SEE up to 55.3 MeV.cm²/mg
- Registers, SRAM, PLL and Global network

  => sensitive to SEU and SET

  Cross-Sections are established

Conclusion (2/2)

TV	Shift Register	Singularity	SEE Summary
1	1	Reference	SEU (DFF)
	2	Enable C-cells	SEU (DFF) + SET (enable)
	3	Clear C-cells	SEU (DFF) + SET (clear)
	4	C-cells in-between R-cells	SEU (DFF) + SET (C Cells)
	5 to 8	DDR registers	SEU (DFF)
	9 to 10	LVDS buffers	SEU (DFF)
	11 to 14	PLL Clock	SEU (DFF) + Few SEE (PLL)
2	1	R Cells TMR	Few SEU (DFF)
	2	R Cells + I/O TMR	Under analysis
	3	SET Filtering	SEU (DFF)
	4	R Cells + I/O TMR + SET Filtering	Φ
	5	R Cells + I/O TMR + C Cells duplication	Φ
	6	Full TMR	Φ

Final report estimated for June 2011

THANK YOU!

Any question?