

IRRADIATION CHARACTERIZATION OF DDR2 AND SDR - SDRAM

F.X. Guerre, M. Mazurek and M. Grandjean Hirex Engineering





DDR2 - SDRAM HEAVY IONS IRRADIATION CHARACTERIZATION FEASIBILITY

ESA PO - 13528/99/NL/MV COO-22 dated from 29/09/2008

Report: HRX/SEE/0258 issue 02 dated from December 2009

M. Grandjean, F.X. Guerre, Hirex Engineering



Summary



- □ Background and Objectives
- □ Devices overview
- □ Test conditions
- □ Test set-up
- □ Irradiation characterization results
- □ Conclusion

Background and Objectives



□ 2007 - Hirex built a new tester

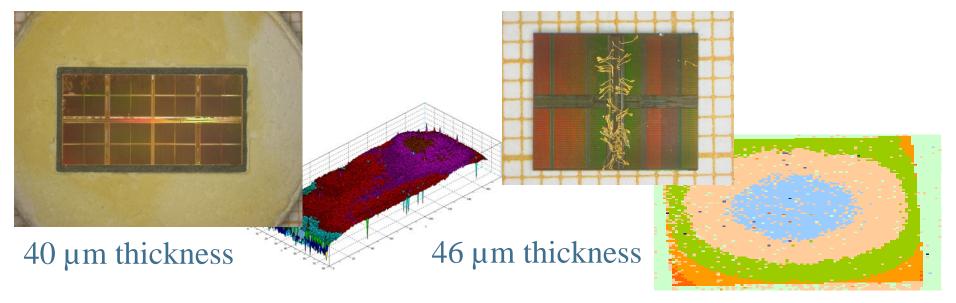
- □ 512 MB DDR2-SDRAM previously tested
 - Compare data
- □ 1 GB DDR2-SDRAM test feasibility
 - Find and validate technical solutions to:
 - Open and thinned the samples
 - Samples soldering
 - Test different references

Keeping the functionality

Device overview



	EDE1108AB	MT47H64M8
Manufacturer	ELPIDA	MICRON
Part description	1 GB DDR2-SDRAM	512 MB DDR2-SDRAM
Package	FBGA-68	FBGA-60
Marking	E1108AB-5C-E 06500W057	48R9 / 6YD22 / D9GMH
Die dimensions	16.9 x 8.7 mm	8.5 x 7.0 mm



ESA - Microelectronics Presentation Days

March 28th and 29th 2011

Test conditions



- □ TAMU (College Station, TX, USA)
 - November 2008
- ☐ HIF (Louvain-La-Neuve, Belgium)
 - May 2009
- □ SEL, SEFI, SEU, SET
- □ 1.8 V / 0.9 Vref / Room Temp / CKB
- □ Dynamic and static tests

Test set-up (1/2)



- □ Software:
 - JEDEC Standard DDR2-SDRAM Specification, JESD79-2E, April 2008
 - Specific algorithms
 - Fill / Check
 - Error SEFI classification
 - Several test sequences
 - Fill / expose / check ...
 - Initialize / fill / expose / check ...
 - Initialize / fill / expose / initialize / check ...

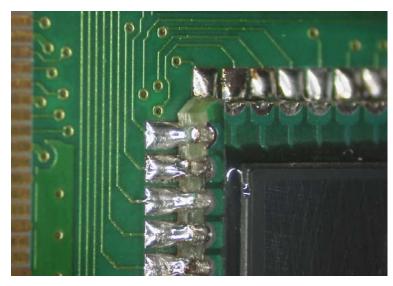
8/20

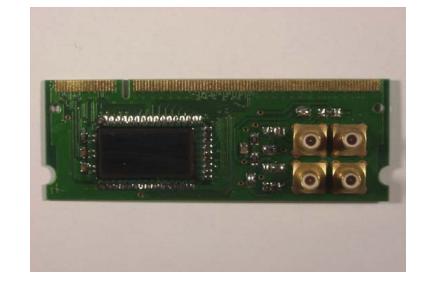
Test set-up (2/2)



□ Hardware

- Samples soldered on stamp board (underfill)
- Samples then opened and thinned (40 µm)
- Stamp board reported on SO-DIMM 200





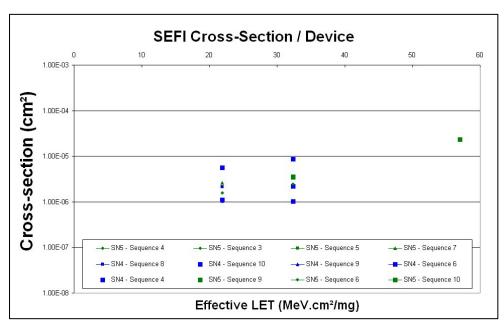
ESA - Microelectronics Presentation Days

March 28th and 29th 2011

Results (1/3)



- □ No SEL @ 32.4 MeV.cm²/mg, 1E7 p/cm², 1.8 V, room temp
- □ SEFI (2 types: Soft and Hard)
 - @ LET 57 MeV.cm 2 /mg => SEFI CSsat / device < 3E-5 cm 2
- □ Row errors
 8191 (0x1FFF),
 16383 (0x3FFF)
 highly sensitive
- □ Leaky cells

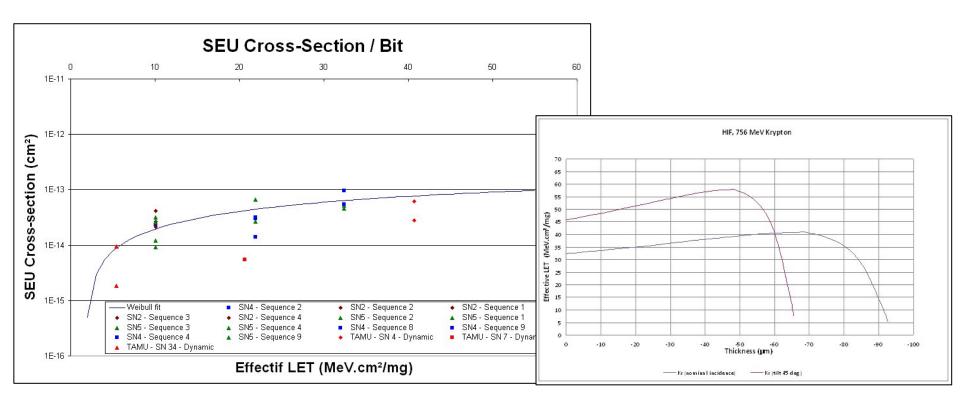


Results (2/3)



10/20

\square SEU @ LET 40.7 MeV.cm²/mg => SEU CSsat / bit < 2E-13 cm²



Calculated with SRIM 2008

Results (3/3)



□ SEU specificities:

- The four word positions on the burst are not similarly sensitive to errors
- Almost all SEU are Single Bit Upset (SBU)
- Clear transitions are twice set transitions
- The bit position distribution is well balanced inside the word

Conclusion (1/2)



- □ ELPIDA 1 GB and MICRON 512 MB DDR2-SDRAM were heavy ions tested
- □ No SEL @ 32.4 MeV.cm²/mg, 1E7 p/cm², 1.8 V, room temp
- □ 2 types of SEFI (Soft, Hard)
 - @ LET 57 MeV.cm 2 /mg => SEFI CSsat / device < 3E-5 cm 2
- □ Row Errors, Leaky cells
- □ SEU
 - @ LET $40.7 \text{ MeV.cm}^2/\text{mg} => \text{SEU CSsat} / \text{bit} < 2\text{E}-13 \text{ cm}^2$

Conclusion (2/2)



- Results are homogeneous
- Characterization of large DDR2-SDRAM is feasible
- □ Specific Device Interface Boards (DIBs) Sample + Stamp board + SO-DIMM 200
- □ Initialization of the device before each write/read processes

Re-Initialization of device's registers



SDR - SDRAM HEAVY IONS IRRADIATION CHARACTERIZATION

ESA contract - No 22327/09/NL/SFE dated from 15/10/2009

Report: HRX/SEE/0287 issue 03 dated from June 2010 M. Mazurek, F.X. Guerre, Hirex Engineering



Background and Objectives



- □ 256 MB SDR-SDRAM (HITACHI)
- Previous SEL tests were performed on samples not fully functional (opening and thinning)

October 2009, SEE Report: HRX/SEE/0276

- Verification and confirmation of SEL results
- oAdd SEFI and SEU data

Device overview

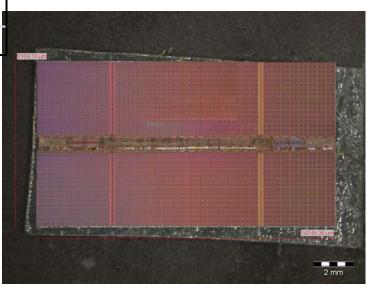


16/20

Part description	256 Mbit SDR-SDRAM	256 Mbit SDR-SDRAM
Provider	Astrium	Oxygen
Package	4-pin TSOP II	4-pin TSOP II
Samples used	SN 516, SN 525, SN 526	SN 1
Package marking	225165BTT75	225165BTT75
Die dimensions	8.0 x 14.5 mm	8.0 x 14.5 mm
Date code	232	423

= 60-70 = 50-60 = 40-50 = 30-40 = 20-30 = 10-20 = 0-10

HM5225165 HITACHI



ESA - Microelectronics Presentation Days

March 28th and 29th 2011

Test conditions



- RADEF (Jyväskylä, Finland)
 - December 2009
- □ SEL, SEFI, SEU
- \Box 3.6 V (Vnom + 10%)
- □ Temperature: room, 50 and 85 °C
- Checkerboard
- □ Auto-refresh mode (variable refresh rate)
- □ Test sequence:
 - Initialize / fill / expose / check / fill / expose ...

Results



```
□ SEL: Tilt 0 ° - LET surface # 55 MeV.cm²/mg

room temp: No SEL

50 °C, 85 °C: SEL CSsat / die = 1E-7 cm²

Tilt 30 ° - LET surface # 64 MeV.cm²/mg

50 °C: SEL CSsat / die # 3E-7 cm²

85 °C: SEL CSsat / die # 4E-5 cm²
```

- □ SEFI (3 types: 2 Softs x 200, 1 Hard x 1600)
 - @ LET 60 MeV.cm 2 /mg => SEFI CSsat / device < 2E-4 cm 2
- □ LE (row, col) and SEU (upset, MBU 5x SBU)
 - @ LET 60 MeV.cm 2 /mg CSsat / bit= 1.4E-9 cm 2

- 256 MB SDR-SDRAM (HITACHI) was heavy ions tested
- □ SEL Tilt 0 ° LET surface # 55 MeV.cm²/mg
 room temp: No SEL
 50 °C, 85 °C: SEL CSsat / die = 1E-7 cm²
 Tilt 30 ° LET surface # 64 MeV.cm²/mg
 50 °C: SEL CSsat / die # 3E-7 cm²
 85 °C: SEL CSsat / die # 4E-5 cm²
- SEFI (Mainly hard, some 2 types soft)
- □ LE (row and col), SEU (upsets, MBU 5x SBU)

THANK YOU!

Any question?