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Studies of Radiation SEE Effects in NAND-Flash and DDR Types of memories

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R&D Final Presentation Days
March, 28-29, 2011, ESTEC, Nordwijk

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Topics

1. **8-Gbit NAND-Flash** (4k Blocks x 64 Pages x 4k byte x 8 bit)
   Samsung K9WBG08U1M, datecode: 3708,
   Micron MT29F8G08AAA-WP, datecode: 4208

   - **Angular Dependence of the Static SEU Cross Section**

2. **2-Gbit DDR2 SDRAM** (8 Banks x 32k rows x 256 columns x 4x8 bit)
   Micron MT47H256M8HG-37E, datecode: 0742,
   Elpida EDE2108ABSE-8G-E, datecode: 0811

   - **Thinning of DDR2 dies (300 ... 200 µm → 80 ... 60 µm)**
   - **SEU- and SEFI-Cross Section @ 125 MHz with DLL on**

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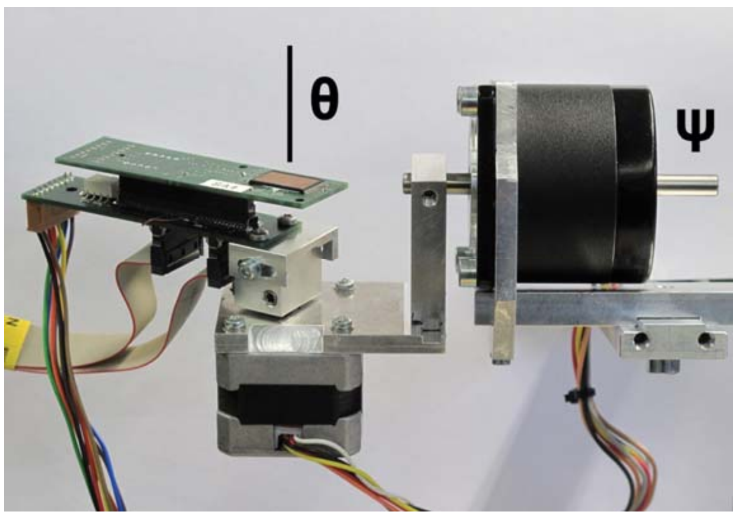
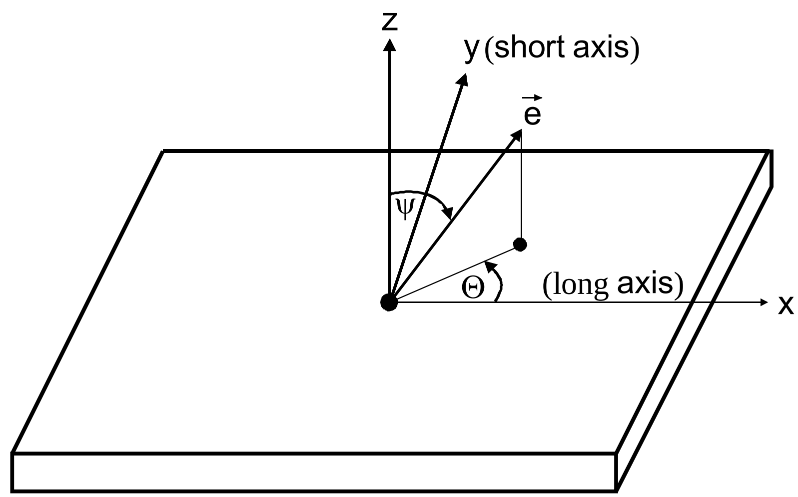
Angular Dependence of the NAND-Flash SEU Cross Section

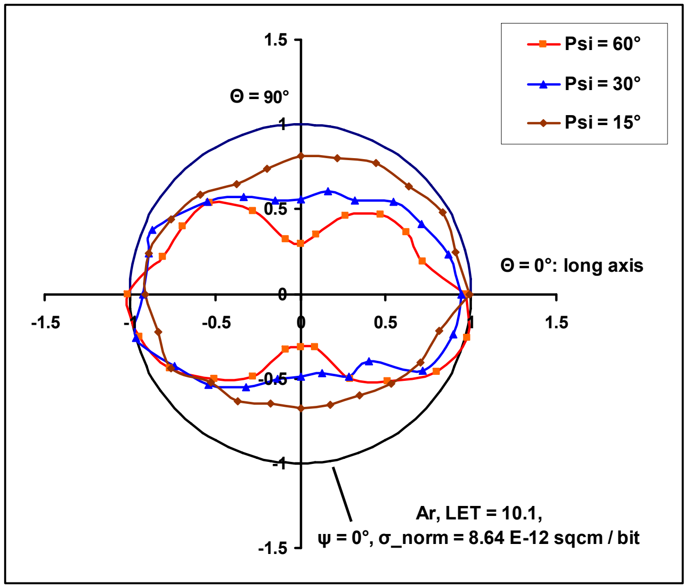
Motivation:
Previous Heavy Ion tests exhibited substantially different SEU Cross Sections for 60° tilting around the long (x) and the short (y) die axis.

To sample the whole hemisphere a set up was implemented for DUT tilting around two orthogonal axes (azimuth angle θ: 0° – 360°, elevation angle ψ: 0° – 90°).

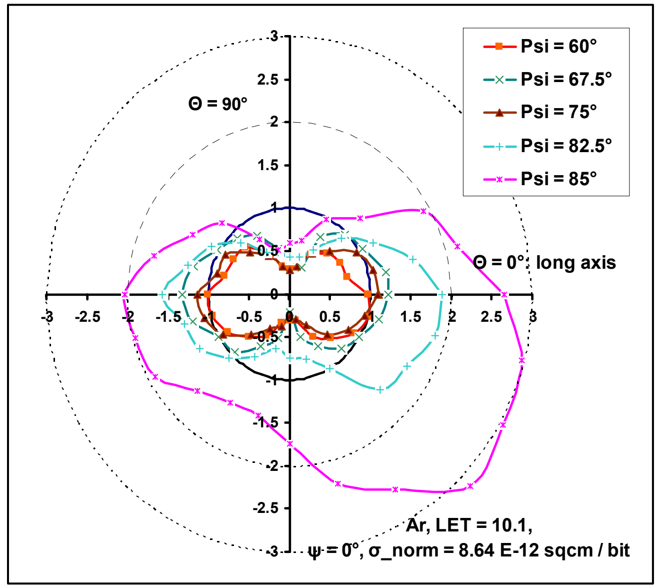




Angular Dependence of the NAND-Flash Static SEU Cross Section, Micron



Normalized SEU cross section, ψ ≤ 60°, Micron DUT

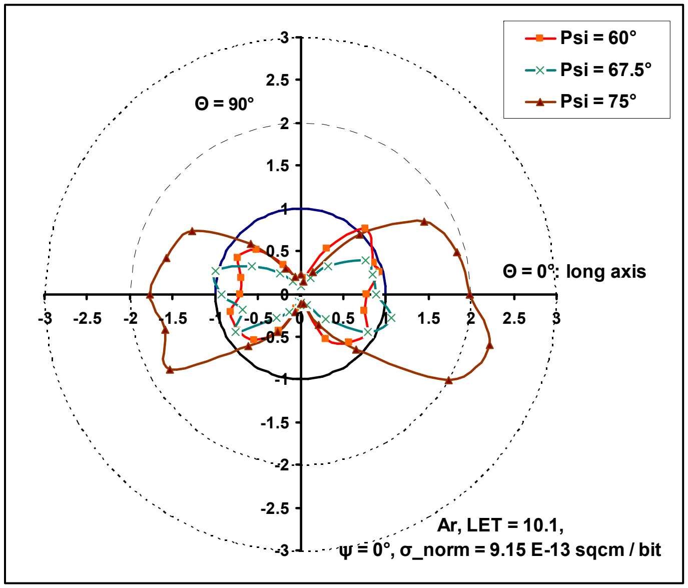


Normalized SEU cross section, ψ ≥ 60°, Micron DUT

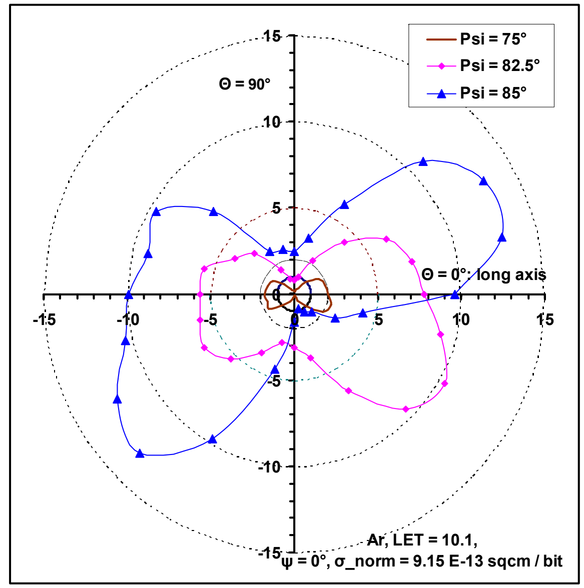
- With increasing elevation angle (ψ), the polar diagram develops a dipole shape with a deep notch at Θ = 90° and Θ = 270°, i.e. for ion incidence along the short axis of the die. It remains within the normal incidence circle.
- For ψ ≥ 60°, the dipole shape remains, but the cross section increases along the long axis of the die (Θ = 0° and Θ = 180°), and exceeds the normal incidence circle by up to a factor of three.

Angular Dependence of the NAND-Flash Static SEU Cross Section, Samsung

ψ < 60°
not measured



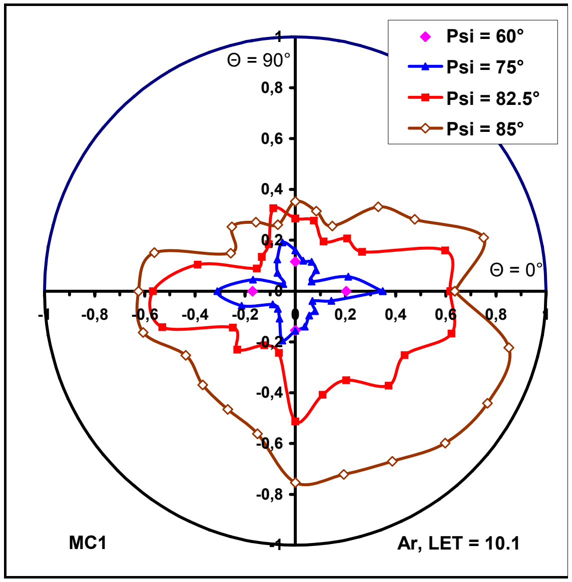
Normalized SEU cross section,
ψ = 60°..75°, Samsung DUT



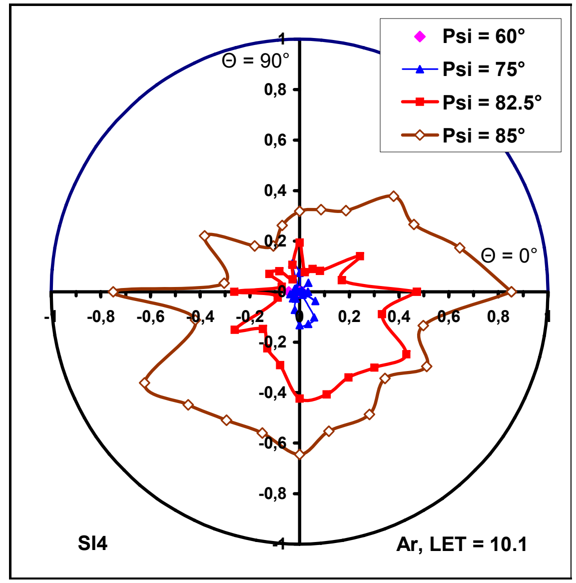
Normalized SEU cross section,
ψ ≥ 75°, Samsung DUT

- The polar diagrams of the Samsung device are qualitatively similar, but σ_norm = 9.15E-13 < 8.64E-12 (Micron)
- The tilt effect is much more significant. At grazing incidence, along the long axis of the die, the SEU cross section increases by more than a factor of ten.

Angular Dependence of the NAND-Flash Static MBU Cross Section



MBU to SEU ratio, Micron DUT



MBU to SEU ratio, Samsung DUT

- MBU (= Multi Bit Upset) clusters are defined by error address distances ≤ 6 in row and/or column direction.
- At normal incidence, the MBU/SEU ratio is less than 2%. It remains < 20% until ψ = 60° (Micron) and ψ = 75° (Samsung). At larger elevation angles (ψ = 85°), the MBU/SEU ratio explodes up to about 80%.

MBU Features common to the Samsung and Micron Device

(i) All MBUs are 0 → 1 falsifications (= charge loss).

(ii) Always only one bit per byte was corrupted.

(iii) At $\psi \leq 45°$ nearly no MBUs occurred.
At $\psi \geq 60°$ the MBU percentage off all SEUs rises steeply.

(iv) Only very few MBUs show corrupted bits over more than 4 columns / more than 4 pages.
MBU classification according to the column distance: D-1 … D-5.

MBU Features differing to the Samsung and Micron Device

(i) Samsung: Page Distance 1, 2, 3, (≥ 4 very rare)

Column Distance: 1, 3 or 5

Mostly D-3 and D-5 MBUs.

D-1 MBUs only for incidence along the short die axes.

Potential explanation: Even and odd columns are physically separated.

Micron: In contrast both, even and odd page, and even and odd column distances.

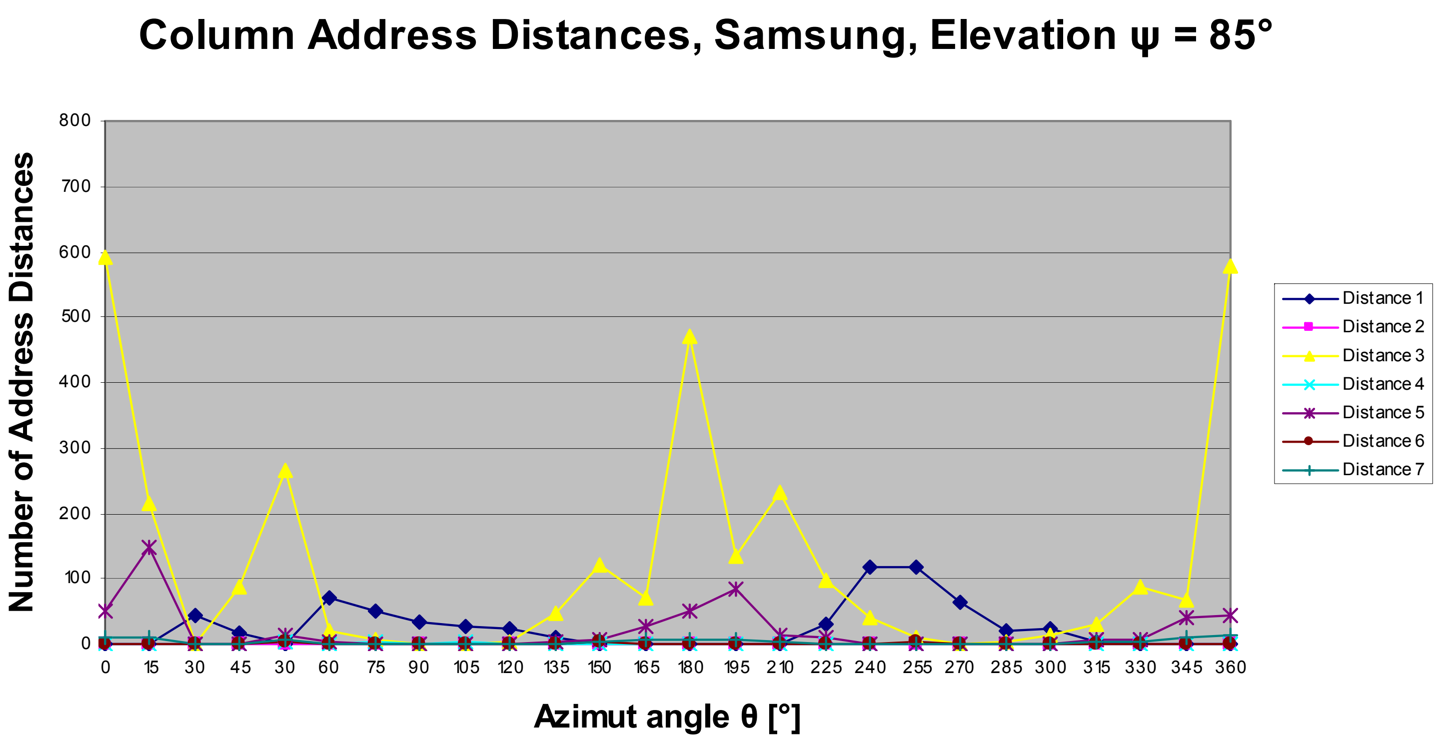
Mostly D-1 MBUs.

(ii) The average omnidirectional SEU cross section $\sigma_{4\pi}$ has been calculated and has been compared to the cross section $\sigma_{0,0}$ at normal incidence:

Samsung: $\sigma_{4\pi} / \sigma_{0,0} = 2.1$ @ LET = 10.1

Micron: $\sigma_{4\pi} / \sigma_{0,0} = 0.8$ @ LET = 10.1

Angular Dependence of MBU Address Distances



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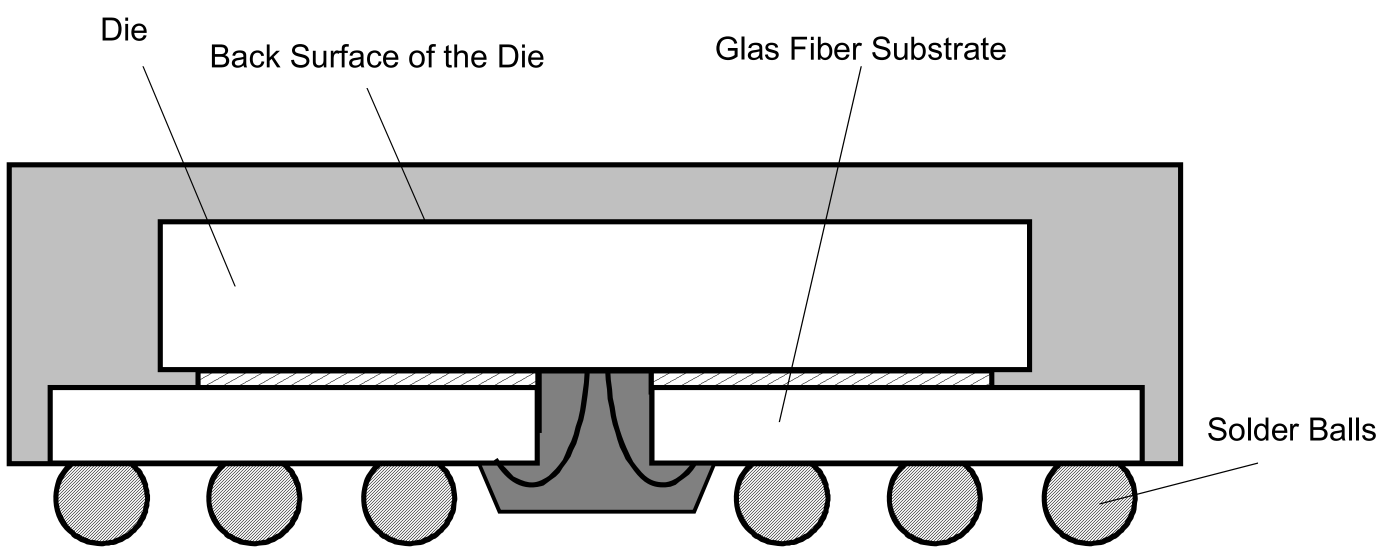
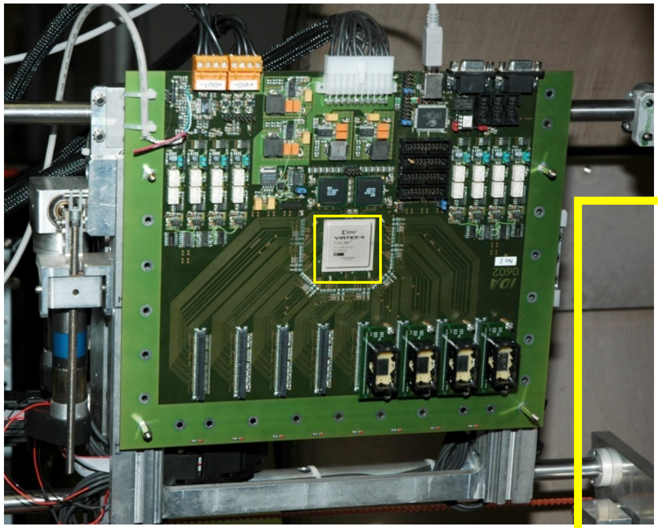
DUT Preparation

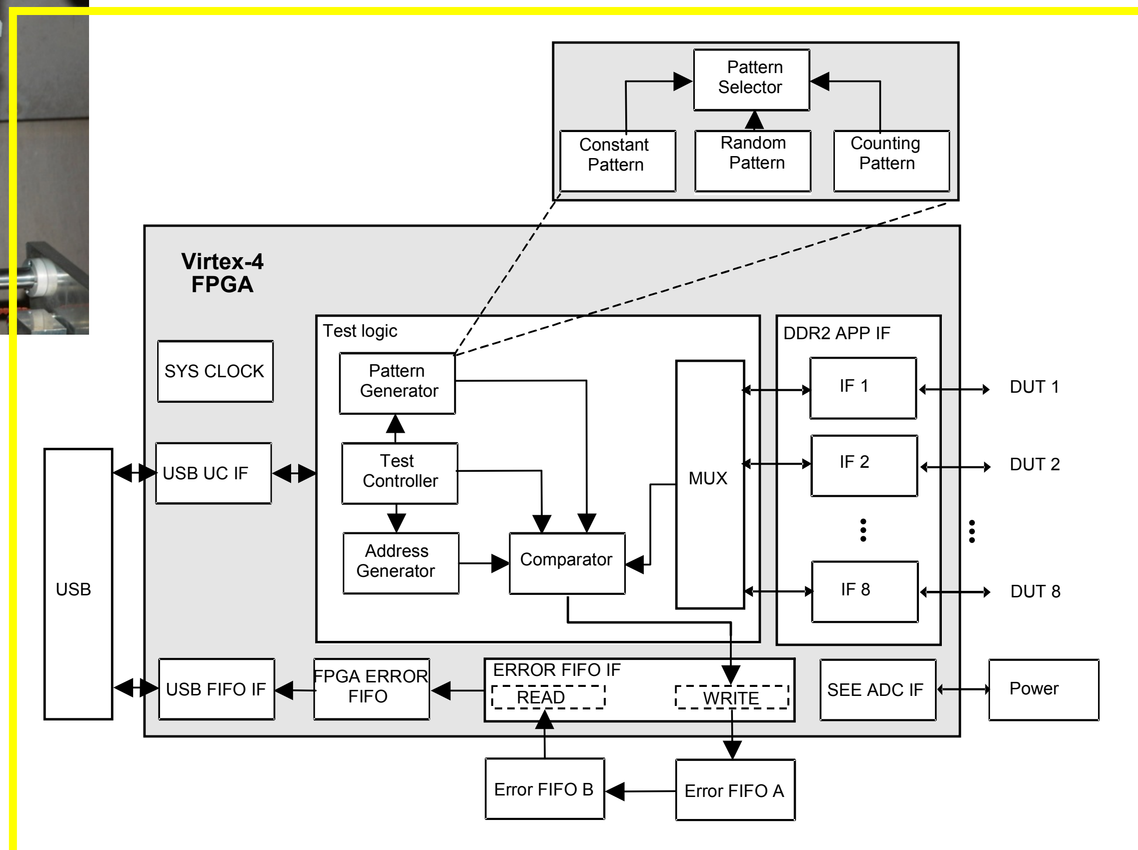
- DDR2-SDRAM and DDR3-SDRAM in FBGA-Package
- die thickness between 180 µm and 350 µm
  penetration of ion beams is about 90 µm at LET = 30
  => backside thinning down to 60 – 70 µm
- etching of the plastic surface at 70°C with HNO3
- sampling of the die curvature
- grinding of the die with steps of about 20 µm along the die curvature
- monitoring of the applied forces



DDR2 SDRAM Test Set Up Architecture

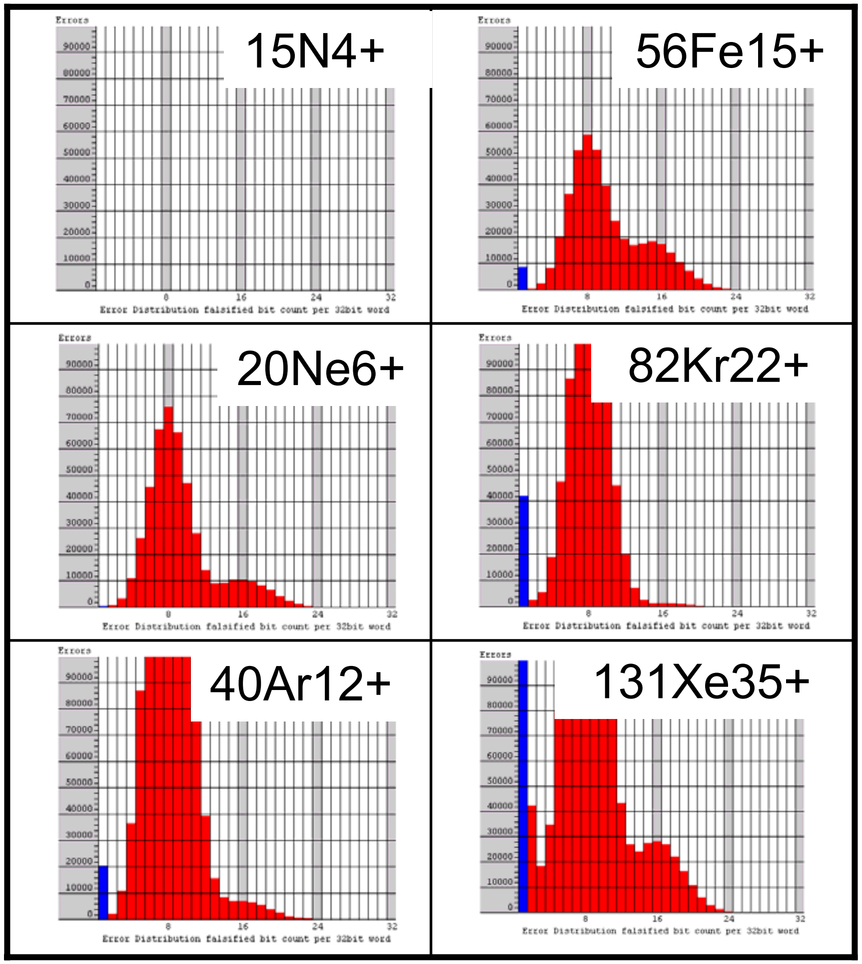


- DDR3 Test Bed ready for use in June 2011

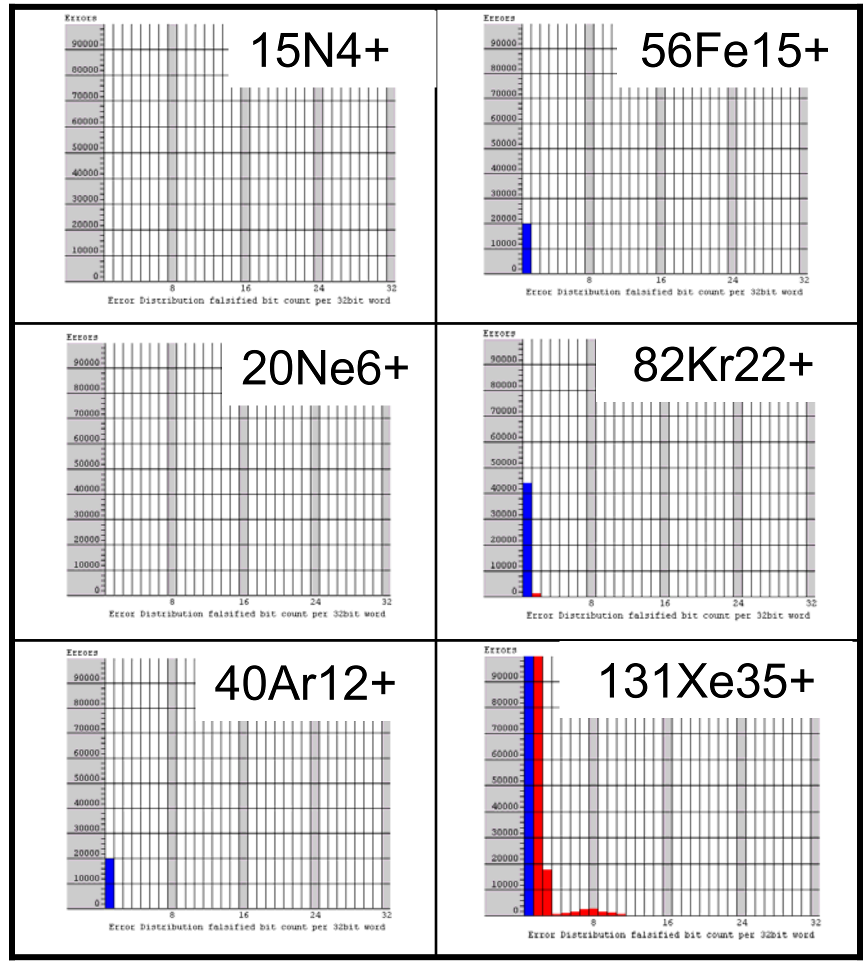


Error Distribution in Read Mode M1a, 4-Byte Burst

No initialisation

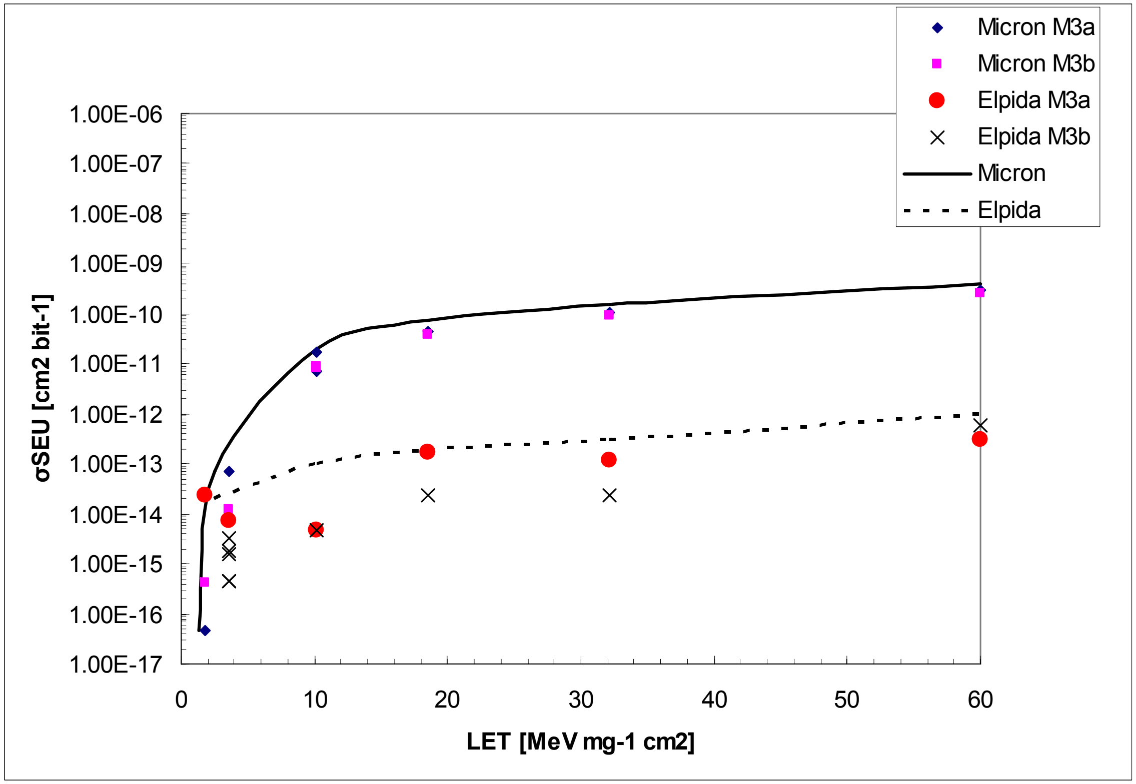


Short initialisation



- Frequent initialisation reduces significantly the count of SEFI related errors.

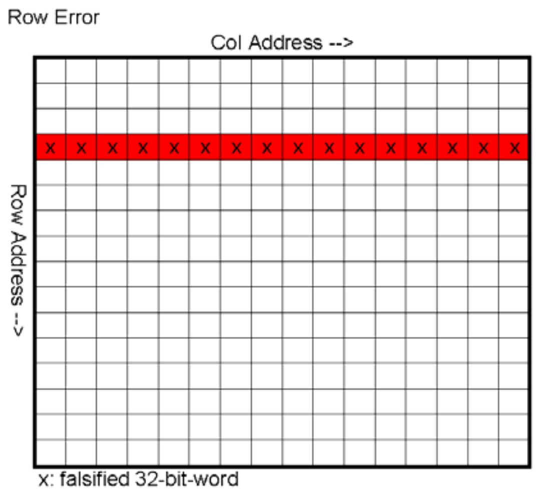
Cross section of single bit errors in Storage Mode M3

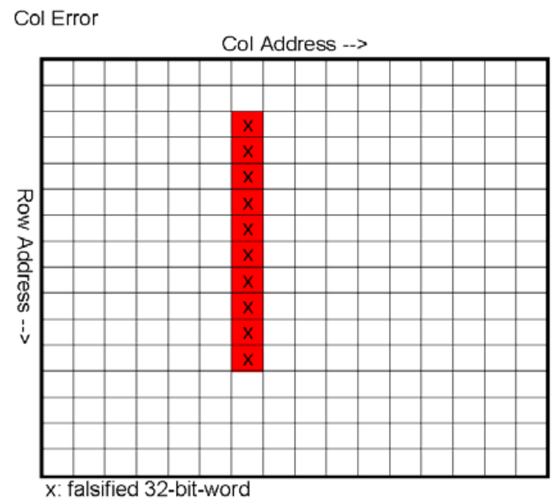


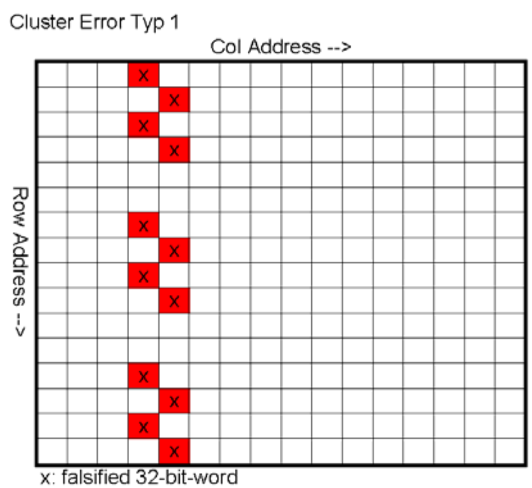
- a/b: without/with short initialisation

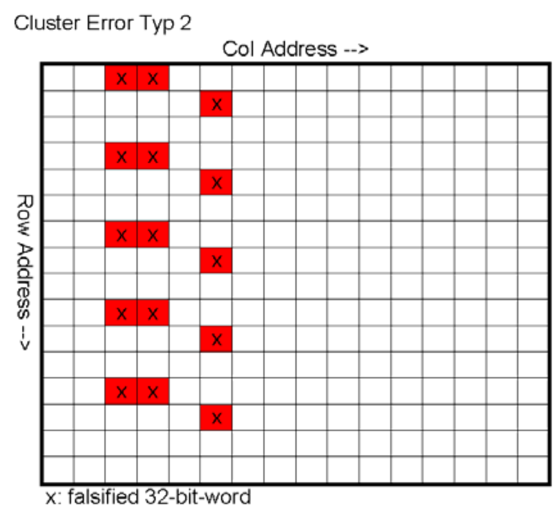
- Elpida shows a substantial lower Cross Section
- Cross Sections of Storage Mode (M3 a/b), Read Mode (M1 a/b) and Marching Mode (M2 a/b) are nearly identical
- also in M1 and M2 nearly all SEUs are static

Example of DDR2 SEFI types

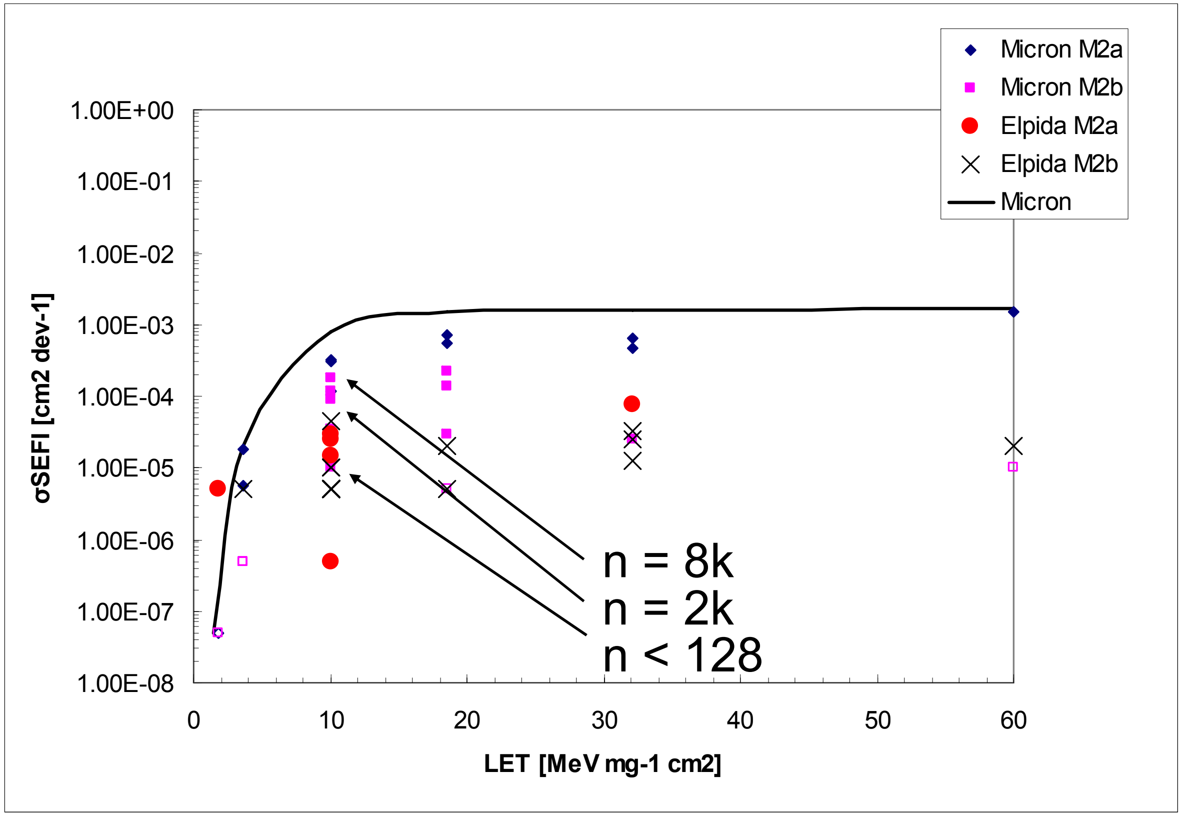








Transient SEFI Cross Section in Marching Mode M2



- a/b: without/with short initialisation, in M2 every n rows

- Transient SEFIs are for example Page Errors or Column Errors
- short initialisation improves the cross section substantially

Publications and Acknowledgements

Publications

[1] H. Schmidt et al., "TID and SEE Tests of an Advanced 8 Gbit NAND-Flash Memory", NSREC 2008 Data Workshop

[2] H. Schmidt et al.,"TID Test of an 8-Gbit NAND Flash Memory", IEEE Trans. Nuclear Science, Vol. 56, Nr. 4, August 2009

[3] L.Li et al., "Heavy Ion SEE Test of an Advanced DDR2 SDRAM", TUZ Conference Proceedings, 2009, Bremen

[4] K. Grürmann et al., "SEU und MBU Angular Dependence of Samsung and Micron 8-Gbit SLC NAND-Flash Memories under Heavy-Ion Irradiation", accepted for NSREC 2011 Data Workshop

Acknowledgements

We would like to thank Reno Harboe-Sørensen and Véronique Ferlet-Cavrois for their support and for their understanding of the imperfections associated with real work.

Further we thank the technical staff of RADEF, PIF-PSI and CASE for their excellent support and Daniel Peyre, formerly with Astrium France, for refreshing discussions.