RADIATION ASSESSMENT OF DEEP SUBMICRON CMOS PROCESSES

Contract No. 22485/85/09/NL/PA

CNES – QEC final presentation day

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PROJECT STRUCTURE

- Activity 1
  - Report on Imec's 65 nm technology
- Activity 2
  - Study Hardness Multi-Gate Devices
  - Study Hardness High-κ/Metal Gate Devices
  - Study Hardness High-Mobility Devices
- Duration : 24 months, starting June 8, 2009

PROTON RADIATION ASSESSMENT OF IMEC'S FINFET TECHNOLOGY WITH DIFFERENT STRAIN ENGINEERING APPROACHES

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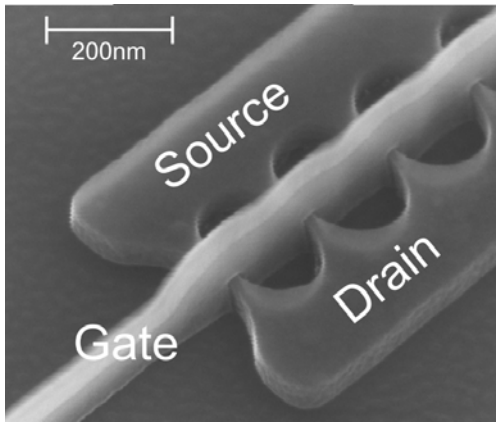
OUTLINE

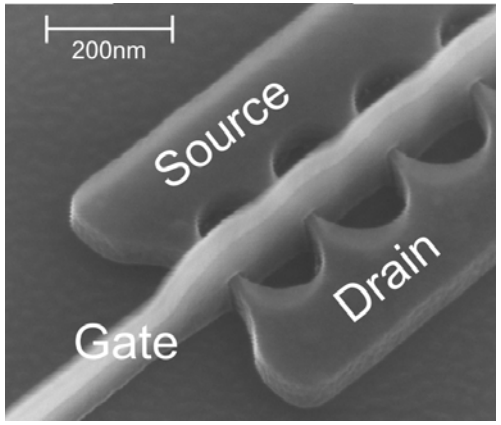
- Introduction: aim and motivation
- Technological, radiation and measurement details
- Results
  - Pre-rad
  - Post-rad
- Conclusions

INTRODUCTION



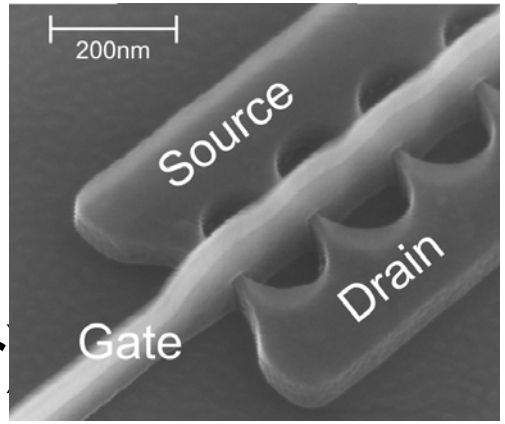
- FinFETs are good candidates for implementation in sub-22 nm CMOS applications.
- Strain engineering boosts the device performance (I_{on} vs I_{off}).
- What about the radiation tolerance?

INTRODUCTION



- From literature, for FinFETs on Silicon-on-Insulator (SOI) substrates, beneficial Single-Event Effects are expected but Total Ionizing Dose (TID) degradation because of the buried oxide and interface coupling.
- For narrow devices, the impact of the BOX should reduce because of the better electrostatic control by the front-gate.
- However, TID and heavy-ion damage has been observed in our tri-gate MuGFETs !!!

PROCESS SPLITS

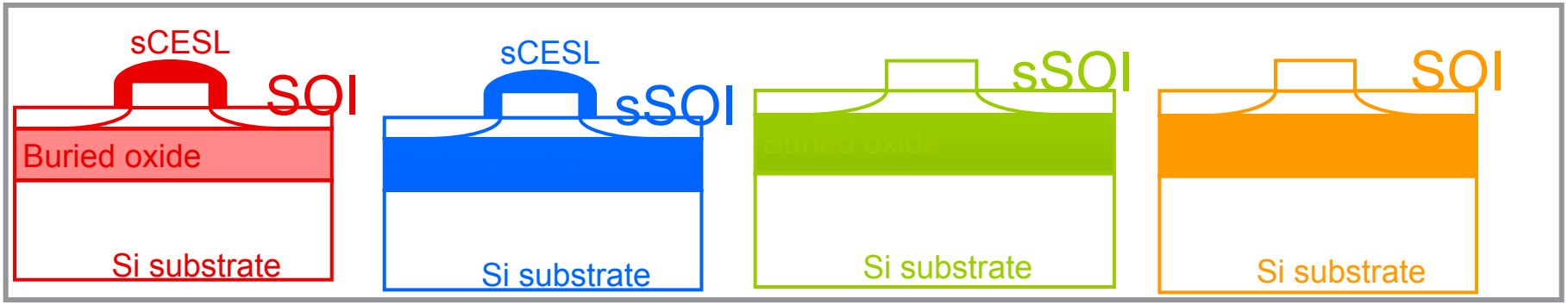


Wafer D12: SOI + SEG (reference wafer)

Wafer D13: SOI + SEG + CESL

Wafer D20: sSOI + SEG

Wafer D21: sSOI + SEG + CESL



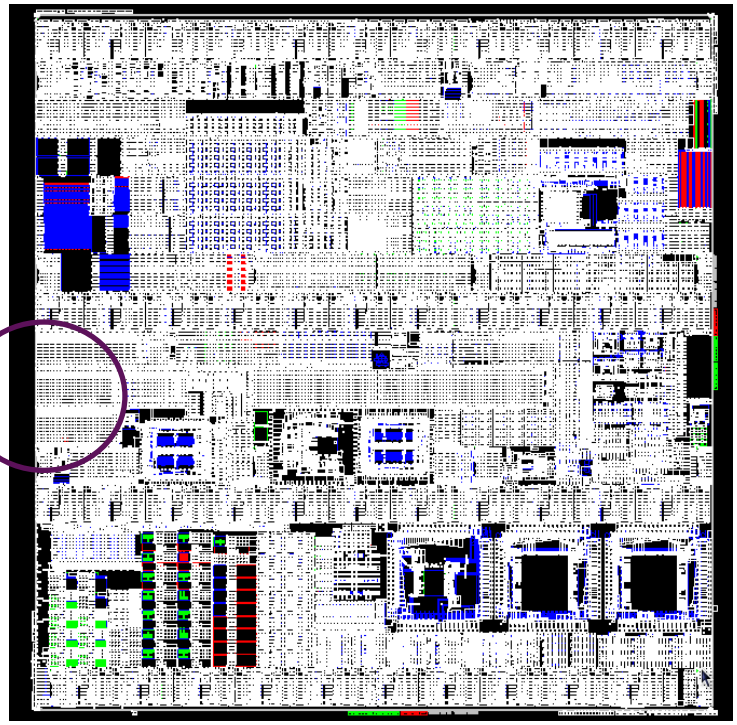
MASK LAY OUT: RHYTHM

n- and pMOSFETs with:

W=20 nm and L=50, 80, 150, 400 and 900 nm

L=150 nm and W=20, 40 120, 370 and 870 nm

H_{fin}=65 nm



For N=5 fins, the width is given by $W=5x(2xH_{fin}+W_{fin})$

MEASUREMENTS

Input I_D-V_G characteristics nMOS

V_G=-1.2-->1.2 V, step 10 mV
V_D=50 mV, 0.8 V and 1.2 V
V_B=-20 V, 0 V, 20 V

Output I_D-V_D characteristics nMOS

V_D=0-->1.2 V, step 25 mV
V_G=0.25-->1 V, step 0.25 V

Input I_D-V_G characteristics pMOS

V_G=1.2-->-1.2 V, step -10 mV
V_D=-50 mV, -0.8 V and -1.2 V
V_B=20 V, 0 V, -20 V

Output I_D-V_D characteristics pMOS

V_D=0-->-1.2 V, step -25 mV
V_G=-0.25-->-1 V, step -0.25 V

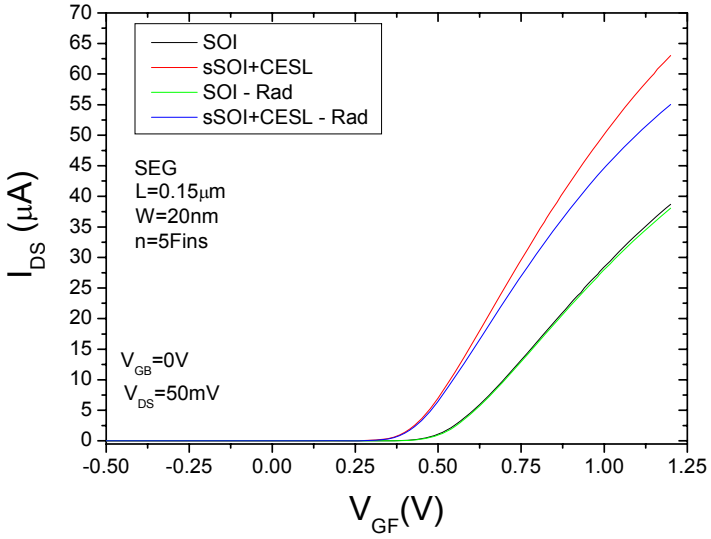
PARAMETERS EXTRACTED

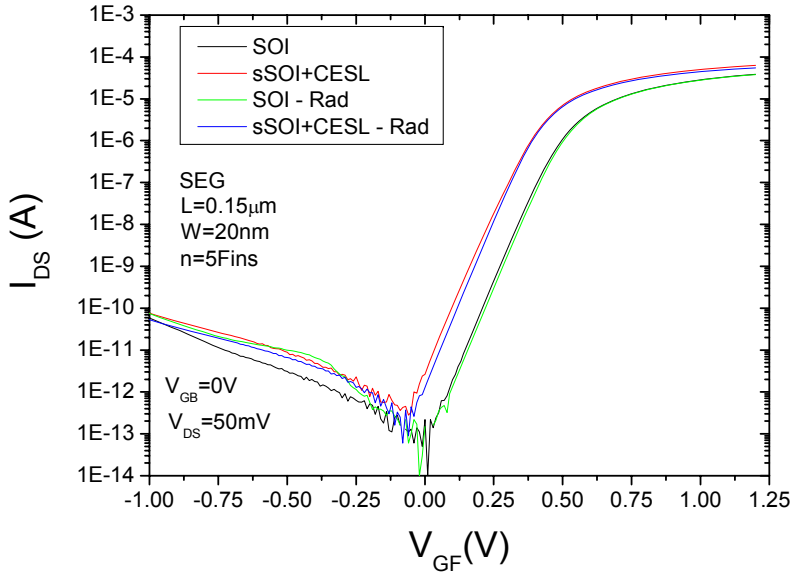
- The threshold voltage (V_{Tlin}) in linear operation through the Y function method by linear extrapolation.
- The threshold voltage in saturation (V_{Tsat}) at V_D=1.2 V or -1.2 V through linear extrapolation of I_D versus V_G.
- The subthreshold slope $S^{-1}=d\log(I_D)/dV_G$ in decade/mV; S is the swing.
- The maximum transconductance as the maximum of $g_m=\partial I_D/\partial V_G$.
- The series resistance R_{SD} defined by V_D/I_D in strong inversion for devices with different lengths extrapolated to 0.
- Drain Induced Barrier Lowering or DIBL=$\Delta V_T/\Delta V_D$.

RADIATION CONDITIONS

- The radiation and testing conditions have been described in Technical Note 1. Unbiased 60 MeV proton irradiations have been performed at the Cyclone facility in Louvain-la-Neuve up to a fluence of 10^{12} p/cm^2 in week 46 (Nov. 9-13, 2009).
- Post-rad testing at least one week after irradiation ('cooling' of the samples in LLN).

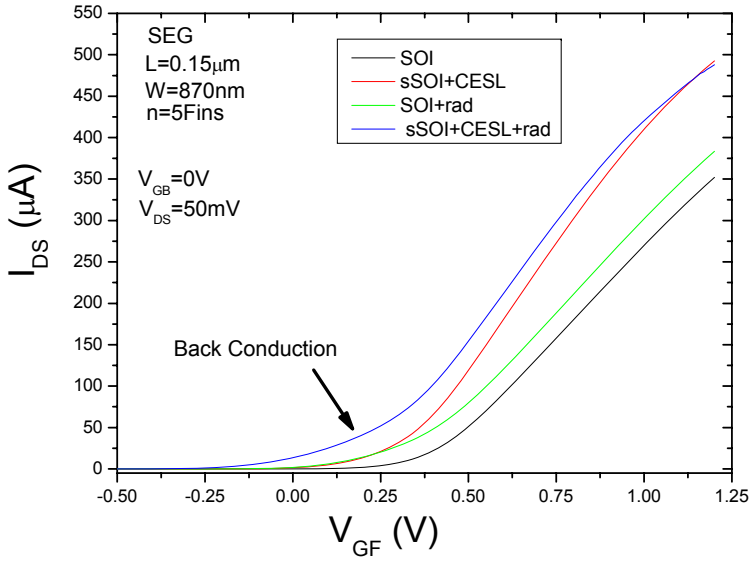
RESULTS (HIGHLIGHTS)

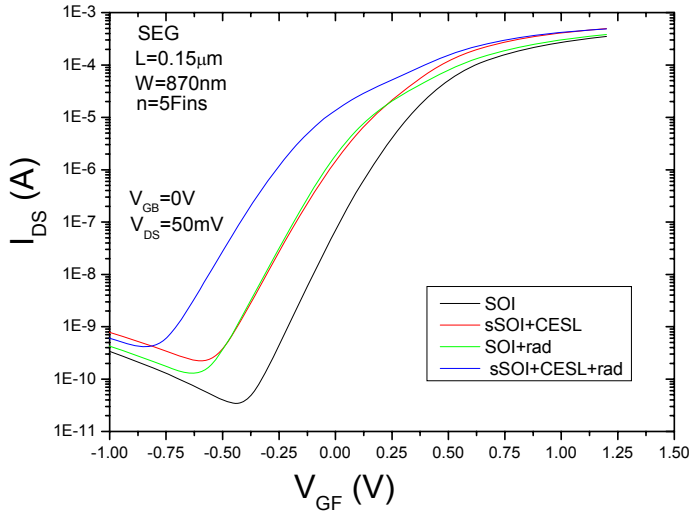




As expected, narrow fin devices do not show strong degradation in the input characteristics.

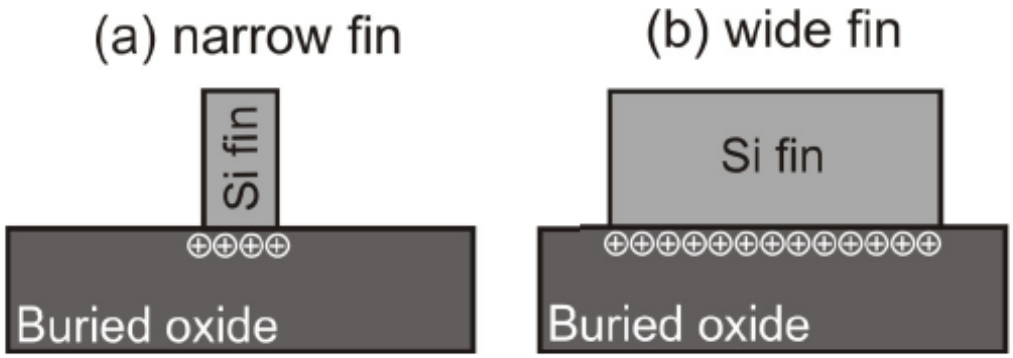
RESULTS (HIGHLIGHTS)

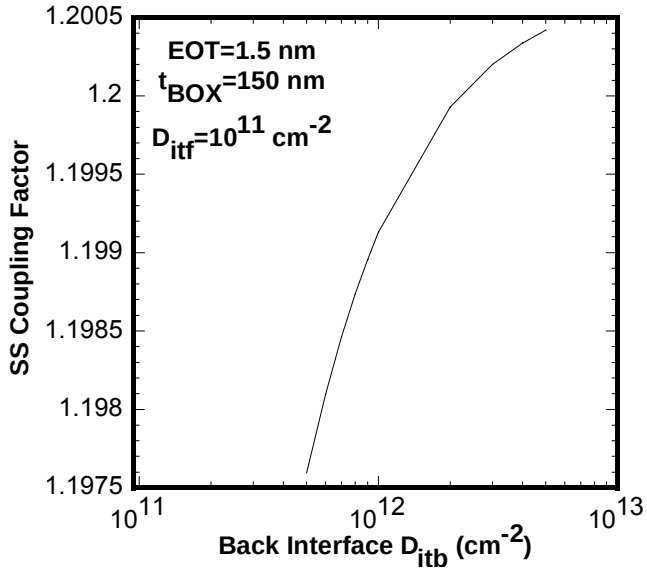




Wide nMuGFETs ~FD SOI FET exhibits back-channel conduction at V_{BG}=0 V, which increases after irradiation. This is in line with positive charge trapping in the BOX.

SUBTHRESHOLD SWING

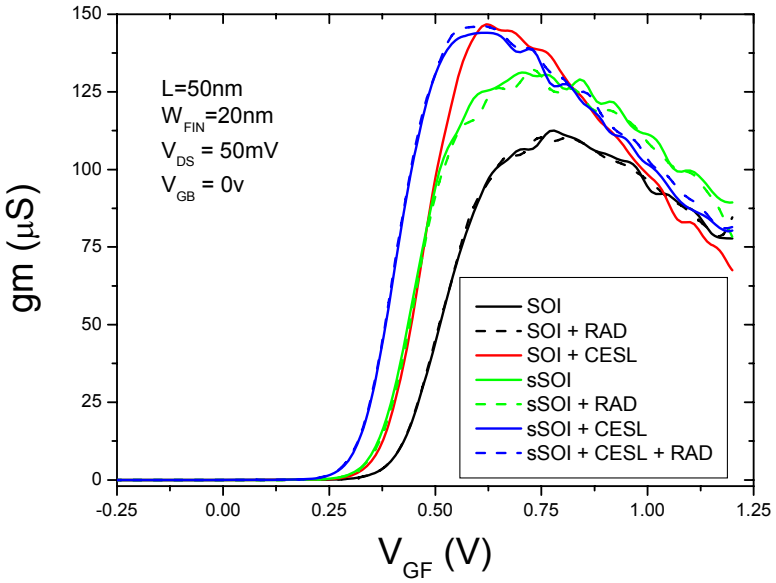


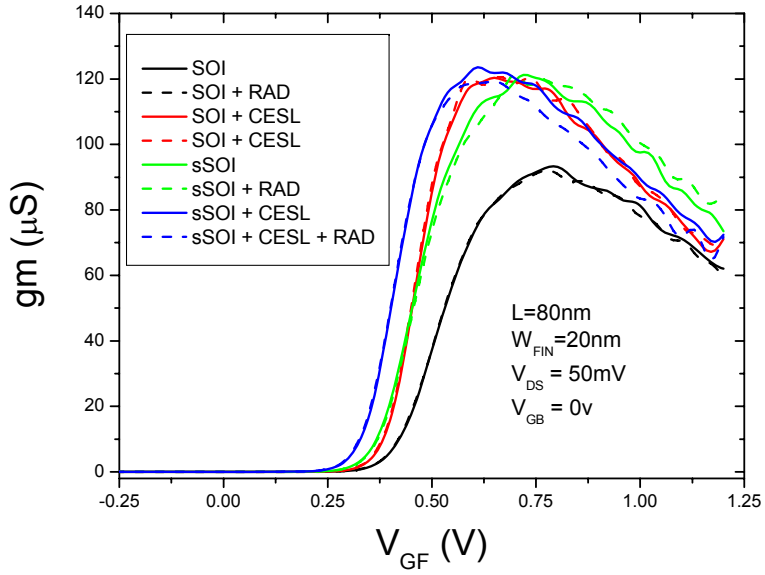


Increasing SS for nMOS follows from increased back-channel conduction after irradiation.

Reduced SS for p-MuGFETs follows from a combination of Fermi level shift with hole trapping, reduced effective interface charge and reduced coupling factor.

RESULTS: MAX TRANSCONDUCTANCE





For narrow MuGFETs, little degradation of the transconductance.
This suggests already little radiation-induced strain relaxation.

CONCLUSIONS

- Narrow p- and nFinFETs generally do not show degradation of their characteristics for 10^{12} p/cm^2 at 60 MeV, within the measurement accuracy of a few %.

- Note that some n-MOS chips have broken down after irradiation, but this is most likely due to the fact that they are at the edge of the test chip.

CONCLUSIONS/2

- Wide n- and p-MuGFETs do show some clear degradation, since they are closer to a fully depleted SOI transistor.

- For wide n-MugFETs, the SS and DIBL increases due to the increase of the back-channel conduction. This results from positive charge trapping in the BOX, yielding a lower back channel threshold voltage.

CONCLUSIONS/3

- For wide p-MugFETs, the SS and DIBL decrease due to the increase of the back interface surface potential. This results from positive charge trapping in the BOX, yielding a higher back channel threshold voltage.

- The low-field mobility of the devices shows a consistent trend: small increase for p- and decrease for n-channel FinFETs.

CONCLUSIONS/4

- No clear evidence has been found for proton-radiation-induced strain relaxation both for narrow or wide fin devices.

- This is different from the case of heavy neutron irradiations (few 10^{14} p/cm^2) where mobility degradation in n-channel devices could be interpreted in terms of displacement damage induced strain relaxation.

INITIAL RESULTS OF THE POST-IRRADIATION TESTING OF THE HIGH-κ/METAL BULK DEVICES

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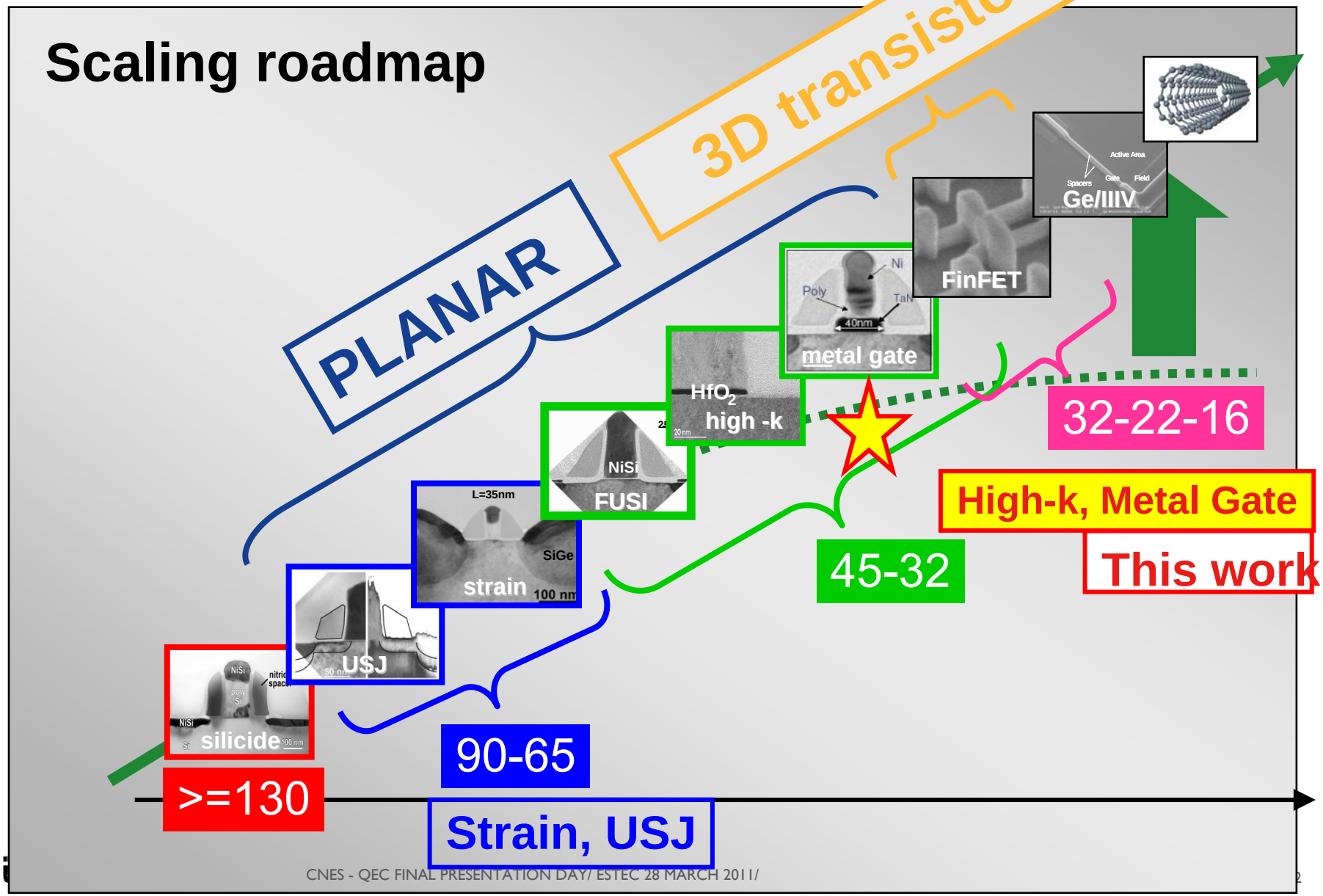
OUTLINE

- Advanced MG – High K Gate first CMOS
- Irradiation Experiment
- Results: highlights

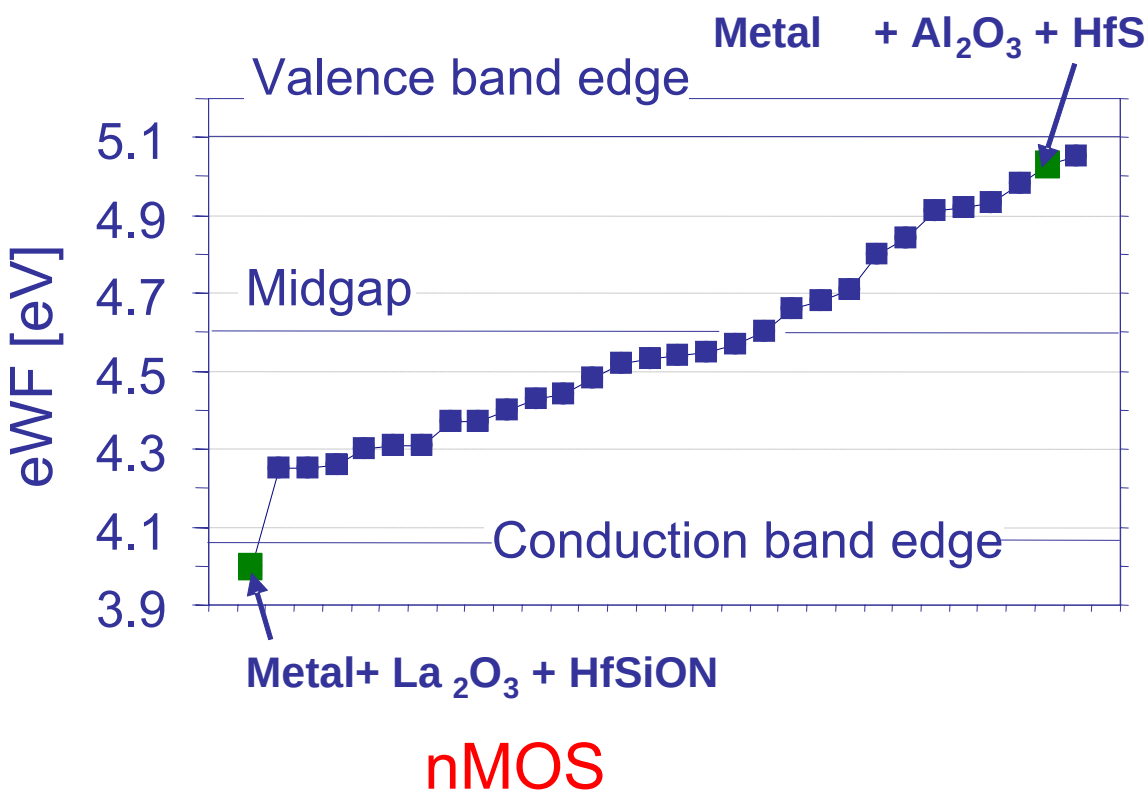
Impact of irradiation on next generation process modules

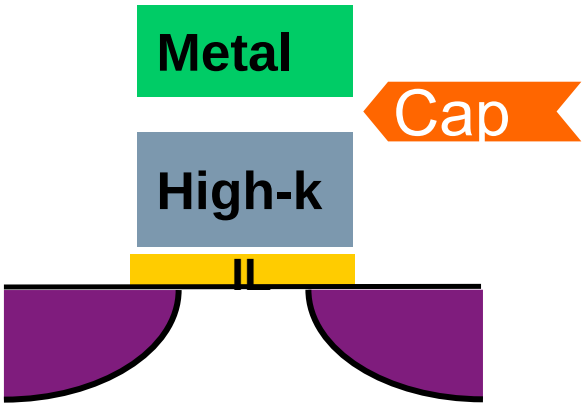


INTEGRATION :GATE FIRST METAL GATE

Gate first approach

A production worthy option implies minimal process adaptations
⇒ A thin metal is inserted and capped with polysilicon (MIPS)
⇒ use 1 metal with an additional tuning option (capping layer) that allows to reach the needed work functions.





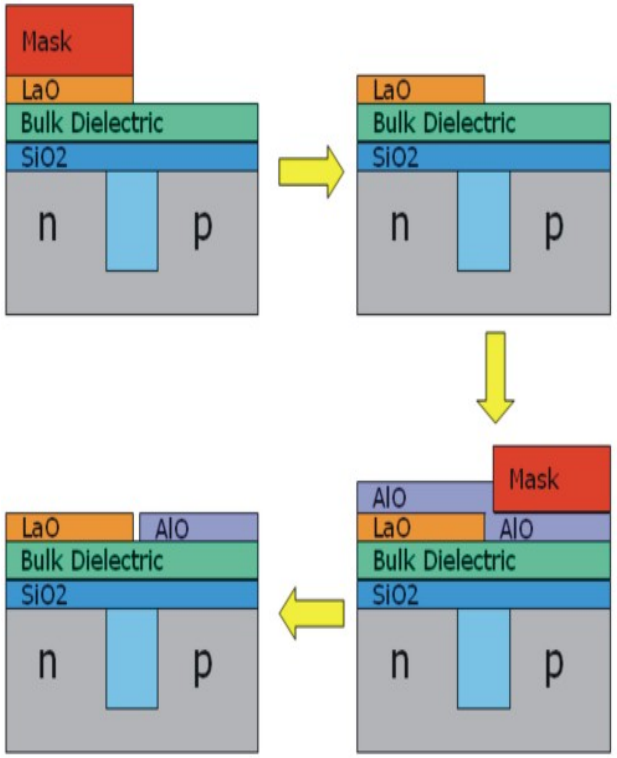
S. Kubicek et al., IEDM 2007 (La_2O_3,Al_2O_3)

PROCESSING ASPECTS: SMDD FLOW

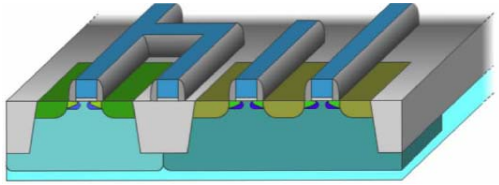
- nMOS devices processed with 5 nm TiN electrode and a La cap on the high-κ gate dielectric

- pMOS devices processed with 5 nm TiN electrode and a Al_2O_3 cap on the high-κ gate dielectric

- 300 mm wafers



MEASUREMENTS



E-TEST: devices tested

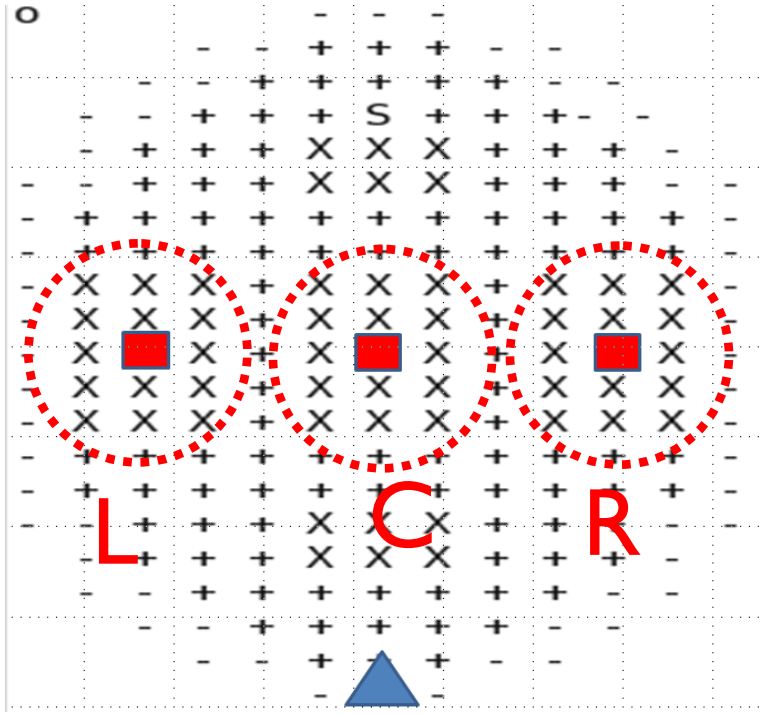
Front-end

Transistors analysis
Arrays of active devices
JG -nFET/pFET
ITP curves: Idsat/Ioff
Vt sat roll-off

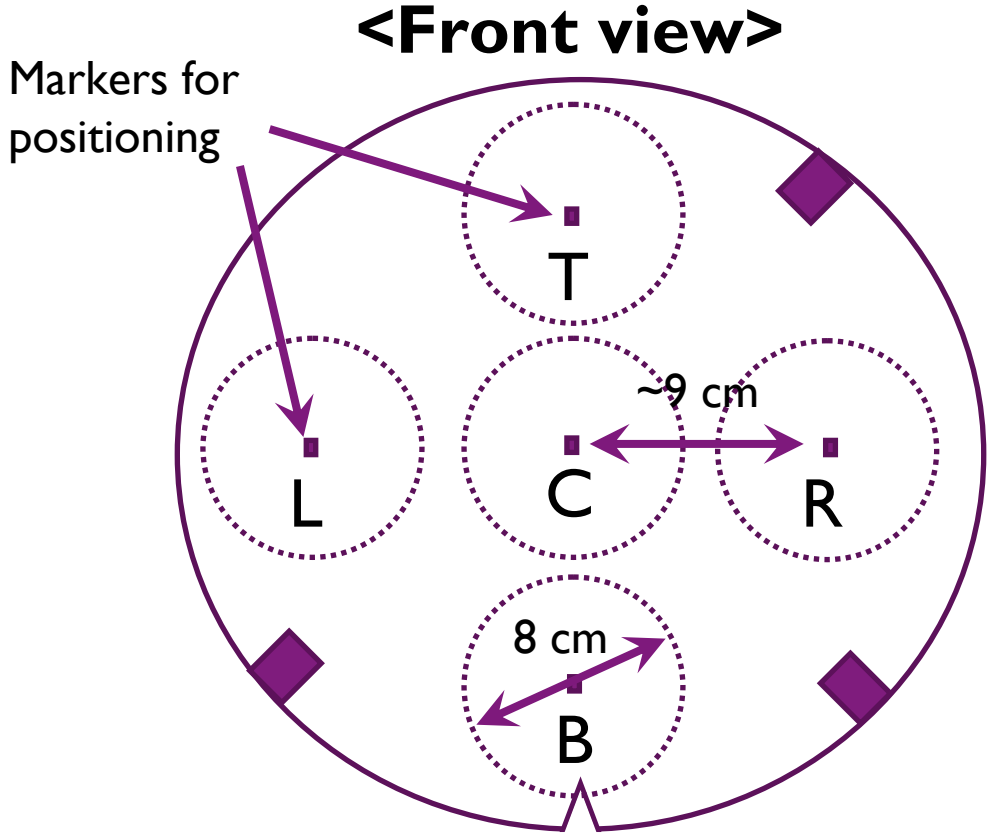
Diodes analysis
Diode leakage

Sheet resistance
Active, poly VDP sheet R

Wafer map



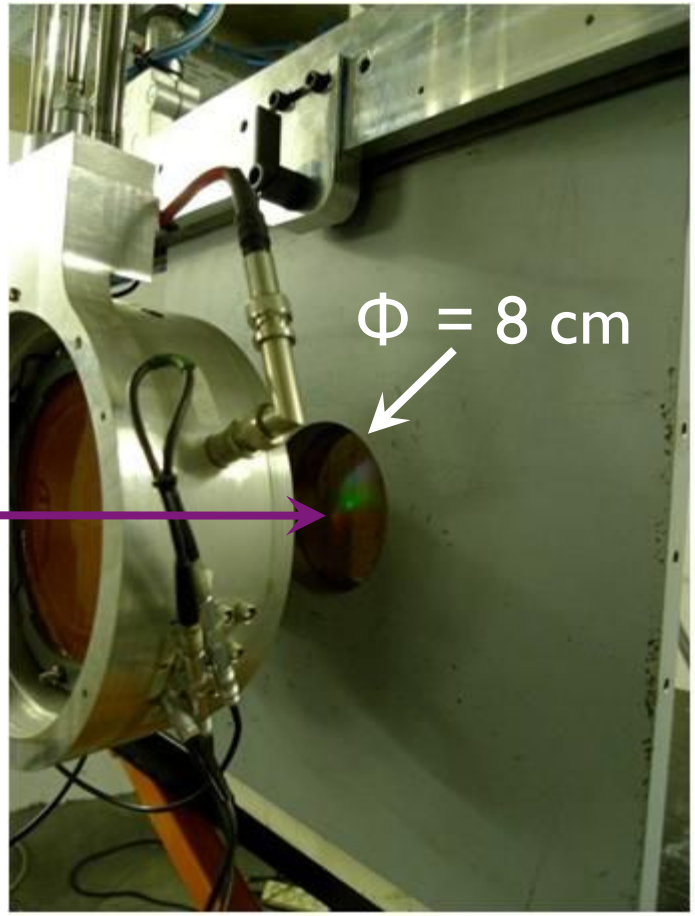
WAFER PREPARATION BEFORE IRRADIATION



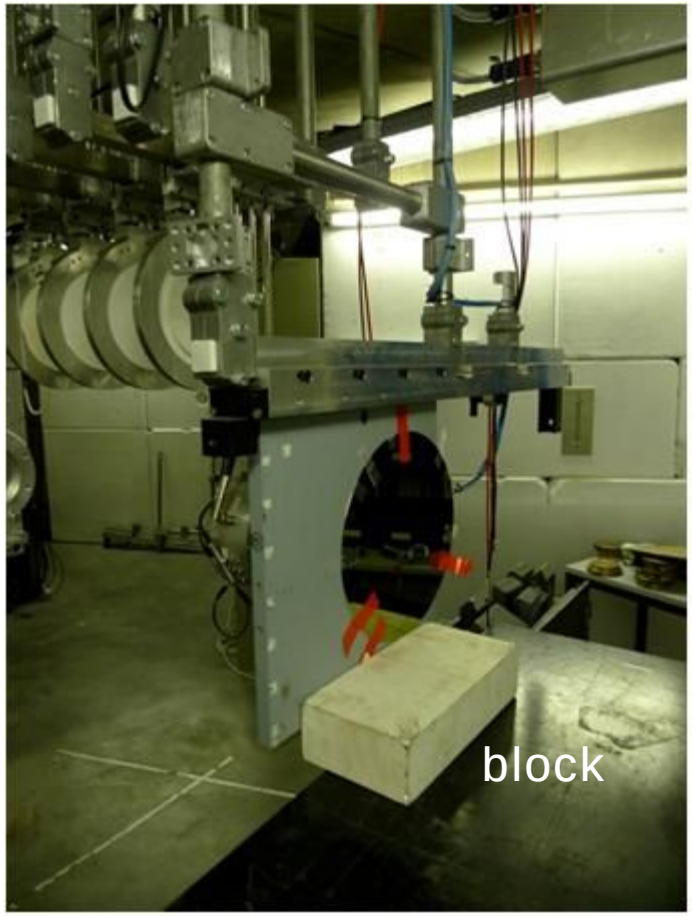
1. Put 5 marks (C, L, R, T, B) with a marker pen for positioning with the laser beam

WAFER SETUP ON IRRADIATION APPARATUS

<Front side>



<Back side>

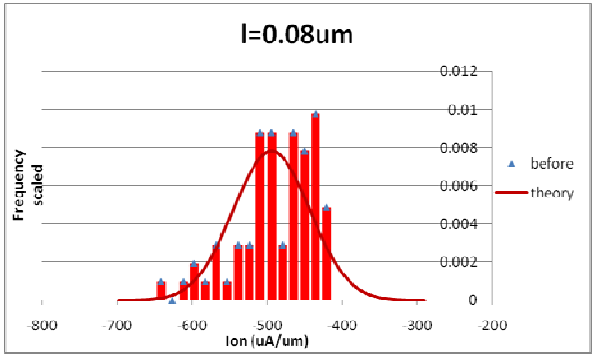


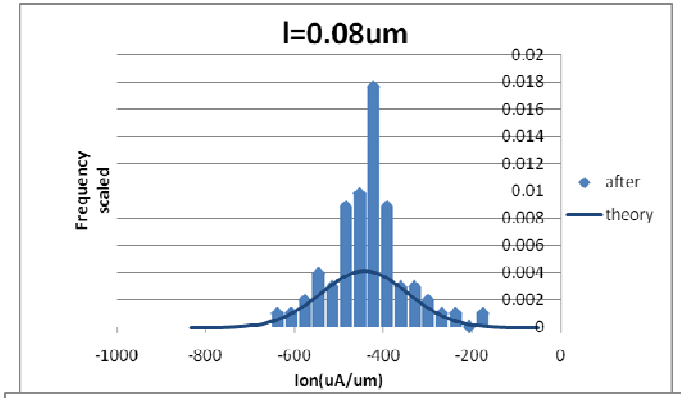
1. put the wafer on a block to prevent falling
2. positioned the wafer using a reference mark and laser beam
3. Fixe the wafer

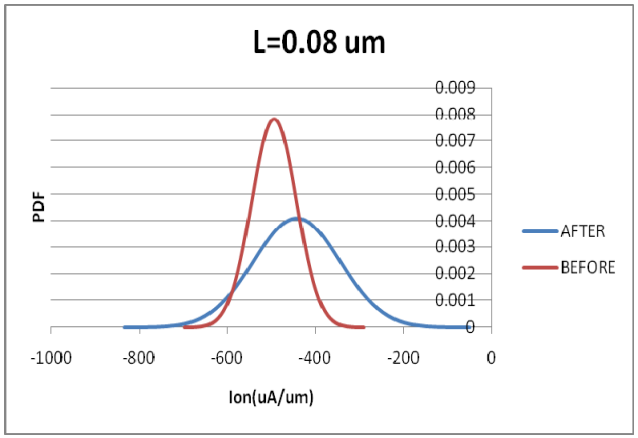
IRRADIATION

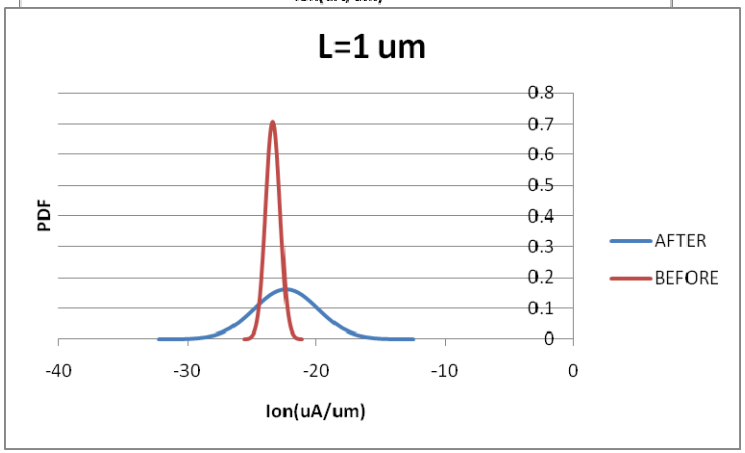
RUN	Energy (MeV)	POSITION	START	STOP	MEAN FLUX (1/cm² s)	Fluence (1/cm²)
1	62	C	9:30	10:30	3E8	1E12
2	62	L	16:20	17:15	3.33E8	1E12
3	62	R	17:15	18:15	3.25E8	1E12

RESULTS: HIGHLIGHTS





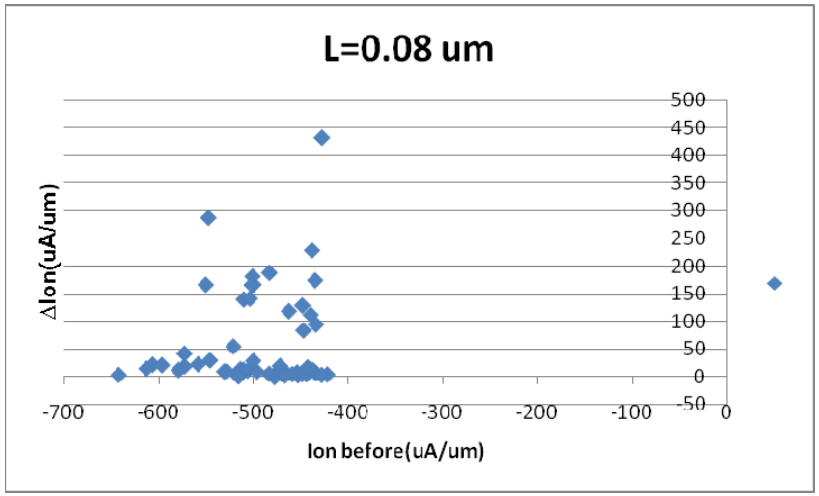


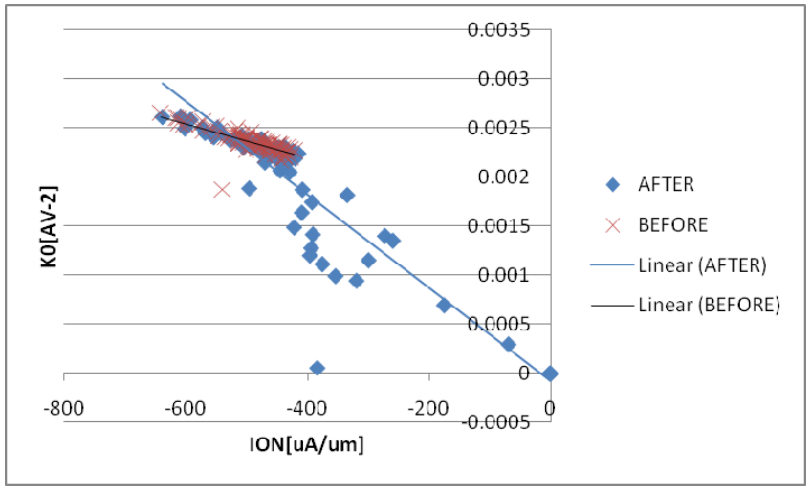


Before irradiation: the on current of the pMOSFETs is statistically distributed due to process variability.

After irradiation: radiation-induced variability further widens the distribution.

RESULTS: HIGHLIGHTS





The radiation-induced variability is ***uncorrelated*** with the process-induced one.

The degradation of I_{on} of the pMOSFETs is due to the degradation in the transconductance (series resistance).

CONCLUSIONS

- The TID response of advanced CMOS is no longer deterministic but should be described in statistical terms. More detailed analysis has shown that a Gaussian distribution is too simple to describe the results.

- It is shown here that the radiation-induced variability adds on top of the process-induced one.

- MG/high-κ pMOSFETs mainly show series resistance degradation. The n-channel devices exhibit degradation of the gate stack (I_G, subthreshold slope,...) → effect of the La cap layer?