SEE and TID
Radiation Test Results
of Digital Circuits Designed and Manufactured in ST 40nm/45nm/65nm/90nm/130nm CMOS technologies

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Headline

- **Circuits tested**
  - 5 technologies
  - 8 test vehicles
- **Test plan performed over 2009**
  - 4 test facilities
  - ~800 test runs
- **Main SEE HI/proton test results and R&D digressions**
  - latchup and hard fail results
  - SEU cross-sections on 45nm SRAMs
  - well tie frequency and SEU
  - low-E proton ionization with Low-LET ions
- **Main TID test results**
  - up to 300 $krad_{Si}$
- **Conclusion**

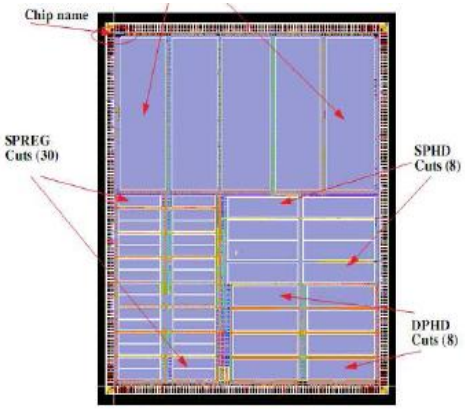
5 test vehicles tested in 65, 90 and 130nm

- **5 test vehicles in ST CMOS 65nm/90nm/130nm**
  - for validation of terrestrial rad-hard Flip-Flops ❹+ ❻
  - for Soft Error Rate characterizations of libraries ❺
  - for electrical characterization of libraries ❼
  - for validation of terrestrial rad-hard and ULP SRAM ❽

rFF65 ❹

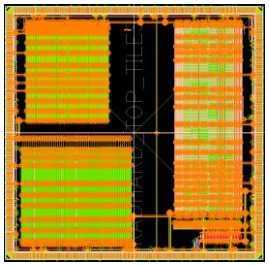
->72k rad-hard FF

SERVAL65-Alliance ❺



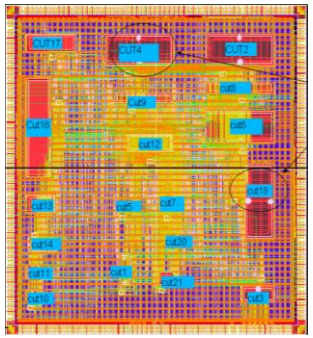
->10Mb SRAM
->500k std FF

SERM10 ❻



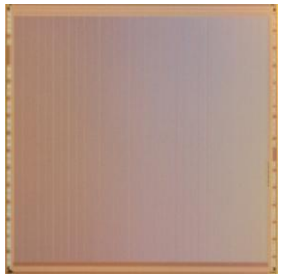
->160k rad-hard FF

SP10LLC ❼



-> 1Mb SRAM

Medical SRAM ❽



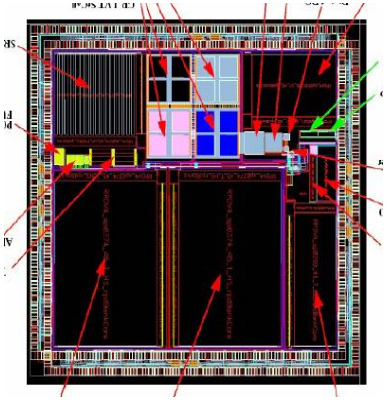
-> 8Mb rad-hard SRAM

- **pre-characterization with alphas and atmospheric neutrons**
  - set-ups developed by ST and kindly reused for this contract at no cost

3 test vehicles in 45/40nm

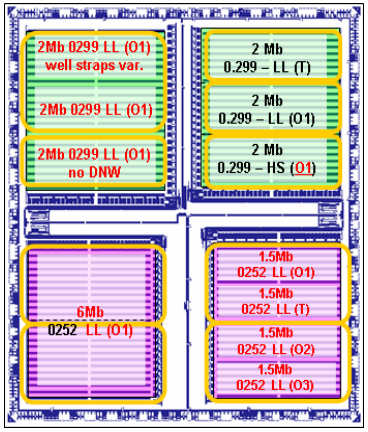
- **3 test vehicles in ST CMOS 45nm/40nm embedding SRAMs**
  - libraries validation and PROcess MOnitoring in the time ❶+ ❸
    - SRAMs, ROMs, standard cells, via chains (back-end stress), ring oscillators (speed meas.), dividers (delay path meas.), IOs, Fuse : 75 M transistors & 24mm²
  - for characterization of Single Port SRAM in large memory cuts ❷

Promo45 ❶



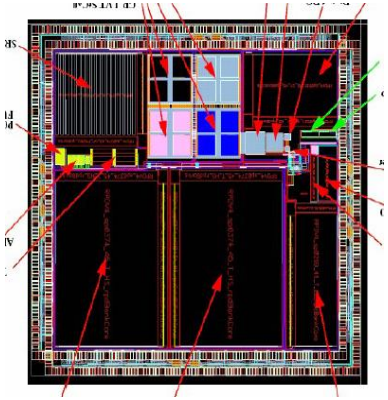
->13Mb SRAM

Pantera45 ❷



->24Mb SRAM

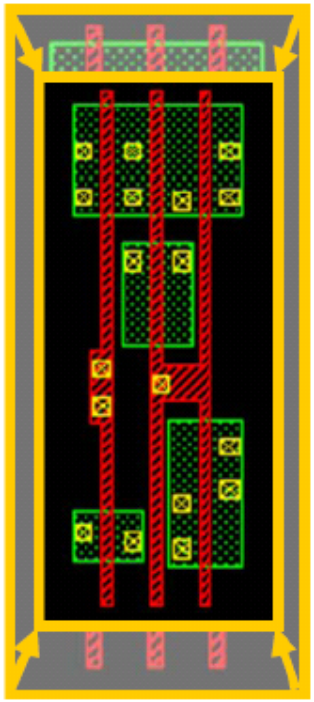
PROMO40 ❸

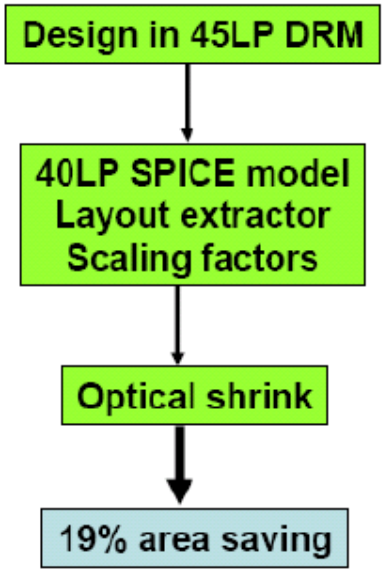


->13Mb SRAM

40nm is an optically shrunk technology

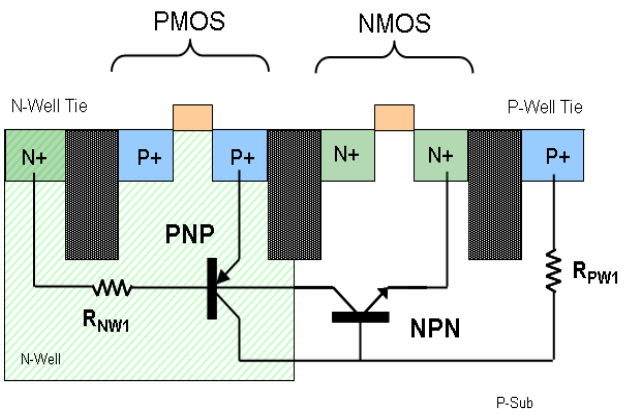
- **What is a shrunk technology?**
  - Daughter is 10% linear shrink of Mother
  - All nominal devices aligned
  - Daughter is built-in within mother technology
    - allowing fast transition (same DRM, DRC)
- **Example of ST Mother (45nm) and Daughter (40nm)**





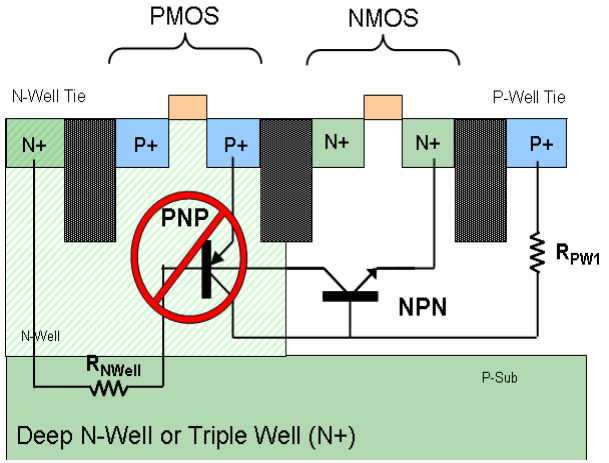
Reminders about ST Deep-NWell (DNW) layer

- **DNW is reversed-biased N+ buried layer**
  - Enabling Ultra Low power
  - Reducing Noise from substrate
- **DNW removes SEL**
  - proven in ST 90/65nm at VDD+40% and 125degC
  - *ST papers at NSREC'07 and ESA QCA days 2007/2009*
- **DNW increases SER/MCU**
  - by reinforcing natural bipolar in Pwell
  - *ST papers at IRPS 2010*

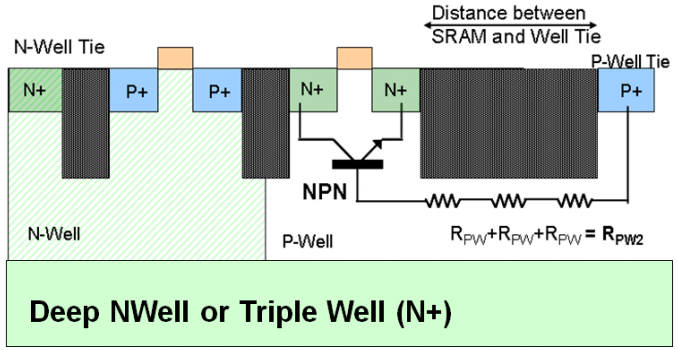


Deep-NWell added beneath CMOS inverter

SEL



MCU



Test vehicles overall content

- **+50 Mbits of SRAMs**
  - 1 rad-hard terrestrial SRAM covered by 2 eDRAMs
- **~1.5 M of Flip-flops**
  - 6 flavors from production libraries
  - Rad-hard terrestrial Flip-flop in 2 technologies
- **8 SRAM areas :**
  - 0.252µ2, 0.299µm², 0.374µm², 0.52µm², 0.62µm², 0.98µm², 1.3µm², 4.3µm²
- **2 SRAM architectures :**
  - SP (single port) and DP (dual port)
- **2 technologies :**
  - standard and Flash compliant
- **2 Threshold Voltages :**
  - Standard and High VT (low power)

Test vehicle name	Techno option	Generator	Device	DNW	Size
SP10LLC	90nm (flash)	SP10LLC	1,3µm2	none	0,312Mb
		SP10LLC	1,3µm3	none	0,312Mb
SERVAL65	65nm LP	DPHD	0.98µm²	both	1Mb
		SPHS	0.525µm²	both	2Mb
		SPREG	0.62µm²	both	2Mb
		shift-registers	plain FF, X4, 13T	both	199K
		shift-registers	plain, X35	both	159K
		shift-registers	plain, X4, 9T	both	194K
		shift-registers	clear, x4, 13T	both	194x2K
ROBUSTFF65	65nm LP	shift-registers	largest rFF	none	2x36K
PROMO45	45nm LP	RPD HS	0.374µm²	yes	5Mb
		RPD LL	0.374µm²	yes	5Mb
		RPD HS	0.299µm²	yes	2Mb
PROMO40	40nm LP	RPD HS	0.374µm²	yes	5Mb
		RPD LL	0.374µm²	yes	5Mb
		RPD HS	0.299µm²	yes	2Mb
PANTERA45	45nm LP	SP SRAM LP1	0.299µm2	yes	2Mb
		SP SRAM LP2	0.299µm2	no	4Mb
		SP SRAM LP3	0.299µm2	no	2Mb
		SP SRAM LP4	0.299µm2	no	4Mb
SERM10	90nm (flash)	shift-registers	largest rFF	none	4x40K
Medical	130nm	stand-alone	4,3µm2	none	8Mb

Effective test plan

- **4 test campaigns in 2009: RADEF, UCL & PSI (~1 week) and ENEA (50 days)**
  - 9-14 ion-LET and 6-8 proton energies
- **Extensive Design-of-Experiment:**
  - 3 Patterns
  - 10 power supplies
  - 5 Temperatures
  - minimum 2 samples tested per circuit

-474 test conditions

-768 test runs

device	Pattern	Power Supply	Temp.	Algorithm	# of runs
Oct-Dec 2009: ENEA +40days experiments to 296krads					
5 devices	-	Nominal	Room	-	1
Sept-2009: PSI Effective Design of experiment					
Promo45	CKB/ALL0/1	1.0V/1.1V/1.21V	25/125°C	Static	53
Pantera45	CKB/ALL0/1	1.0V/1.1V/1.21V	25/125°C	Static	50
rFF65	ALL0/ALL1	1,2V	25/125°C	Static	
SERVAL65	CKB/ALL0/1	1,08V/1.2V/1.32V	25/125°C	Static/Dyn.	60
SP10LLC	CKB	0,9V/1.2V	25°C/100°C	Dyn./PowerDown	32
Med. SRAM	CKB/ALL0/1	1.4V/1.5V	25/125°C	Static	59
RADEF May 2009					
Promo45	CKB	1.0V/1.1V/1.21V	25/125°C	Static/Dyn.	83
Pantera45	CKB	1.0V/1.1V/1.21V	25/60/80/100/125°C	Static	53
rFF65	CKB/ALL0/1	0,55V/0,96V/1,08V/1.2V	25/125°C	Static/Dyn.	87
SP10LLC	CKB	0,9V/1.2V	25°C/100°C	Dyn./P-Down/Stat	53
UCL March 2009					
Promo40	CKB	1.1V/1.21V	25°C/100°C/125°C	Dynamic	59
SERM10	CKB/ALL0/1	0.85V/1.2V/1.32V	25/125°C	Static/Dyn.	131
Med. SRAM	CKB	Nom./BackBias	25/125°C	Static	43

Test results for latchup and hard fail

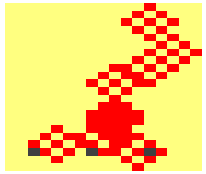
- **Rare latchup events at high LET/Vdd/Temp on devices:**
  - without Deep N-Well in 90LP / 65LP

- **No Latchup ever recorded during irradiations on devices:**
  - with Deep N-Well in 65LP / 45LP / 40LP
    - with heavy ions and protons,
    - up to 120 MeV.cm2/mg and VDD + 20% and 125 degC
  - without Deep N-Well in 45LP/40LP
    - with heavy ions and protons,
    - up to 120 MeV.cm2/mg and VDD + 10% and 125 degC

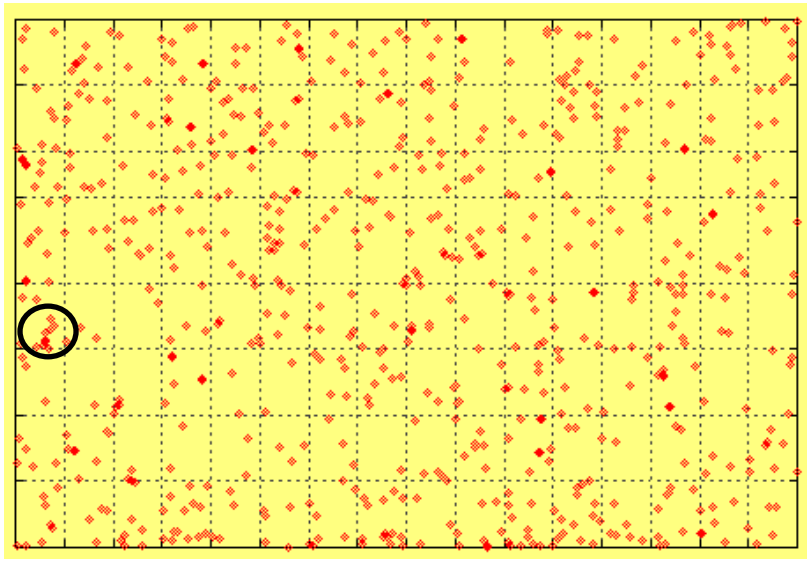
- **No hard fail or permanent damage ever recorded during all tests**
  - on circuits in ST CMOS 130nm, 90nm, 65nm, 45nm and 40nm
  - with heavy ions up to 120 MeV.cm2/mg
  - With proton up to 230 MeV
  - VDD up to nominal + 10%
  - temperature up to 125degC

Reminders on flips/SBU/MCU/events

1 event : 1 or several bits fail at one time



1 flip : ◆
1 radiation-induced soft error

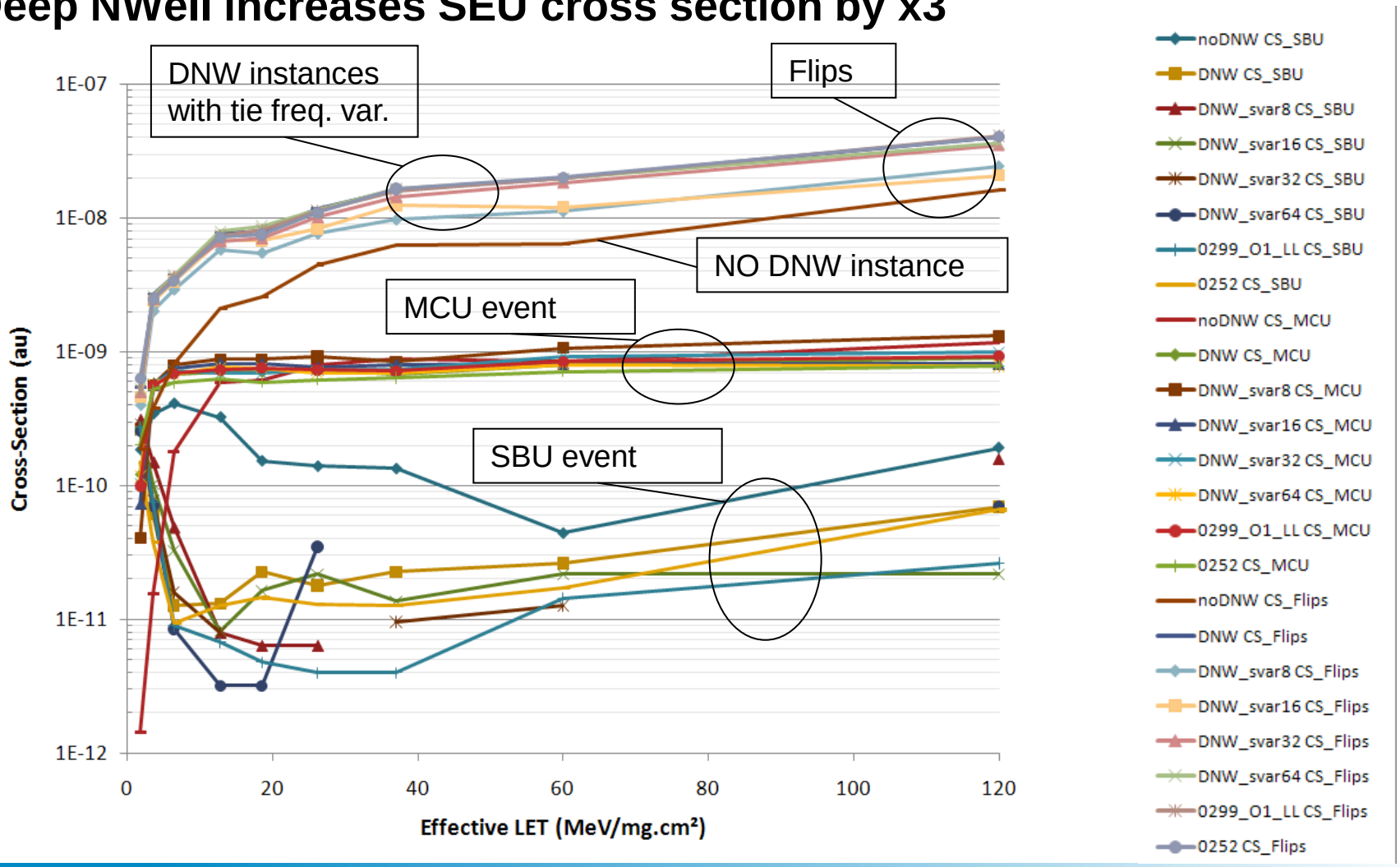


Bitmap error

- **Single Bit Upset or SBU: 1 event of 1 bit fail**
- **MCU : multiple upsets**
- **MBU : MCU in same logic word**
- **No MBU ever recorded**
  - With ad-hoc internal multiplexation (scrambling) in ST memory arrays
- **EDAC can be 100% efficient**

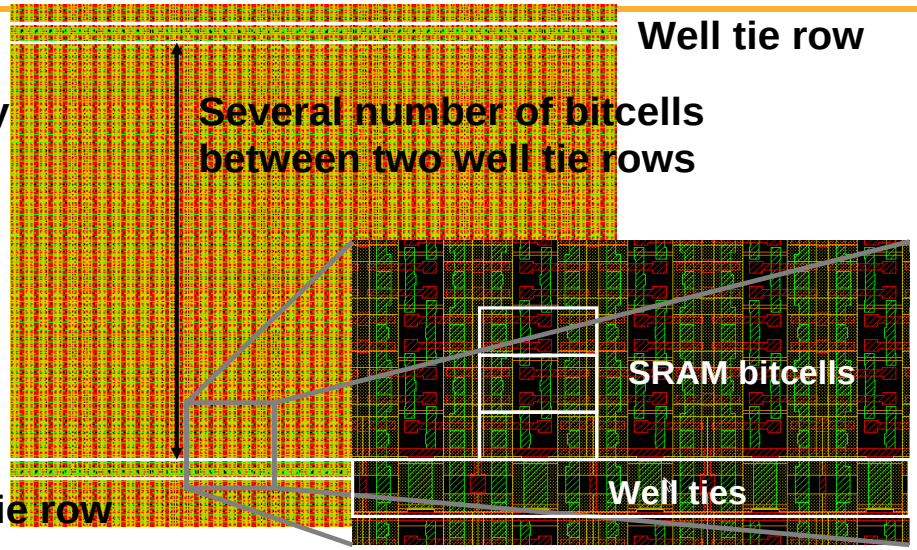
Focus on HI results on 45nm SRAM test circuit

- **Unmitigated asymptotic cross-section 5E-8 to 2E-7 /cm2.bit**
- **Deep NWell increases SEU cross section by x3**

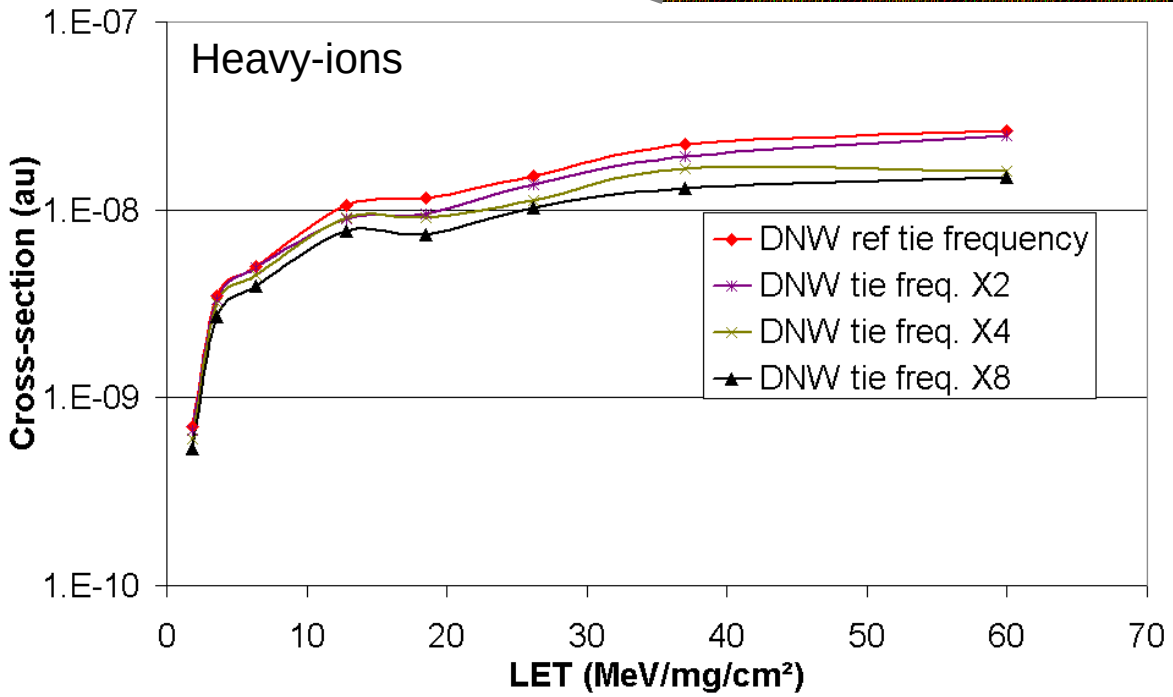


Focus on well ties in SRAM array

Well tie frequency studied
- -Reference
- -Reference x 2
- -Reference x 4
- -Reference x 8



Presented at IRPS'10

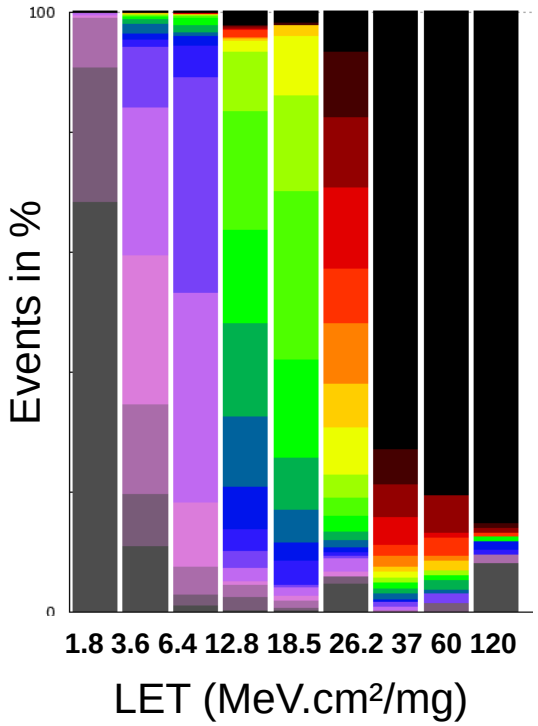


Higher well tie freq.
= lower cross section
= smaller MCU events

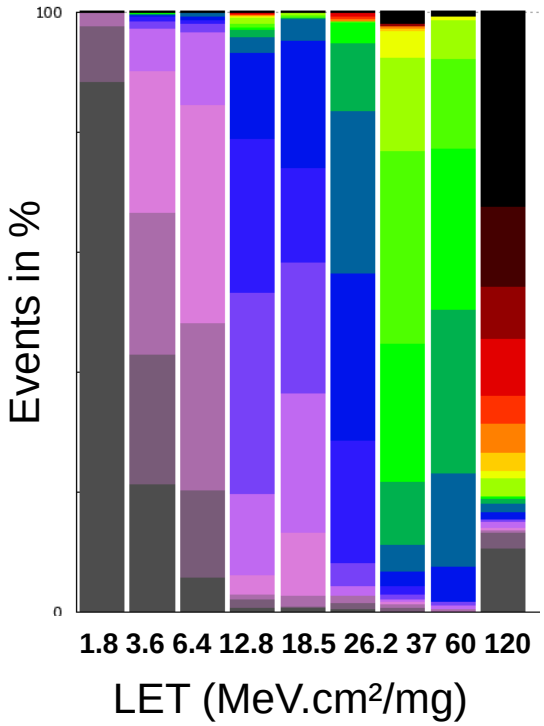
Focus on HI test results 45nm: MCU

- **With DNW Higher tie freq. reduces upsets number per MCU events**
  - smaller cross section
  - well tie reduce bipolar amplification
- **Smallest number of upset per event is observed for device without DNW**

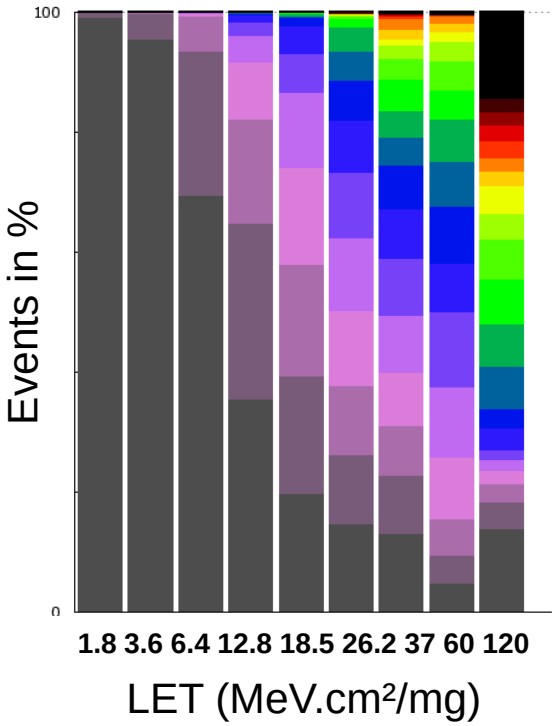
45nm with DNW with standard well tie density

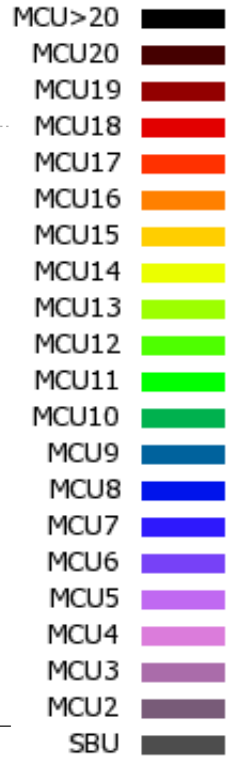


45nm with DNW with well tie density x8



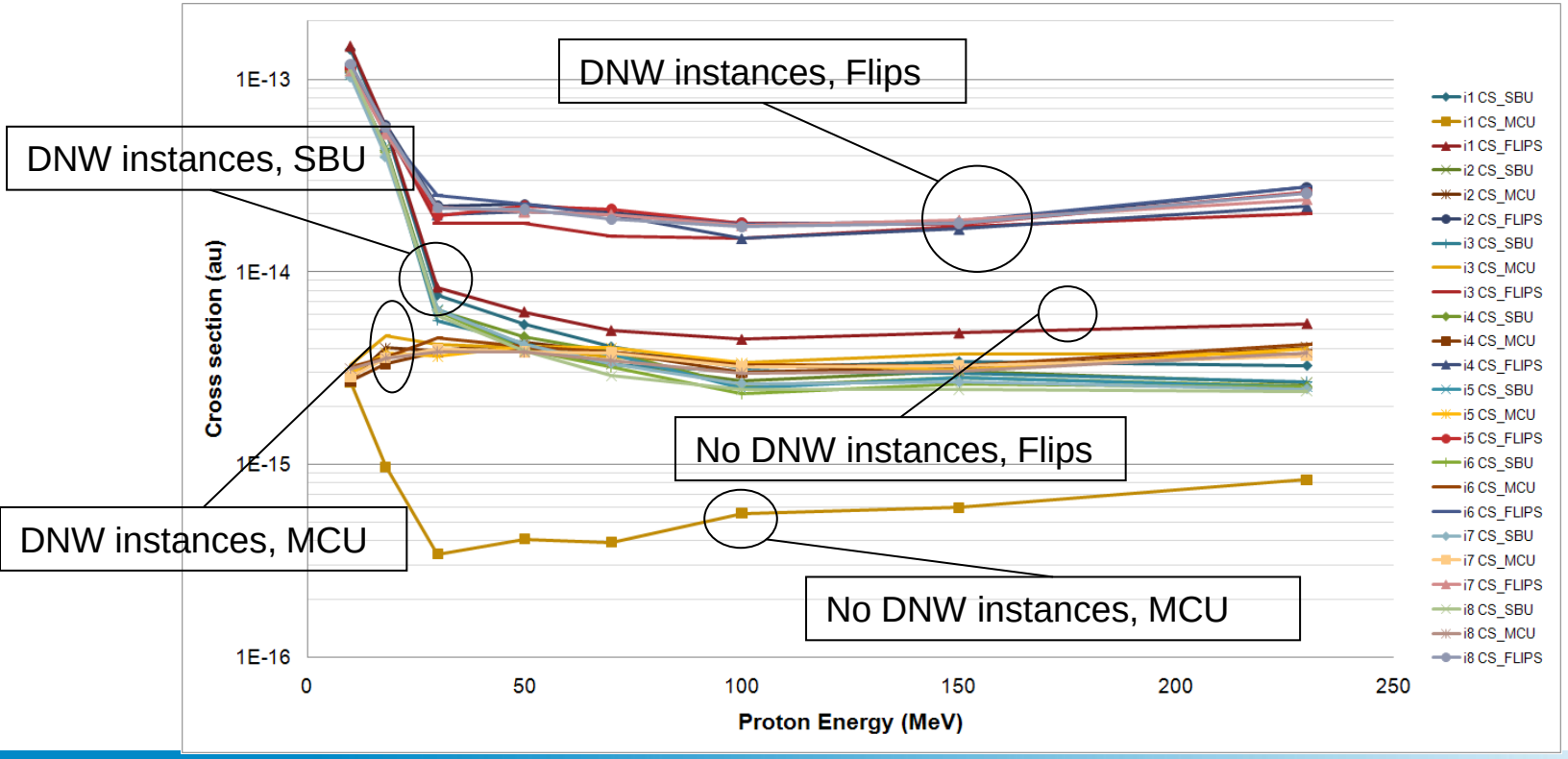
45nm without DNW with standard well tie density





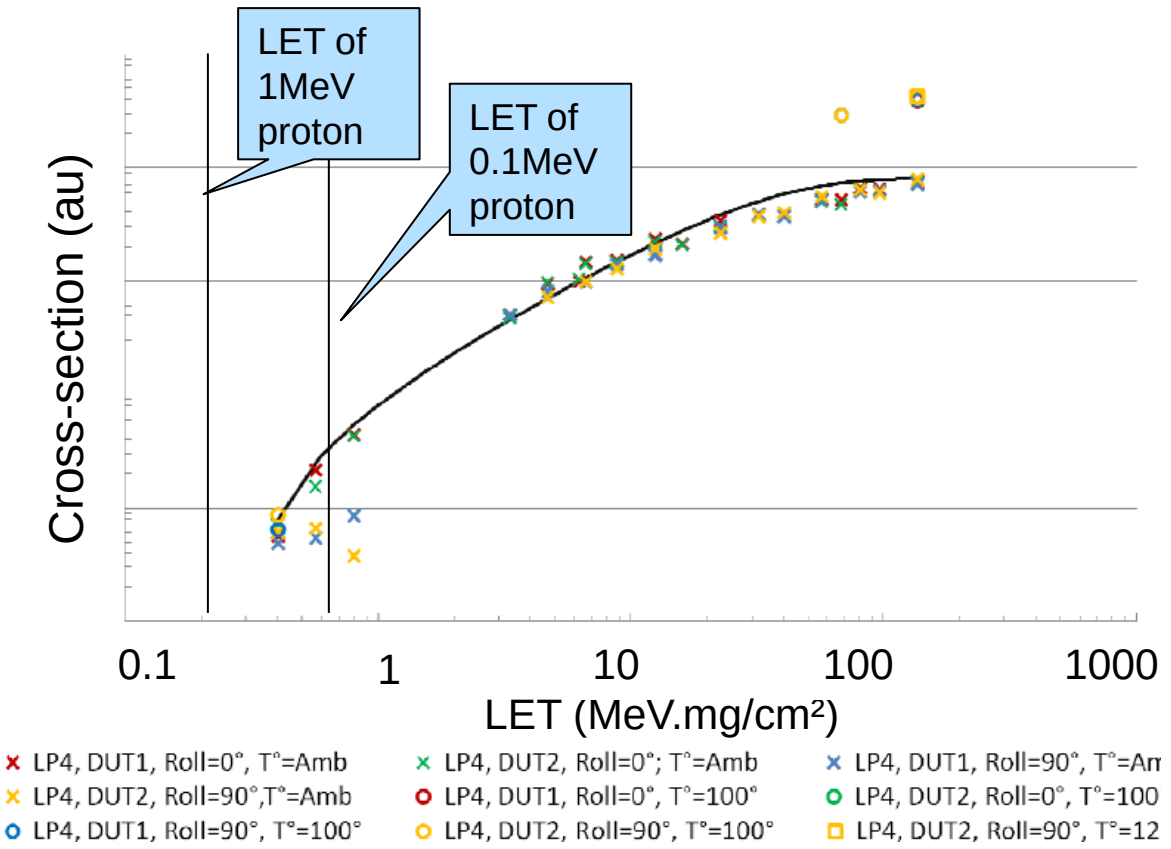
Focus on proton results on 45nm SRAM circuit

- **Proton cross-sections 2^{E}-14 cm2/bit (no DNW) to 9^{E}-14 cm2/bit (DNW)**
- **10 and 20 MeV cross-sections increase attributed to**
  - Low-E proton ionization: proton LET @20MeV very small (1/10 LET@1MeV)
    - same behavior on SRAM cell with higher Qcrit (90nm).
  - 100MeV residue pollution: probable since MCU cross-sections increase as well
- **Specific 1MeV – 3MeV proton measurement needed to conclude**



R&D digression: using low-LET ions to emulate Proton ionization

- **Facility:**
  - UCL, Be
- **Experimental details:**
  - Helium ion
  - 0.3-0.5-0.7 MeV.cm²/mg
  - Temp. & roll angle
- **Test vehicle:**
  - 40nm SRAMs
- **No cross section increase @ Low LET**



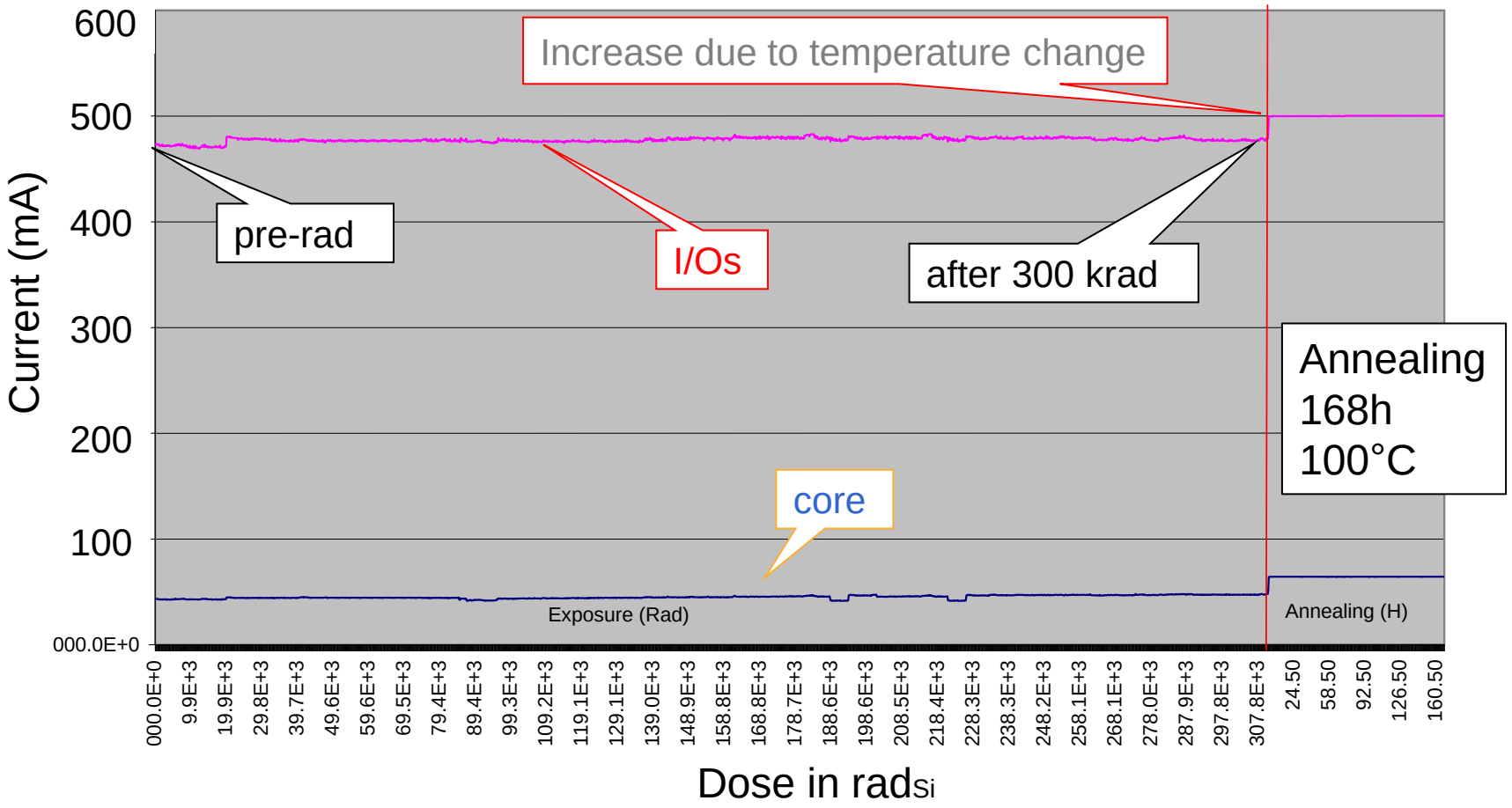
TID test results at ENEA with Cobalt 60 source

- **300krad$_{Si}$ TID Experimental details at ENEA, Rome**
  - all devices power supplied at nom. VDD
  - all devices with input signals tied to specified values (not floating)
  - preferential pattern
  - dose rate ~292radSi/h
  - 24hours annealing biased @ Room temp. + 100h annealing biased @100°C
  - current monitored on all power lines of each board. Sampling 30minutes
    - +2000 read points per device
- **Four technologies (5 test vehicles) tested**
  - 45nm: Promo45 SRAM
  - 65nm: rFF65 no DNW & SERVAL65
  - 90nm: SP10LLC
  - 130nm Medical SRAM
- **No over consumption at 300kradSi**
  - zero current increase on all power domains
- **100% functionality at 300kradSi**
  - first order functional parameters unchanged

Evidence of TID immunity @ 300kradSi

Focus of TID results in 45nm

- **100% functionality and no overconsumption after**
  - +1000h of continuous gamma irradiation @252radSi/h
  - 100h annealing @100°C



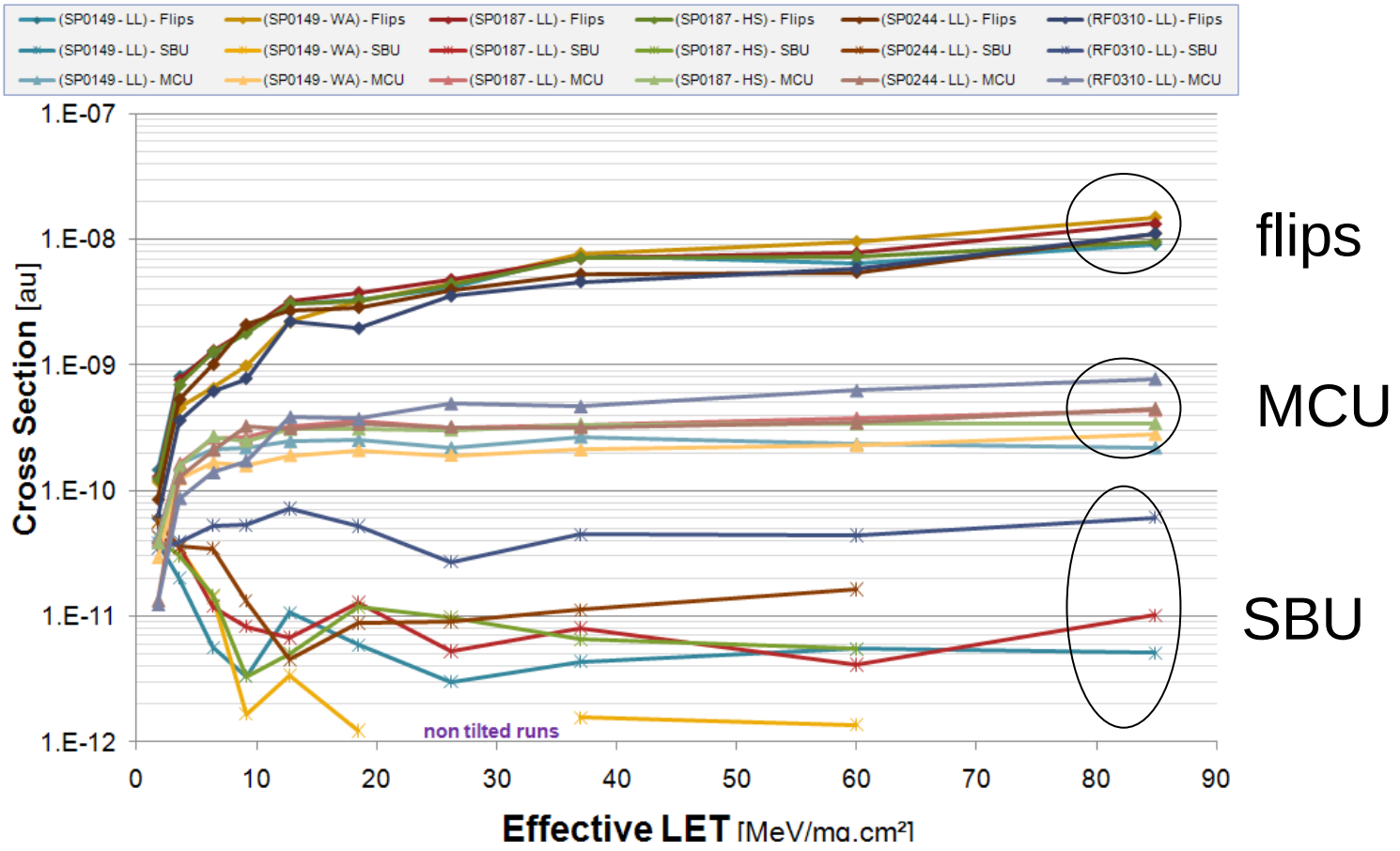
Radiation hardness further improves… in 45/40nm

- **SEL immunity verified under heavy ions & protons**
  - Up to 120MeV.cm²/mg & 125°C & Vdd + 10%
  - Up to 230MeV & 125°C & Vdd + 10%
- **Low SEE cross-section & Low MCU/MBU rate**
  - Reduced bipolar effect inside wells (article list)
- **No TID effect up to 300krad$_{Si}$**

Technology	Deep NWell	SEU rate in GEO @ solar quiet	SEL immunity
CMOS0**65**LP	yes	1.4e-6 upset/bit/day	yes
CMOS0**45**LP	yes	1.6e-7 upset/bit/day	yes
CMOS0**45**LP	no	3e-8 upset/bit/day	yes

Radiation hardness further improves … in 32nm

- **SRAM SEL immunity verified under heavy ions (beyond the scope of this contract)**
  - Up to 85MeV.mg/cm² & 100°C & Vddnom + 10%
- **Sat. cross section with DNW < 6e-8cm²/bit**



Conclusions

- **8 circuits jointly tested ESA and ST-Crolles from March to Dec. 2009**
  - with heavy ions, protons and gamma rays
  - using ESA certified beams and test methods
  - ~800 test runs: VDD, temp, pattern, clock, facility, algorithm…

- **High intrinsic radiation hardness measured with heavy ions and protons**
  - no latchup nor hard fail
    - up to 120 MeV.cm²/mg
  - low SEU cross sections with heavy ions / protons
  - EDAC 100% efficient with appropriate scrambling
  - Low energy protons not clearly observable at PSI

- **Very high intrinsic radiation robustness measured with gamma rays**
  - no over-consumption and 100% chip functionality at 300krad for every DUTs
  - no longer need for costly TID mitigation techniques (guard rings, edgeless transistors, …)