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Single Event Latchup Testing
Advanced Analog to Digital Converter
ADC08D1000WG-QV

Hi-Rel Operations

Radiation Engineering/RHA Programs
2900 Semiconductor Dr.
Santa Clara, CA 95052

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Rev. B

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The Sight & Sound of Information

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1.0 Objective

The ADC08D1000WG-QV was evaluated for SEL (Single Event Latchup) performance. The objective was to measure the SEL cross section vs. the effective LET (Linear Energy Transfer) to the maximum cross section and effective LET possible at the experimental facility of use, or to verify that the part is immune to SEL for effective LET's $\leq$ 120MeV/mg/cm^2.

2.0 Conclusion

The Space Level version of the ADC08D1000, the ADC08D1000WG-QV, is immune to SEL with LET's up to 121.89 MeV/mg/cm^2.

3.0 Summary

No latchup was observed, on any of the 3 DUT's (Devices Under Test), at room and hot temperatures, with Bi^{209} at 0° incident angle, LET = 99.85 MeV/mg/cm^2 at the surface of Si. The incident angle was increased to 35°, LET = 121.89 MeV/mg/cm^2 at the surface of Si, and, again, no latchups were observed on the 3 DUT's at both room and hot temperatures.

The control unit was found to have a SEL threshold of between 5.76 and 14.33 MeV/mg/cm^2 (see Table 2, page 11). The control unit consisted of a commercial version of the ADC08D1000, known to be susceptible to SEL. All other conditions of SEL testing on the control unit were identical to that of the 3 DUT's.

4.0 Test Data

See Table 1, page 10, for SEL Data taken on the 3 DUT's. Table 2, page 11, is SEL data taken for the control unit. The control unit was prepared in case no latchups were observed on the Space Level parts to verify and validate the experiment's ability to cause and observe a latchup. The results of Table 2 are comparable to previous results obtained for the commercial version of the ADC08D1000, and, therefore, add an extra degree of validation to the results of "no observed latchups" for the Space Level part.

5.0 Description of Product

The ADC08D1000WG-QV is a dual, high performance, low power monolithic analog to digital converter capable of converting analog input signals into 8-bit words at 1 GSPS (Gigasample per second). It employs two 2.0V dc power supplies (1.8V to 2.0V normal operating supply voltage range). The differential inputs provide a full scale differential swing, selectable, of 650mVp-p or 870mVp-p input, or 560mV to 840mV in 512 steps when using extended control mode (extended control mode was not used during testing and is not recommended for use in radiation environments – see application notes in the military data sheet). The digital outputs from the two ADCs are available on 4 separate differential (Low Voltage Differential Signal, LVDS) 8-bit buses (current and previous sample for each channel clocked out at ½ the sampling rate). The output format is offset binary. The output voltage is selectable to either 3mA (normal LVDS drive) or 2.2mA (reduced drive for reduced power consumption) into a 100ohm differential load. Normal output voltage drive, 3mA, was used for testing by setting the OUTV pin, pin 3, to high (V_A = V_{DR} = OUTV=2.0V).

The ADC08D1000WG-QV, Space Level, die was used for the DUT's. The die was placed in a decapsulated plastic package to facilitate SEE (Single Event Effects) testing.

6.0 Test Method

JESD57 (EIA/JEDEC Standard No. 57), "Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation" was strictly adhered to for test procedures and definitions (available at http://www.jedec.org/). ESCC 25100 was also used as a reference, and, as closely as possible, was adhered to (available at https://escies.org/public/radiation/esa/standards.html). JESD57 defines the requirements and procedures for Earth based SEE testing of integrated circuits. The test method is only valid when using a Van de Graaff or Cyclotron Accelerator. This method does not apply to SEE testing that uses neutrons, protons and other lighter particles. This test method assumes that the accelerator test facility has the ability to mount and position the DUT in a vacuum chamber, provide heavy ion dosimetry; etc. Inquiries and visits to the site have verified that this is indeed the case. All DUT's must be decapsulated.

7.0 Description of Test Setup

The test circuit for the ADC08D1000WG-QV consists of the ADC08D1000 Demonstration Board driven by WaveVision 4 software. The board was secured to the vacuum chamber fixture in the vacuum chamber.

For SEL testing the input was a slowly varying sine wave, approximately 1MHz, full scale, on both the I channel and Q channels (AC coupled through a balun and ac coupling capacitors, 4.7nF). The input signal was clocked in (sampled) at a frequency of 1 GHz. current probes, attached to an oscilloscope, and current meters were used to monitor the total current on both the V_A and V_{DR} power pins of the DUT. A latchup event was defined as a sustained increase in DC current on either the V_A or V_{DR} power pins that persisted until the part was powered down. A temperature controller was connected to the thermistors and to the resistive heaters and provided both temperature measurement and heater control for the hot temperature testing.

A personal computer was connected to the ADC08D1000 Demonstration Board for communication, control, and data gathering. The ADC08D1000 Demonstration Board receives the ADC data clock and output data of the ADC08D1000WG-QV device and stores it in onboard memory. Data and events were uploaded to the personal computer after every run (exposure to accelerated ions) and after every power up sequence to make sure the DUT was still operating correctly.

8.0 Test Plan and Procedures

8.1 Ions, Angles, Temperatures, and Applied Voltage

The SEL test was started with the heaviest ion available at 0° incident angle (0° being the beam perpendicular to surface of die) to establish the saturated or largest cross-sectional area. The lower energy (lighter) ions were to be selected in descending order, as available, until latchup was no longer observed (below the threshold of SEL).

The SEL testing was performed at two (2) different temperatures and maximum operating voltage as follows: ~35º C (ambient temp at “Room Temp” in the vacuum chamber), and 85º C (Hot Temp, as determined on the top outer surface of the package) with V_A = V_{DR} = OUTV = 2.0V. 85°C, as determined at the top outer surface of the package, was chosen because it is the maximum practical temperature that the part can be heated to on a demonstration board without the adhesive of the heaters melting and falling off the board. A previous experiment, comparing the thermistor temperature (located on the board, near the package) to the surface temperature of the top of the package with both channels running at 1GHz and at room temperature (ambient, ~35°C), found a 20°C rise at the top surface of the package from the reading of the thermistor (thermistor at 45°C and thermal probe touching the top surface of the package reading 65°C). Experiments have also determined that junction temperature runs at about 45°C to 55°C above ambient on the same board under the same conditions (junction temperature is at about 85°C when the top of the package is at 65°C). Therefore, at “Hot Temp”, the thermistor is at 65°C, the top surface of the package is at 85°C, and the junction temperature is at about 105°C. For these reasons, “Hot Temp” testing was performed with the thermistor running at about 65°C.

Testing was also performed at 35° incident angle, measured from a perpendicular to the surface, when needed to achieve an effective LET of approximately 120MeV/mg/cm^2.

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8.2 Power Up / Power Down and Testing Sequence

a) Set up test equipment/circuit, with DUT, and verify correct operation.
Initial Power Up Sequence:
1) Apply 2.0V to V_A and V_{DR} simultaneously
2) Apply Clock – 1GHz sine wave 600mVpp
3) Apply Waveforms to be sampled, (see section 8.0 for description), to both channels I and Q.
Subsequent Power Down Sequences:
1) Remove 2.0V from V_A and V_{DR} simultaneously (leave clock signal and inputs to channels I and Q applied and running).
Subsequent Power Up Sequences:
1) Apply 2.0V to V_A and V_{DR} simultaneously (leave clock signal and inputs to channels I and Q applied and running).
Final Power Down Sequence:
1) Remove 2.0V from V_A and V_{DR} simultaneously
2) Remove Clock – 1GHz sine wave 600mVpp
3) Remove Waveforms being sampled from both channels I and Q.

b) Check with facility’s personnel for correct ion, beam characteristics, energy, and flux. Ensure detectors are working properly.
c) Power up Device-Under-Test (DUT), using the “Subsequent Power Up Sequences” step above. Ensure it is operating properly.
d) Expose the DUT to the ion beam.
e) Record all pertinent data after exposure including if DUT latched-up or not.
f) Power down DUT using the “Subsequent Power Down Sequences” step above.
g) Repeat steps “b” through “f” for different energies and ion species.
h) Repeat steps “b” through “g” for samples #2 and #3.
i) Repeat steps “b” through “h” at 85°C (case temperature).
j) These procedures may be modified at the time of test, based upon the responses of the previous exposure results and test time remaining. A rough plot of cross section vs. LET on semi-log paper (cross section on logarithmic vertical axis, LET on linear horizontal axis) will be generated real time during testing to ensure accumulated data is making “sense”. If data is not making “sense”,

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re-evaluate and adjust test methods as needed. Take careful notes on why data isn't making "sense" and the adjustments that were deemed necessary.

k) Power Down as per "Final Power Down Sequence" above.

l) Upon completion, the data was analyzed and this final test report was generated.

8.3 Other Information Associated with Testing

a) Facility:
   1) Lawrence Berkeley National Laboratory
   2) 1 Cyclotron Road
   3) Berkeley, CA 94720

b) Test Method: EIA/JESD 57 – "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation", December, 1996

c) Sample Size: 3

d) Bias Voltage: $V_A = V_{DR} =$ OUTV = 2.0V.

e) Sampling Frequency: 1 GHz

f) Temperatures: ~35ºC (room temperature, no heat applied) and 85ºC (outer case temperature with heat applied).

g) Selected LET values, see figure 1 (page 9). The facility reserves the right to change this table. The actual "Cocktail" used was the 4.5MeV/nucleon "Cocktail" as per figure 1 with HeH^{+1}, B^{10}, Kr^{78}, Co^{59} not available, and Cu^{63} instead of Cu^{65}.

h) Ions used, see figure 1 (page 9) and the previous paragraph, (g).

i) Fluence: $1x10^2$ to $5x10^7$ ions/cm²

j) Flux: $1x10^2$ to $1x10^6$ ions/cm²·s

9.0 Test Facility, Dates, and Personnel

The test facility for the Single Event Effects testing is the 88" Cyclotron Facility at Lawrence Berkeley National Laboratory located in Berkeley, California. The 88"

Cyclotron provides heavy ion beams to perform SEE testing in a controlled environment. The facility generates ion beams for about a dozen different ion species at three energies per nucleon, 4.5MeV, 10Mev, and 16MeV. The 88" Cyclotron is located in Building 88 at 1 Cyclotron Road in Berkeley, CA.

Test Facility Personnel:

a) Peggy McMahan
Operations Supervisor
(510) 486-5980

b) Michael Johnson
Technical Support
(510) 486-4389

The testing was performed 0800 to 2000 on June 14 and 15, 0800 to 1600 June 16, 2006.

10.0 Test Equipment

a) Triple Power Supply
b) Oscilloscope with current probes
c) 3 Function Generators – Two Rohde Schwarz SME 03 (5Khz to 3 GHz) and HP 8662A (1280Mhz) . Note both Rohde Schwarz generators were configured for an external reference from the HP generator.
d) Lakeshore Temperature Controller, Model 332
e) Laptop Computer – Executes WaveVision 4 Software
f) 5 DVM's for monitoring Supply Voltages and Currents
g) ADC08D1000 Demonstration Boards & ADC08D1000 Development Boards with decapsulated parts (DUT's) already mounted on them.

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4.5 MeV/nucleon cocktail (HeH to Bi)

This cocktail, based on a tune of the ion source and Cyclotron using 40Ar+8, has an A/q ratio of 5 and energy of 4.5 MeV/nucleon. Typical components are shown in the table; the "standard" components are shaded. To achieve lower LET, boron can be added by special request. For even lower LET, HeH molecules can be accelerated; this requires a special tune-up. For an LET of 100 MeV/mg/cm2, Bi can be run at this energy, but requires advance notice and the AECR-U ion source.

Ion	Energy (MeV)	LET# (MeV/ mg/cm^2	Range in Si# (μ)
HeH^{+1*}	18., 4.5	0.26,.064	180.,179.
$^{10}B^{+2}$	45.	1.64	79.
$^{15}N^{+3}$	67.	3.09	67.
$^{20}Ne^{+4}$	90.	5.77	53.
$^{40}Ar^{+8}$	180.	14.3	48.
$^{59}Co^{+12}$	266.	27.31	43.
$^{65}Cu^{+13}$	293.	29.89	44.
$^{78}Kr^{+15}$	325.	39.54	41.
$^{86}Kr^{+17}$	378.	39.24	47.
$^{136}Xe^{+27}$	603.	68.83	48.
$^{209}Bi^{+41}$	940.	99.64	54.

LETs and ranges calculated using SRIM2003
* After break up in target or a scattering foil.

Figure 1 – 4.5MeV/nucleon Table

Table 1 – Test Log

Date: 06/14/2006
Facility: Lawrence Berkeley National Laboratory
Product Type: ADC08D1000WG-Q/QV
DUT's: ADC08D1000 Demonstration Boards with DUT #1A (Runs 1 – 7), #2A (Runs 8 - 16), #3A (Runs 17 – 27)

Run #	Spec -ies	Incident Angle	Effective LET MeV/ mg/cm^2	Flux #/ cm^2*s	Effective Fluence #/cm^2	# Events Latchup	Va Currrnt mA	Vdr Current mA	Δ (diff) Latchup Current mA	Applied Voltage (V)	Temp. °C @ therm.	Total Effective Fluence #/cm^2	Cross Sec-tion cm^2	Accumul-ated (note 1) Ionizing Dose(rads)
1	Bi^{209}	0°	99.85	2E4	1.00E7	0	698	365	NA	2.0	41.5			15.976E3
2	Bi^{209}	0°	99.85	2E4	1.01E7	0	698.5	365.2	NA	2.0	41.4			32.11176E3
3	Bi^{209}	0°	99.85	9E4	1.01E7	0	707	369	NA	2.0	41.4	3.02E7	0	48.24752E3
4	Bi^{209}	35°	121.89	8E4	1.01E7	0	708.5	368.1	NA	2.0	42.6			64.38328E3
5	Bi^{209}	35°	121.89	8E4	1.01E7	0	693	360	NA	2.0	42.2	2.02E7	0	80.51904E3
6	Bi^{209}	35°	121.89	2E5	1.03E7	0	702.9	331	NA	2.0	65.0			96.97432E3
7	Bi^{209}	35°	121.89	1E5	2.84E7	0	702.9	331	NA	2.0	65.0	3.87E7	0	142.34616E3
8	Bi^{209}	0°	99.85	1E5	1.09E7	0	711.6	328.2	NA	2.0	38.4			17.41384E3
9	Bi^{209}	0°	99.85	1E5	1.01E7	0	711	328	NA	2.0	40.1			33.5496E3
10	Bi^{209}	0°	99.85	1E5	1.01E7	0	711	328	NA	2.0	41.2	3.11E7	0	49.68536E3
11	Bi^{209}	35°	121.89	Run	Halted		operator	error	Attenuat	-ors left	In	place		49.68536E3
12	Bi^{209}	35°	121.89	1E5	1.01E7	0	712	327	NA	2.0	41.4			65.82112E3
13	Bi^{209}	35°	121.89	1E5	1.02E7	0	712	327	NA	2.0	42.6			82.11664E3
14	Bi^{209}	35°	121.89	1E5	1.02E7	0	711	327	NA	2.0	42.5	3.05E7	0	98.41216E3
15	Bi^{209}	35°	121.89	1E5	1.01E7	0	718	326	NA	2.0	63.7			114.54792E3
16	Bi^{209}	35°	121.89	1E5	1.01E7	0	716	325	NA	2.0	63.8	2.02E7	0	130.68368E3
17	Bi^{209}	35°	121.89	1E5	1.01E7	0	704.6	321.9	NA	2.0	45.0			16.13576E3
18	Bi^{209}	35°	121.89	1E5	1.01E7	0	704.3	322.3	NA	2.0	43.9			32.27152E3
19	Bi^{209}	35°	121.89	1E5	1.06E7	0	704	322	NA	2.0	43.1	3.08E7	0	49.20608E3
20	Bi^{209}	0°	99.85	1E5	1.61E7	0	705	322	NA	2.0	43.5			74.92744E3
21	Bi^{209}	0°	99.85	1E5	1.01E7	0	704	322	NA	2.0	43.0			91.0632E3
22	Bi^{209}	0°	99.85	1E5	1.11E7	0	704.2	322.3	NA	2.0	43.3	3.73E7	0	108.79656E3
23	Bi^{209}	0°	99.85	1E5	1.01E7	0	710.3	325.0	NA	2.0	62.9			124.93232E3
24	Bi^{209}	0°	99.85	1E5	1.10E7	0	710.5	324.2	NA	2.0	64.5	2.11E7	0	142.50592E3
25	Bi^{209}	35°	121.89	1E5	1.04E7	0	710.7	324.5	NA	2.0	64.5			159.12096E3
26	Bi^{209}	35°	121.89	1E5	1.05E7	0	710.4	324.7	NA	2.0	64.9			175.89576E3
27	Bi^{209}	35°	121.89	1E5	1.02E7	0	711.5	324.2	NA	2.0	65.1	3.11E7	0	192.19128E3

Table 2 – Test Log

Date: 06/14/2006
Facility: Lawrence Berkeley National Laboratory
Product Type: ADC08D1000WG-Q/QV
DUT's: ADC08D1000 Demonstration Board with DUT #39 (Runs 28 – 34)
(Previous version of silicon)

Run #	Spec -ies	Incident Angle	Effective LET MeV/ mg/cm^2	Flux #/cm^2*s	Effective Fluence #/cm^2	# Events Latch-ups	Va Current mA	Vdr Current mA	Δ (diff) Latchup Current mA	Applied Voltage (V)	Temp. ℃ @ therm.	Total Effective Fluence #/cm^2	Cross Section cm^2	Accumul (note 1) Ionizing D.(rads)
28	Cu^{63}	0°	30.04	2E4	1.04E7	0	701	325	NA	2.0	40.0			4.999E3
29	Cu^{63}	0°	30.04	2E5	7.24E6	1	705	323	7mA-Va	2.0	41.4			8.478E3
30	Cu^{63}	0°	30.04	2E5	3.63E6	1	705	324	61mA-Va	2.0	41.4	2.127E7	9.403E-8	10.223E3
31	Ar^{40}	0°	14.33	1E5	3.71E5	1	706	325	10mA-Va	2.0	43.0			10.308E3
32	Ar^{40}	0°	14.33	1E5	4.34E6	1	706	324	62mA-Va	2.0	43.2			11.303E3
33	Ar^{40}	0°	14.33	1E5	3.99E6	1	706	324	10mA-Va	2.0	43.1	8.701E6	3.448E-7	12.218E3
34	Ne^{20}	0°	5.76	2E5	3.64E7	0	706	324	NA	2.0	43.6			15.573E3

Note 1: Accumulated Ionizing Dose is an estimate of the worst case bound according to annex B of EIA/JESD57. The large Z (number of protons) species used in this testing lose their energy and stop rather quickly in Si (although the depth vs. LET curve of all the species used showed that the rapid drop off of LET and the penetration depth was well below the epitaxial layer and into the substrate, that is well below the active circuitry and associated parasitics). The formula given in annex B of EIA/JESD57, 1.6E-5*LET*Fluence, with LET in MeV/mg/cm^2, and Fluence in ions/cm^2, assumes that the LET of the species does not decrease and the ion flux continues on through the Si undiminished. Thus, the accumulated ionizing dose presented in the last two tables is certainly an over estimate, and the over estimate gets worse with as Z gets larger. Certainly for Bi209, these figures are greatly over estimated. Preliminary total ionizing dose testing per method 1019.7 of MIL-STD 883G on this product has shown that the performance of the part does not appreciably degrade until approximately 100Krad(Si) total ionizing dose (Co60 gamma rays). Through out the testing the performance of the DUT's with checked with WaveVision4 software (developed by National Semiconductor Corp.) and no degradation of performance was observed on any of the DUT's that would indicate a total ionizing dose equivalent to 100Krad (Si) by Co60 gamma rays was reached.