Particle Test of Xilinx Virtex-II FPGA using XTMR Mitigation Technique

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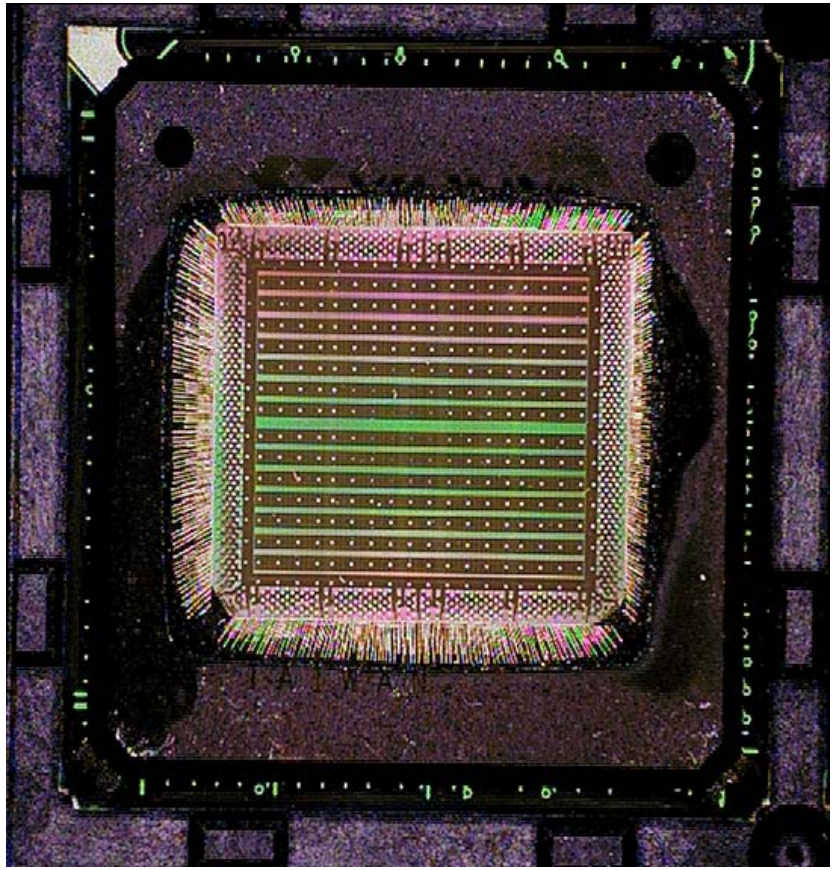
Purpose

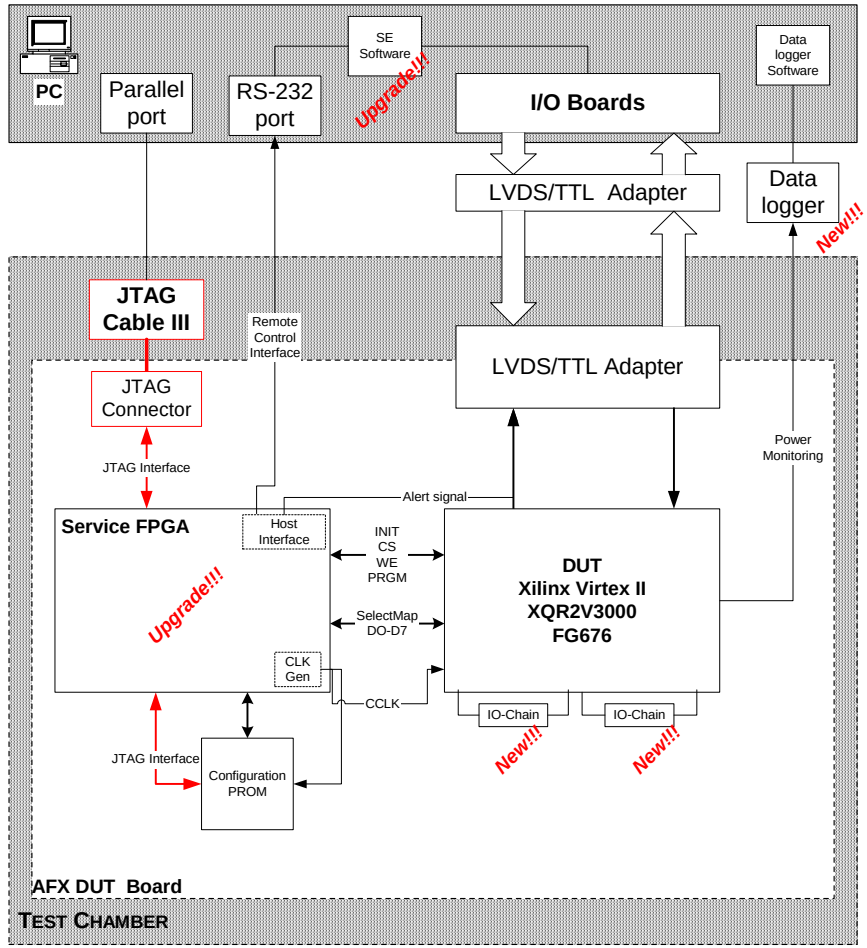


- Test Mitigation with Xilinx TMR Tool (XTMR)
- Test IO mitigation concepts
- SEE Characterization

- Test Vehicle
  - XilinxVirtex-II XQR2V3000 plastic FG676

Test Setup

- In situ testing
  - Functional testing
  - Recording SEU in Configuration memory
  - Power Monitoring
- Mitigation
  - All logic triplicated with XTMR tool
  - All inputs triplicated
  - Triple/double voted outputs
  - Continuously re-writing of configuration memory - “Scrubbing”
  - Detection scheme for known SEFIs
    - POR SEFI
    - CRC SEFI
    - FAR SEFI
  - Clocking of TCK input + ground TRST (avoid JTAG SEFI)



One Design Tested

Included test modules:

- Application like (FFT algorithm)
- Simple Shift register (FFmatrix)
- LUT intensive circuit (LUTmatrix)
- MULT18x18 circuit (M18matrix)

All modules are about equally sized in aspect of recourse usage

+ IO-test circuits

Resource usage (XTMR):

- 30% of all FF
- 96% of all LUT
- 87% of all 18-bit Multipliers
- 52% of all IOBs (LVCMOS)
- No BRAM or DCMs

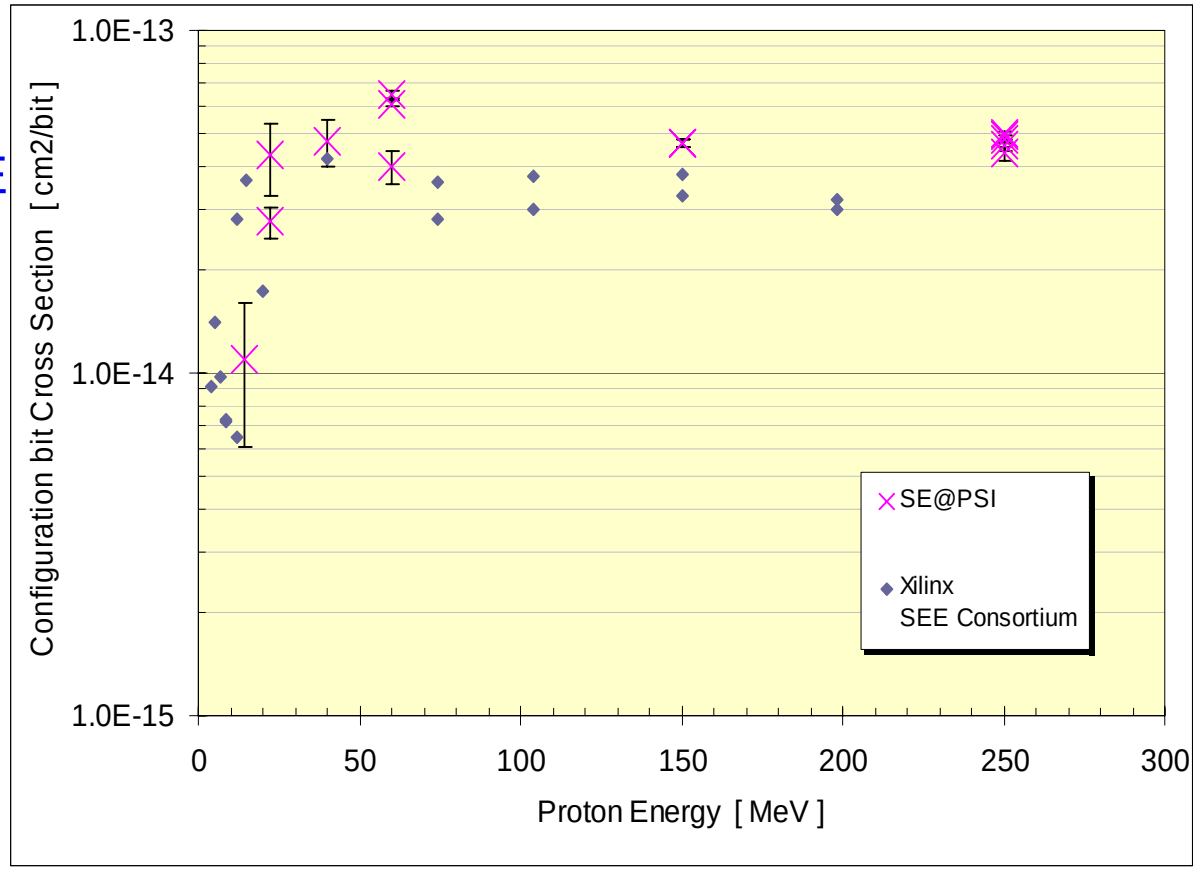
Protons Results

PSI, Switzerland

SEU - Configuration Memory Bits

Configuration bit
cross section from
(SE@PSI) and Xilinx SEE
Consortium
(G. W. Swift, Jan 2004)

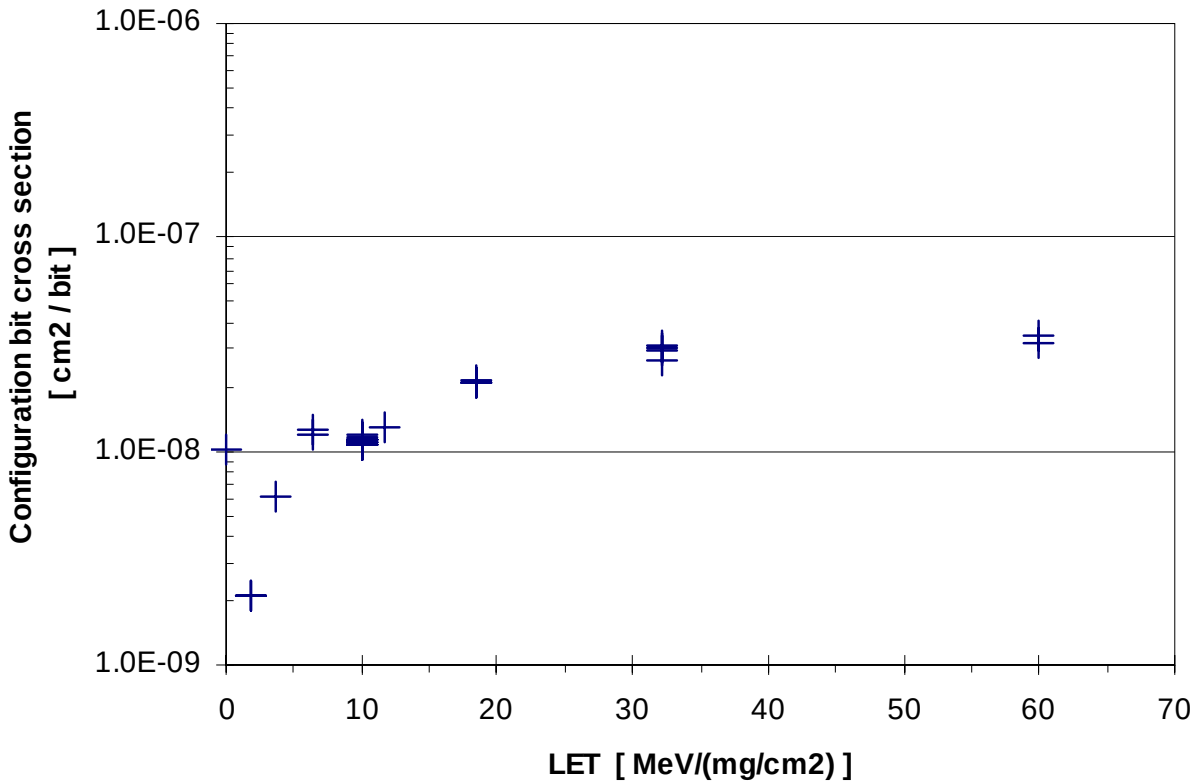
Onset:
~20 MeV
Qsat:
~5E-14 cm2/bit



Heavy Ion Results
RADEF, Finland

SEU - Configuration Memory Bits

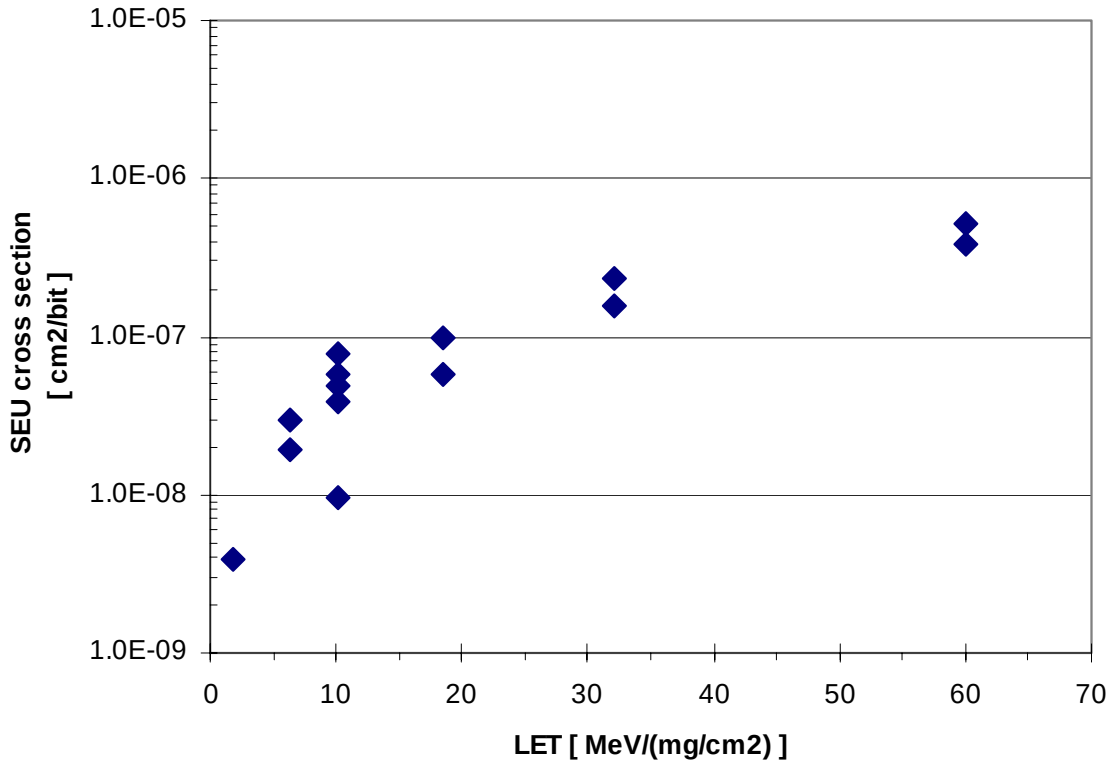
LETth:
~2 MeV-cm2/mg
Qsat:
~3E-8 cm2/bit



Heavy Ion Results
RADEF, Finland

SEU – User logic Flip-Flops

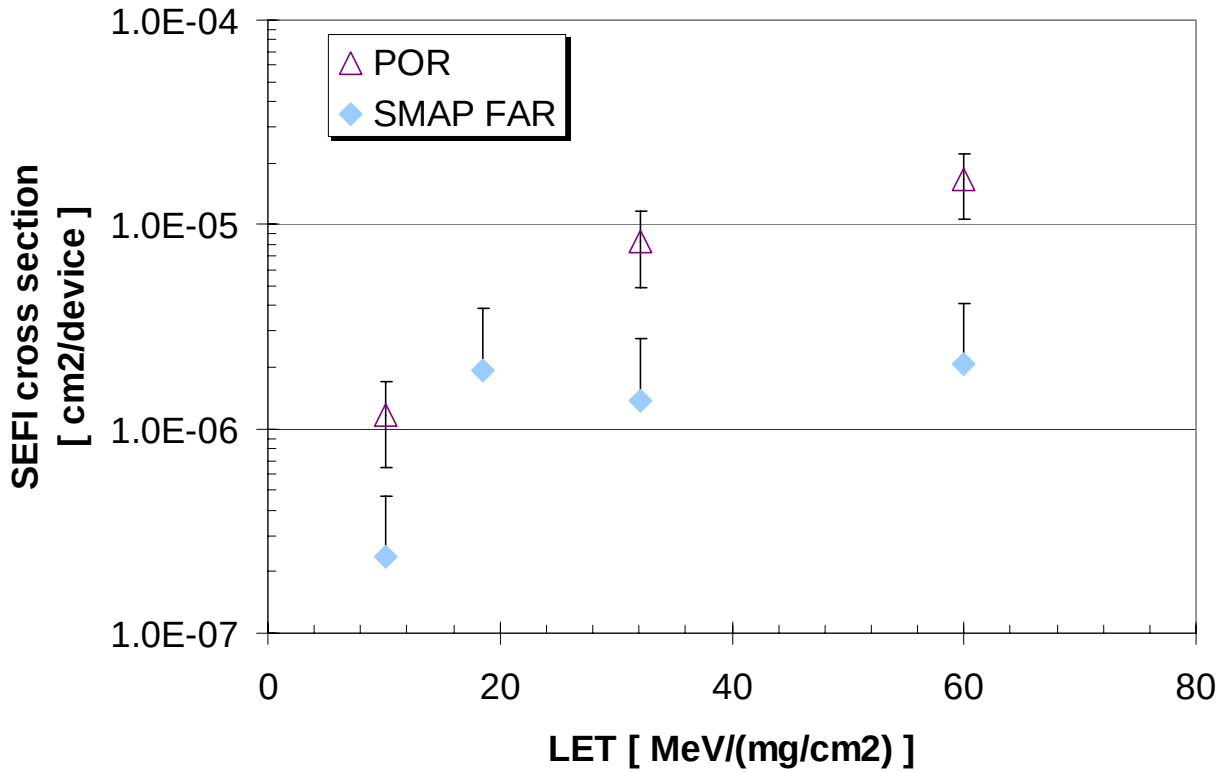
LETth:
~5 MeV-cm2/mg
Qsat:
~5E-7 cm2/bit



Heavy Ion Results
RADEF, Finland

SEFI – Functional Interupts

LETth:
~10 MeV-cm2/mg
Qsat:
~1E-5 cm2/device

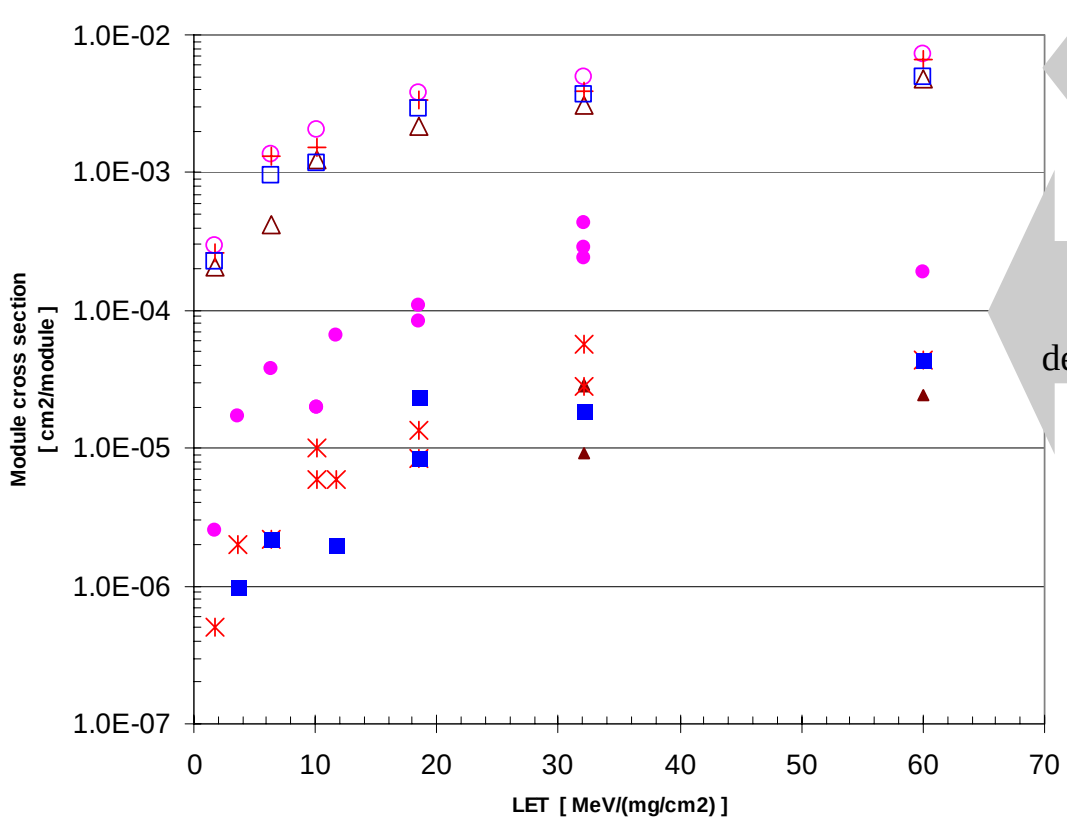


Functional Errors with XTMR (Low Flux Results)

Heavy Ions at RADEF, Finland

XTMR reduce error rate ~100 times

BUT errors with XTMR show flux dependence



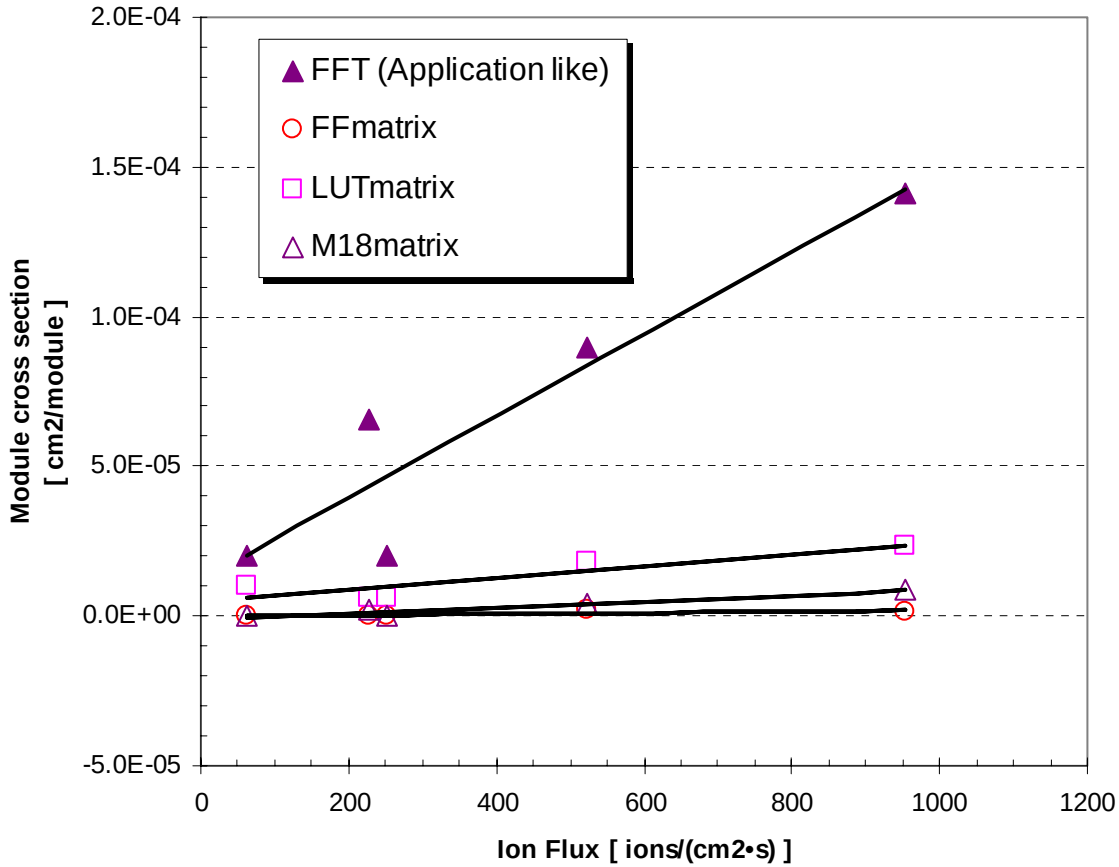
Flux dependence

Heavy Ions at RADEF, Finland

- **Module dependent**
  = Design dependent

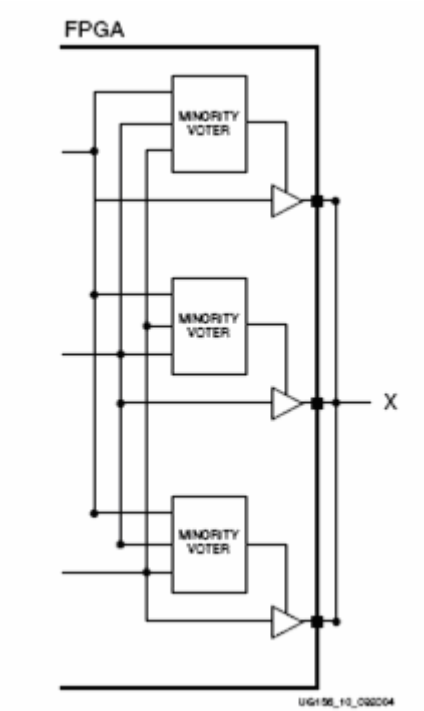
- **Explanation:**
  - **Many upsets in each scrub cycle take out the mitigation scheme**

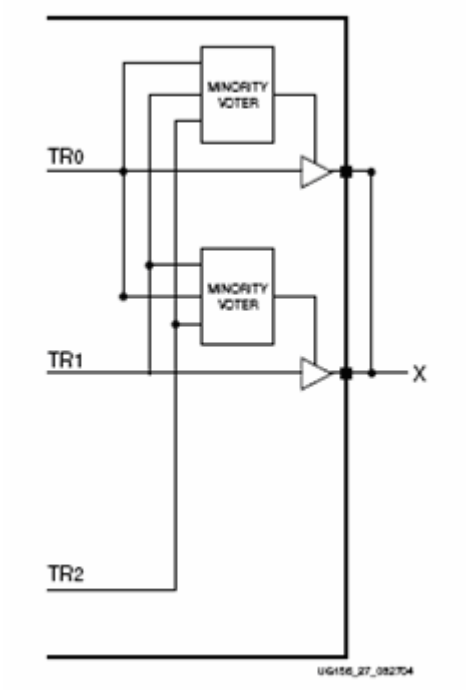
- This is a test artifact
  - Flux high compared to scrub rate



IO Mitigation Concepts

available with Xilinx TMR tool





Triple-Voted Outputs

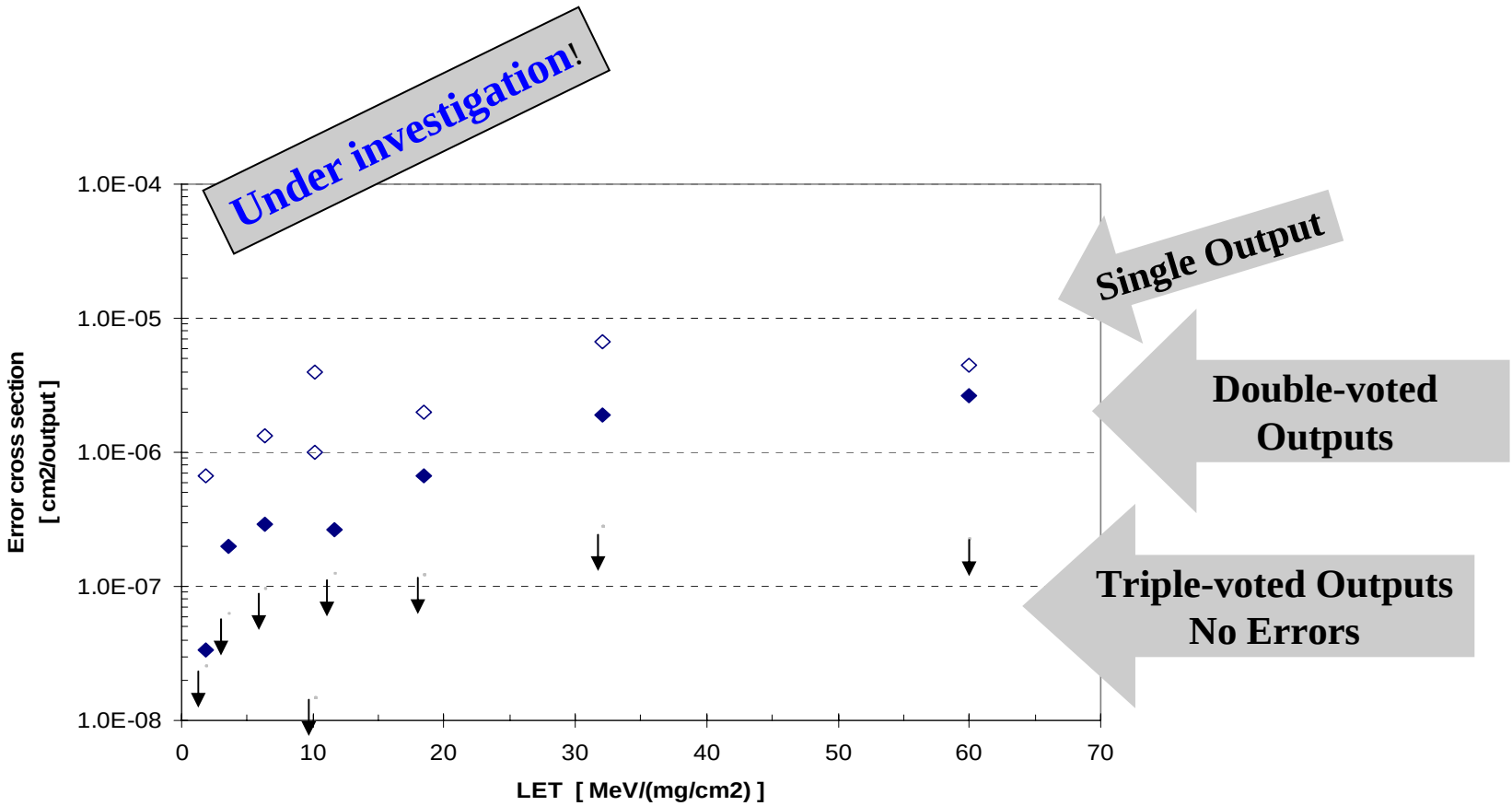
- 3 IOs hardwired on PCB with internal voting circuits

Double-Voted Outputs

- 2 IOs, instead of 3
- Save IOs
- In theory equal SEU protection as Triple-voted

Results - IO Mitigation Concepts

Heavy Ions at RADEF, Finland



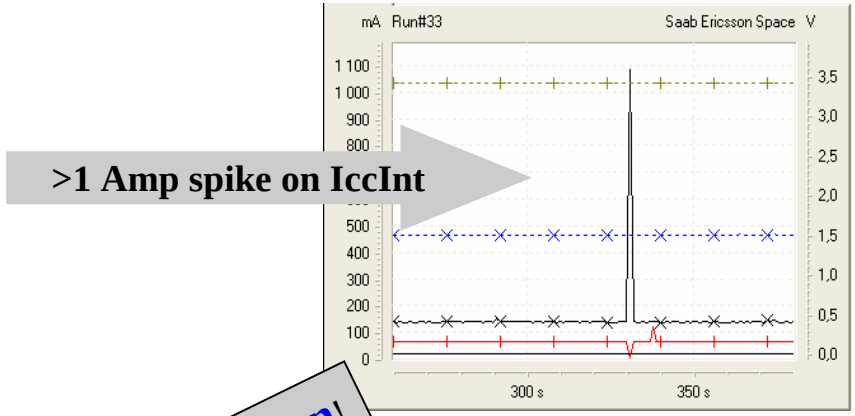
”Dead lock” events

Heavy Ions at RADEF, Finland

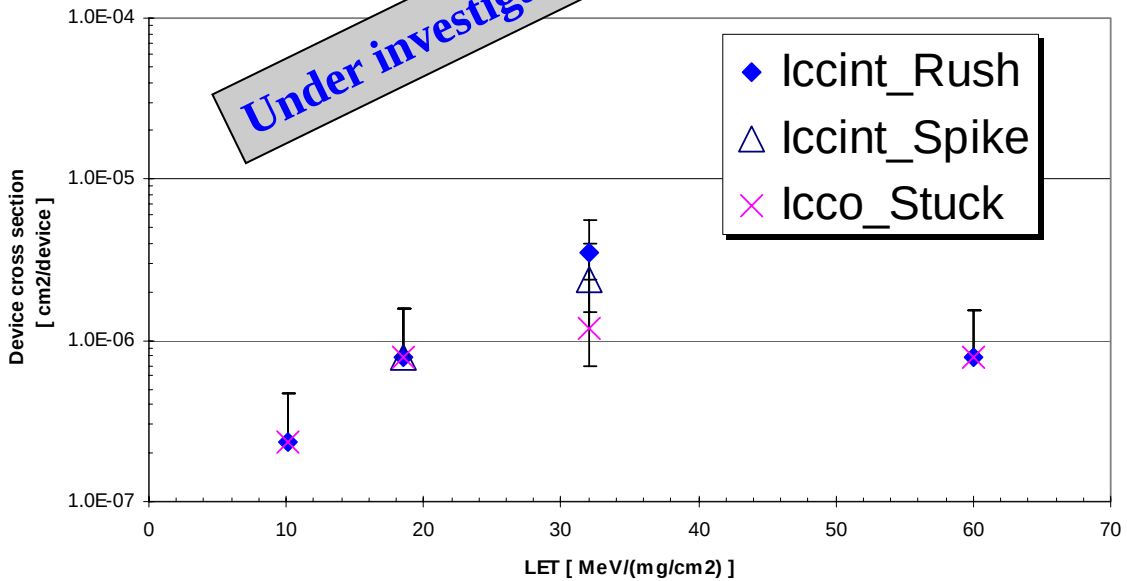
Latch-up Like Events

- Required Power Cycling to recover test system

Limitation of the power supply in the test system, prevented us to fully characterize these events



>1 Amp spike on IccInt

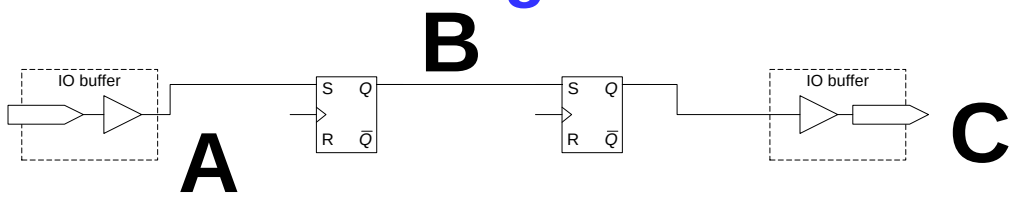


Conclusion

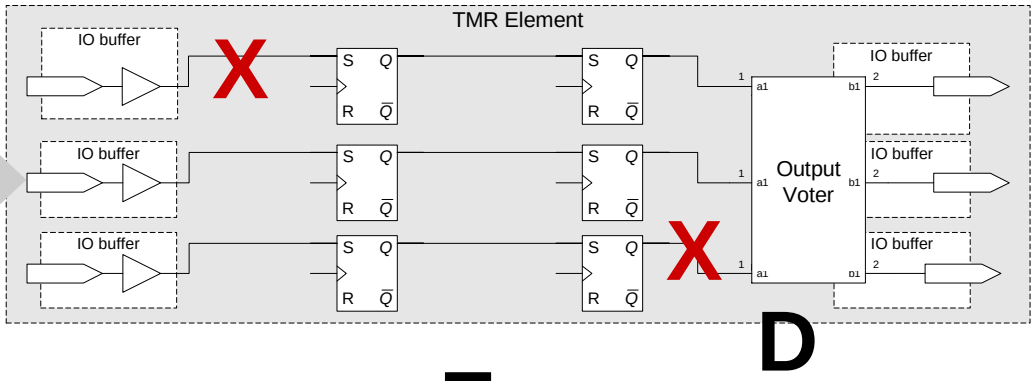
- **Applications will need SEU protections like**:
  - Continuously Scrubbing of Upsets in Configuration Memory
  - Careful Selection of Scrubbing Rate (Cfg upsets / scrub cycle <<1)
  - XTMR (to reduce upset rates)
  - SEFI Detection and/or Watch Dog Circuitry
  - Clocking of TCK input + ground TRST (avoid JTAG SEFI)
- **SEE Test Results are Design Dependent**,
  - Consider “Low Flux” SEE Test
- **Consider Pre-Cautions Like**:
  - Use Triple-voted outputs instead of Double-Voted output (or re-test)
  - Use over current recover circuit (or re-test with the same configuration as in your application)

LESSONS LEARNED
Flux dependence is a test challenge

No XTMR

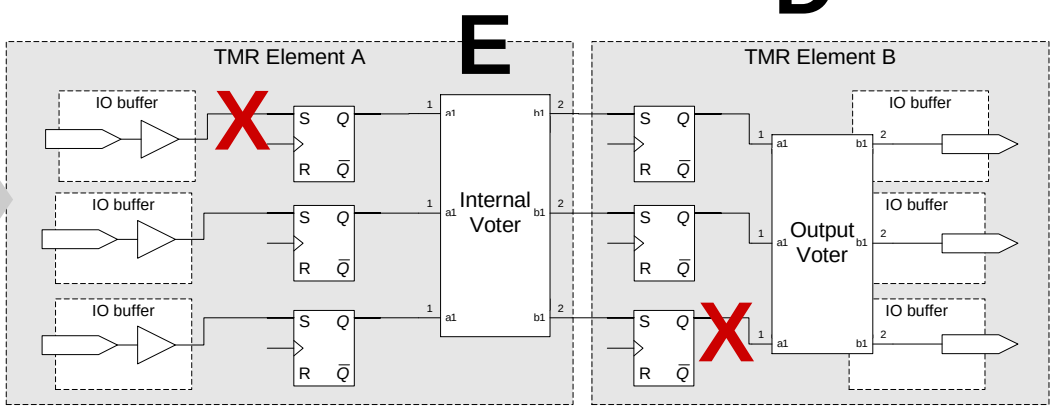


Standard XTMR flow



ERROR

Fixed XTMR flow (reduce flux dependence)



OK

LESSONS LEARNED
Flux dependence is a test challenge

The fixed XTMR dramatically reduced the flux dependence compared to standard XTMR flow

However, this is nothing you want to do if you perform a validation test on flight applications

The application like module (FFT) indicates that the flux dependence increase with complexity

VERY LOW FLUX MUST BE USED!!!