FPGAs for Space
- an overview

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Outline

- FPGAs available today
- Comparing radiation performance
- Upcoming
- What do we miss & Some rare effects
- Conclusion

This is a comprehensive summary. Presented data is taken from presentations, papers and other sources.The data can only be used for orientation purpose.

Main FPGA Vendors for Space

➢ European	➢ US
One time programmable	
	▪ Aeroflex/UTMC ▪ Actel
SRAM based	
▪ Atmel	▪ Xilinx ▪ Honeywell (RHrFPGA, Not for sell?)
Flash based	
	▪ Actel *in development*

FPGA devices for Space

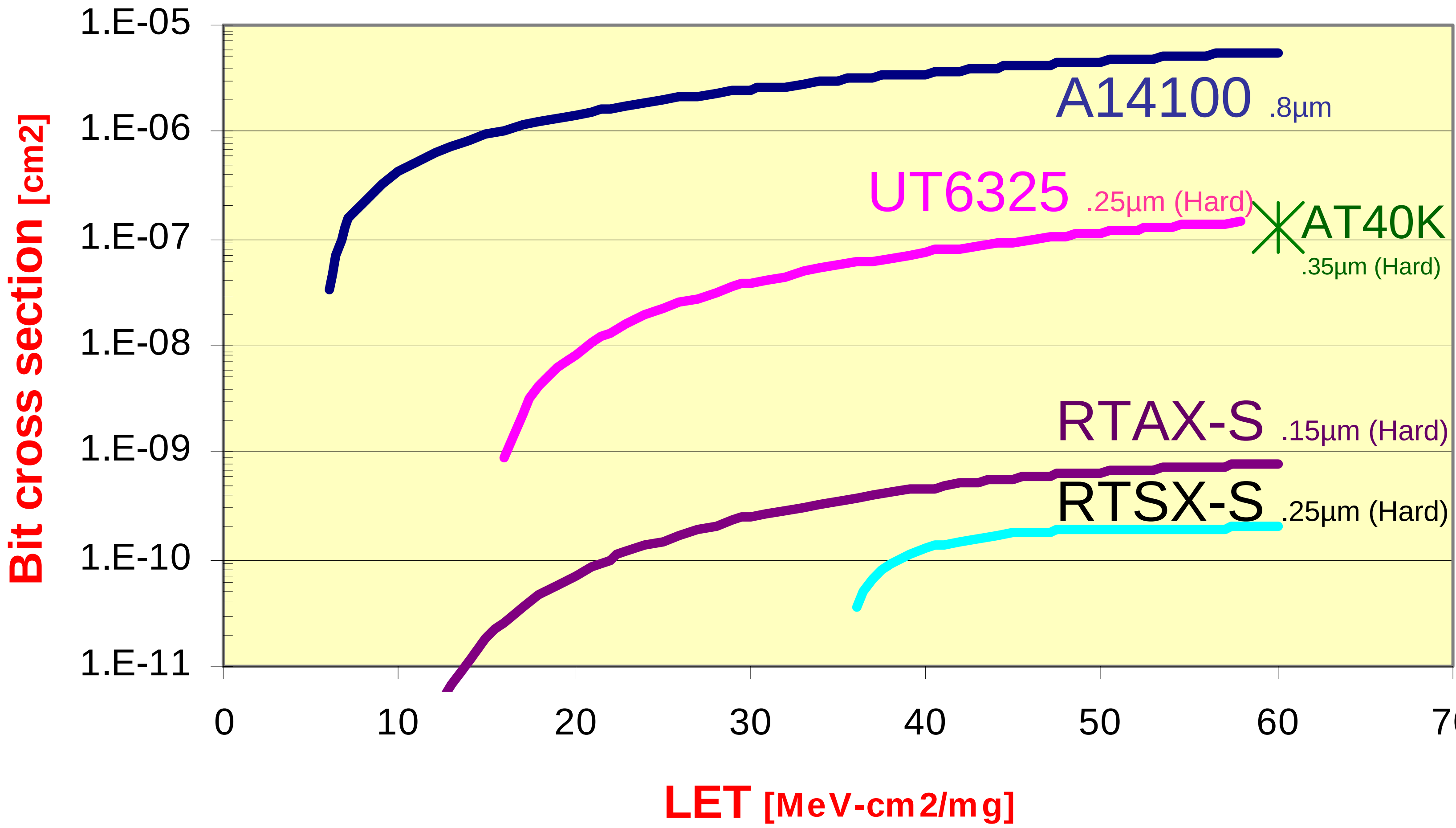
Red cursive not available yet (planned 2007)

Vendor	Family	Parts	Packages	Max IOs	RAM	FF	Logics	Others
Atmel	AT40K 0.35 µm	AT40KEL040 AT40KFL040	MQFPF160, MQFGF256	233	18 k	3 k	2,3 k	5V tolerant I/O
	ATF280E *0.35 µm*	*ATF280E*	MQFGF256 MCGA472	*308+*	*115 k*	*14 k*	*28 k*	*Cold soare*
Aeroflex/UTMC	Eclipse 0.25 µm	UT6325	CQ208, CQ288 CLGA484	310	55 k	3,1 k	1,5 k	
Actel	Act 3 0.8 µm	RT14100	CQ256	228	None	0,7 k	1,4 k	5V I/O
	RTSX-SU 0.25 µm	RTSX32-SU RTSX72-SU	CQ208, CQ256 CCGA624 CCLG256	224 353	None	1,1 k 2 k	1,8 k 4,0 k	3,3V & 5V I/O
	RTAX-S 0.15 µm	RTAX250S RTAX1000S RTAX2000S RTAX4000S	CQ84,CQ208, CQ256, CQ352 CCGA624, CCGA1152,CCGA1272	248 516 684 840	54 k 162 k 288 k 553 k	1,4 k 6,0 k 10,8 k 20,2 k	2,8 k 12,1 k 21,5 k 40,3 k	
Xilinx	Virtex-2 0.15 µm	XQR2V1000 XQR2V3000 XQR2V6000	FG458, BG575, BG728 CG717, CF1144	328 516 824	720 k 1,7 M 2,6 M	10.2 k 28,7 k 67,6 k	11.5 k 32,3 k 76,0 k	8-12 DCM 40-144 Multiplier blocks
	Virtex-4 *90 nm*	*XQR4VLX200* *XQR4VSX55* *XQR4VFX60* *XQR4VFX140*	*CF1144, CF1509*	*960* *640* *576* *768*	*6,0 M* *5,8 M* *4,2 M* *9,9 M*	*178 k* *49 k* *51 k* *126 k*	*200 k* *55 k* *57 k* *142 k*	*DCM, PMCD, PowerPC, DSP, RocketIO*

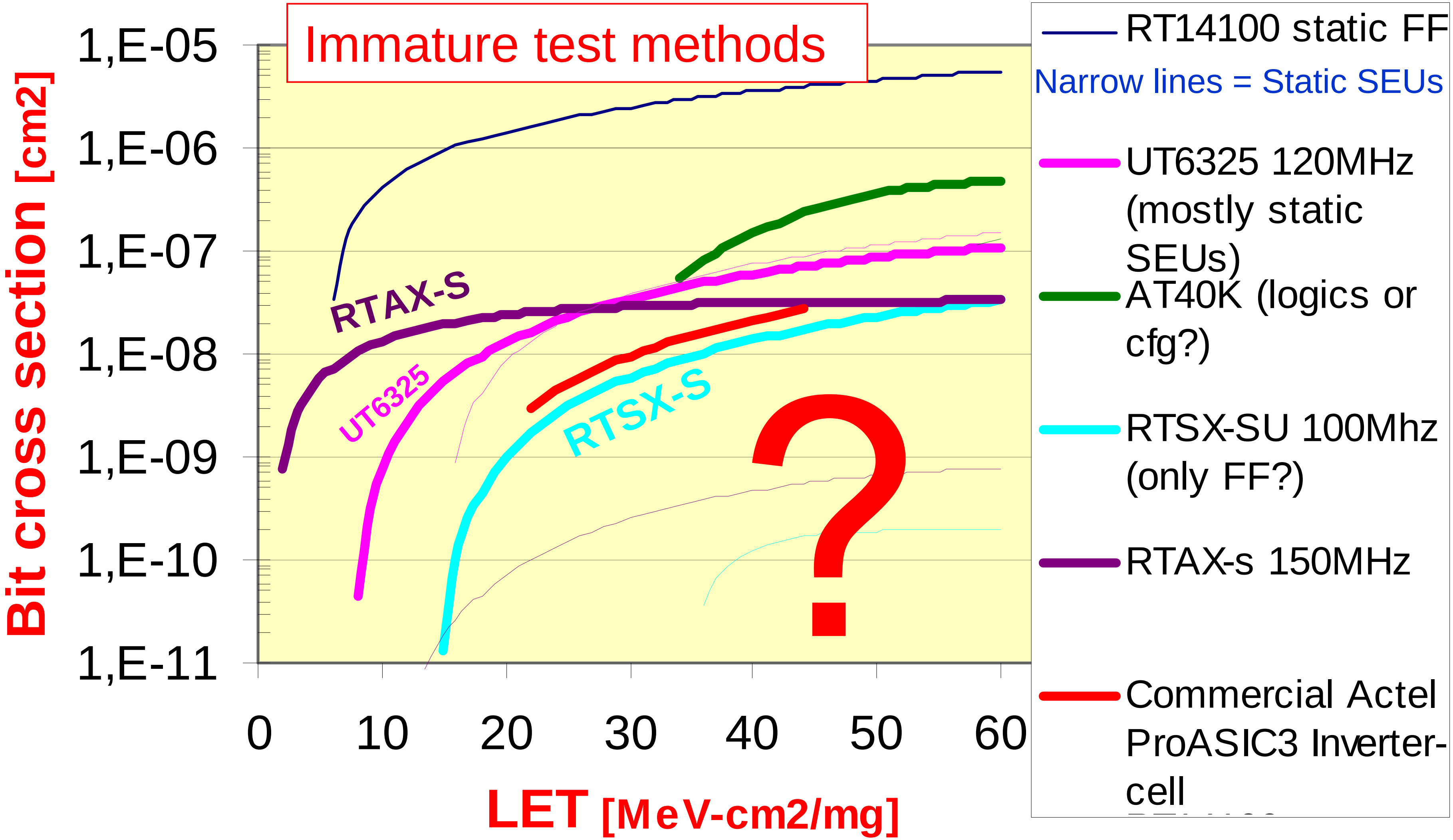
Comparing radiation performance

- All FPGAs address TID and SEL reasonable well
- Heavy ion data primary covers
  - Static SEU – User flip-flop
  - Dynamic SEU (SET)
  - Static SEU – User RAM
- Proton data available for some devices but not all

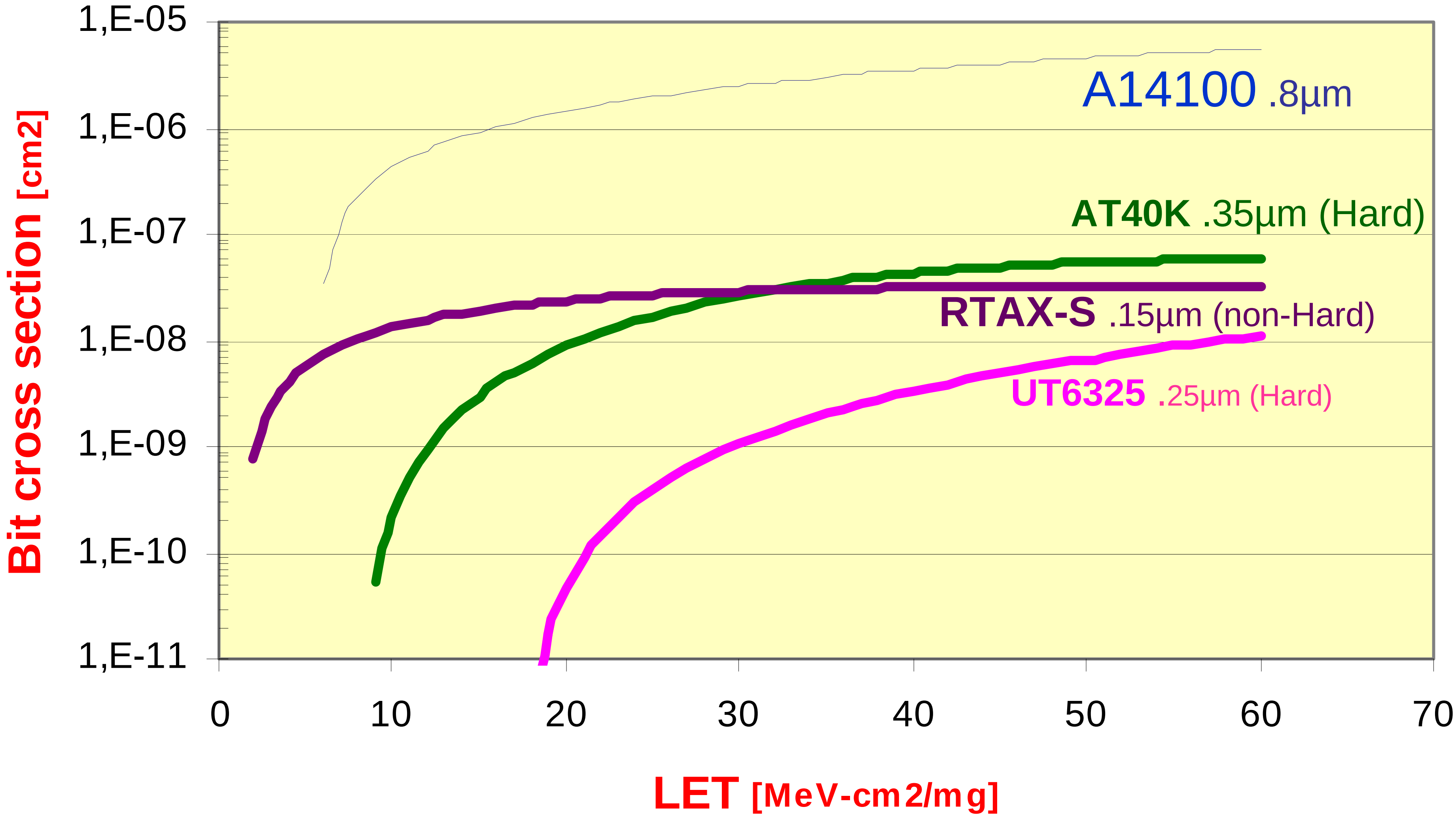
Radiation Performance
Static SEU – User Flip Flops



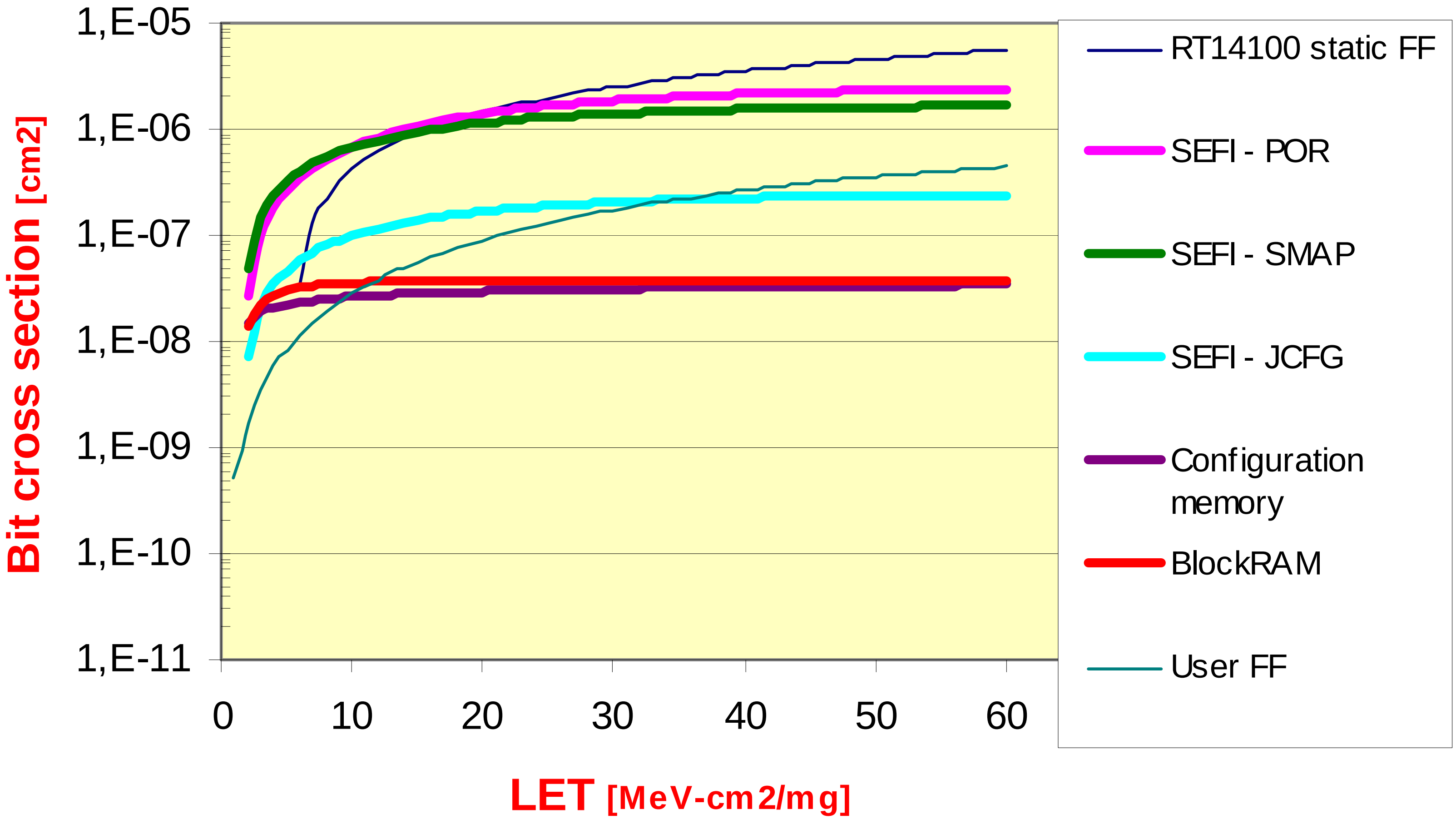
Radiation Performance
Dynamic SEUs - In circuitry Transients (SET)



Radiation Performance
Static SEU – User RAM



Radiation Performance
Static SEE – Xilinx Virtex-II



Add to this, a lot of papers and ongoing work in:

Dynamic testing, Fault injection and mitigation schemes

Upcoming

- 2007
  - Xilinx Virtex-4 devices available
    - Test on commercial die promising, similar to Virtex-II
    - Radiation test planed on rad tolerant die next month
    - Multi upsets might be an issue for XTMR mitigation
  - Atmel ATF280 in fab, radiation test planned before summer.
  - Actel RTAX4000-s now available

- 2008 and later
  - Xilinx works on SIRF FPGA
    - radiation hard re-configurable FPGA.
  - Actel plan to sell ProASIC-3 as RT (no hardening)
    - Expected 2008.
    - Radiation testing is ongoing.
    - Aims for low earth and short missions, No ITAR.
  - Actel works on radiation hard flash based FPGA
    - ProASIC-G4.
    - Expected 2010-2012
  - UTMC/Aeroflex might go for next generation FPGAs

What do we miss? (1/2)

- Proton test data for:
  - Actel RTAX-S
    - Dynamic SEE (LETth ~10 MeV-cm2/mg)
    - SEU RAM
  - Actel RTSX-SU, Dynamic SEU (LETth ~15 MeV-cm2/mg)
  - Atmel AT40K, SEU configuration data (LETth ~10 MeV-cm2/mg)
- Heavy ion test data for:
  - Atmel AT40K; SEU user flip-flops
    - only data taken at 56 MeV-cm2/mg,
    - Atmel expect LETth similar to RAM-cells (~15MeV-cm2/mg)

What do we miss? (2/2)

- Better testing methods for Dynamic SEUs (SET):
  - The data available today is not conclusive
  - Not possible to transfer data to an application design.
- SEU/Memory mapping of RAMs and configuration memories
- TID Testing with characterisation of power up behavior
  - Power up failures observed for Actel A14100 and Xilinx Virtex-1
  - Power up is critical for FPGAs
- Independent Radiation testing
  - Most given data is coming from the manufacturers

Some Rare Effects

Things they never talk about

- Multibit upsets (MBU):
  - Observed for Actel RTAX-s RAMs
    - Need to be addressed for mitigation schemes?
  - Observed for Xilinx Virtex-2 and Virtex-4
    - Need to be addressed for XTMR mitigation?
- SEDR (Single event Dielectric Rupture)
  - Observed for all Actel antifuse FPGAs at high voltage and LET
- TID
  - Actel RTSX32-SU show temporary functionality loss at~60 krad
    - Actel states it is a test artifact due to high dose rate. This has not been confirmed in test.
- Rare Multi events
  - Observed in SEU testing by Actel at high LET
    - Effect is taken for ”facility noise”, which is nonsense.

Conclusion

- All FPGAs address TID and SEL reasonable well
- A full spectra of SEE performance, from almost SEE free to very SEE sensitive
  - Case by case must decide whether mitigation schemes is needed or not and to which extent.
- Dynamic SEUs (SET) must be considered
  - It is reasonable to assume that critical high speed applications in the future always will need to address some kind of mitigation.
- Today and upcoming FPGAs are very complex
  - Accelerator testing on test designs can only be used as guidelines
  - Flight applications are recommended to be validated in accelerator