Radiation Testing of AMI 0.35 um and UMC 0.18 um – Radiation Tolerant and Normal Layout Devices.

TEC-QCA Support Activity to ESA Projects.

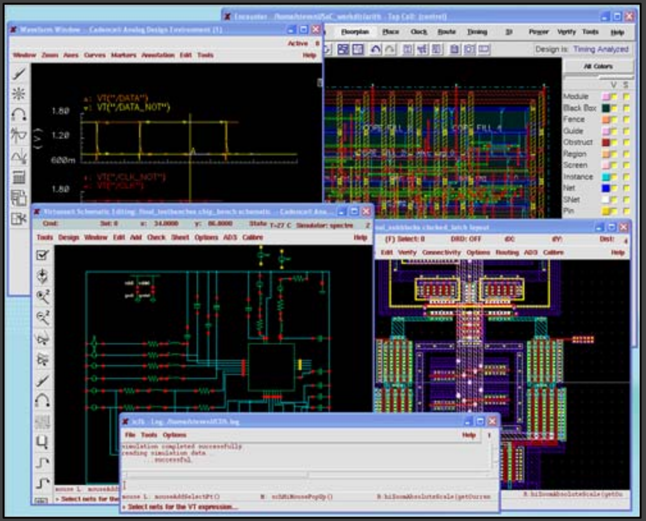
In collaboration with IMEC (Be)

SRON
Netherlands Institute for Space Research

Presentation overview

- Introduction
  - Background research
- Test goals and setup
  - Test goals
  - Measurement theory
  - Test setup / procedure
- Test results
- Conclusions and future research

Institute and group overview



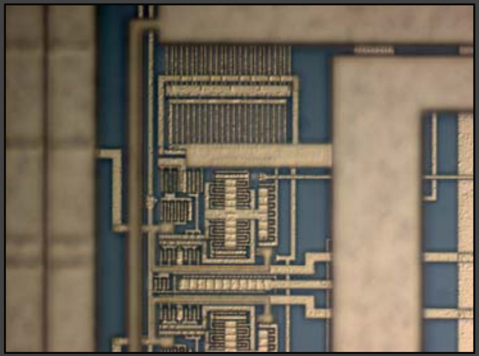
SRON total: ±200FTE
Engineering and science

IC Design group size:

- 4 fulltime mixed signal ASIC designers
- ±2 master students
- ±2 fte effort total digital design, testing, …

Group core competences:

- System level trade offs and optimization
- Mixed signal front end IC design
  - Analog design
  - Digital design & synthesis
  - Mixed signal integration / advanced tooling



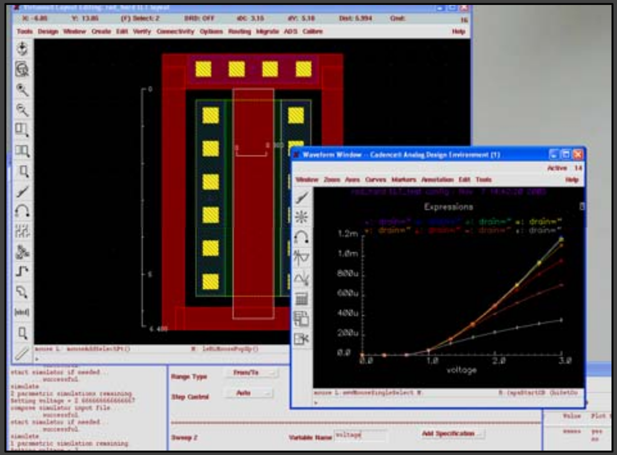
Motivation for radiation testing

SRON develops high performance front end electronics

- A/D and D/A conversion with resolutions >20bit at very low frequencies (1mHz-10Hz bandwidth)
- Readout of X-Ray sensor arrays: 12-16bit A/D and D/A plus digital demodulation

- *Currently digital radiation tolerant circuits do exist (DARE)*
- *Analog circuits are designed using guidelines and trial and error*

  ➔ *No systematic approach for the design of high performance mixed-signal miniaturized electronics available*



- **Evaluate radiation effects on test structures (provided by IMEC)**
- **Research analog parameter degradation**

Target technologies

- Mixed signal design trade off:
  - Larger features sizes benefit:
    - Large signal swing → large ($V_{dd} – V_{th}$) [V]
    - Linear behaviour → large overdrive (V_{gs}-V_{th}) [V], analog components (C_{PP},R_{poly})
    - Low off current switch → high V_{th} [V]
  - Smaller feature sizes benefit:
    - High gain → high C_{OX} [F/μm^2]
    - Good matching → small t_{ox} [m]
    - High speed → lower capacitance minimum device [F]
    - Digital power & density → Digital scaling advantages

Based on SRON application roadmap, optimal trade off estimated to be for 0.18μm, 0.25μm or 0.35μm technologies

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Test goals

- Investigate total dose effects on analog parameters for AMI Semiconductor 0.35µm and UMC 0.18µm test devices:
  - Threshold voltage V_{th}
  - Transconductance g_m
  - Current factor β

- Compare several types of devices:
  Regular layout, Embedded Layout Transistors (ELT) and novel Rectangular Edgeless Transistors (RET)

- Compare performance of technologies and scaling effects

- Estimated device performance in space environment conditions, i.e. total dose in the order of 100kRad(Si)

- Measure online to investigate parameter shift relation with dose

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Measurement theory (I)

Measure I_d versus V_{gs} characteristics and determine parameters as proposed in *"Assessment of the merits of CMOS technology scaling for analog circuit design"* by Vertregt and Scholtens 2004.

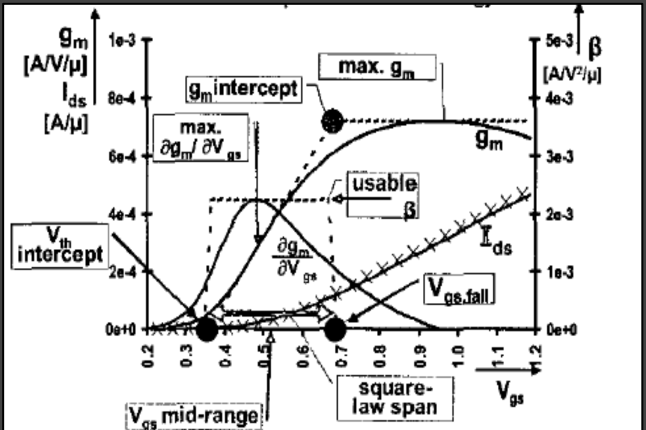


Figure 1 Key device property estimation for circuit design (at V_{ds}=0.5V, V_{sb}=0V)

From Vertregt and Scholtens 2004

Do not use:

- Constant current / unit width biasing
  → degradation linearity over technologies

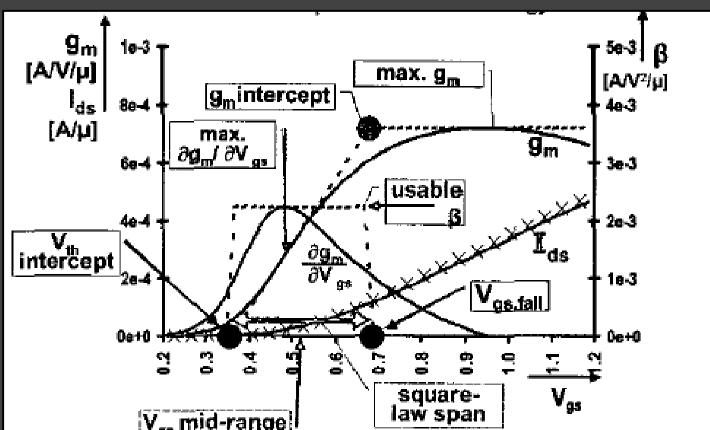
But use:

- Constant overdrive voltage, providing constant g_m/I_d and overdrive →
  - same linearity
  - same noise/unit current
  - same gain/unit current

→ Provides efficient transistor parameter extraction from design based view

Measurement theory (I)

1. Measure I_d versus V_{gs}



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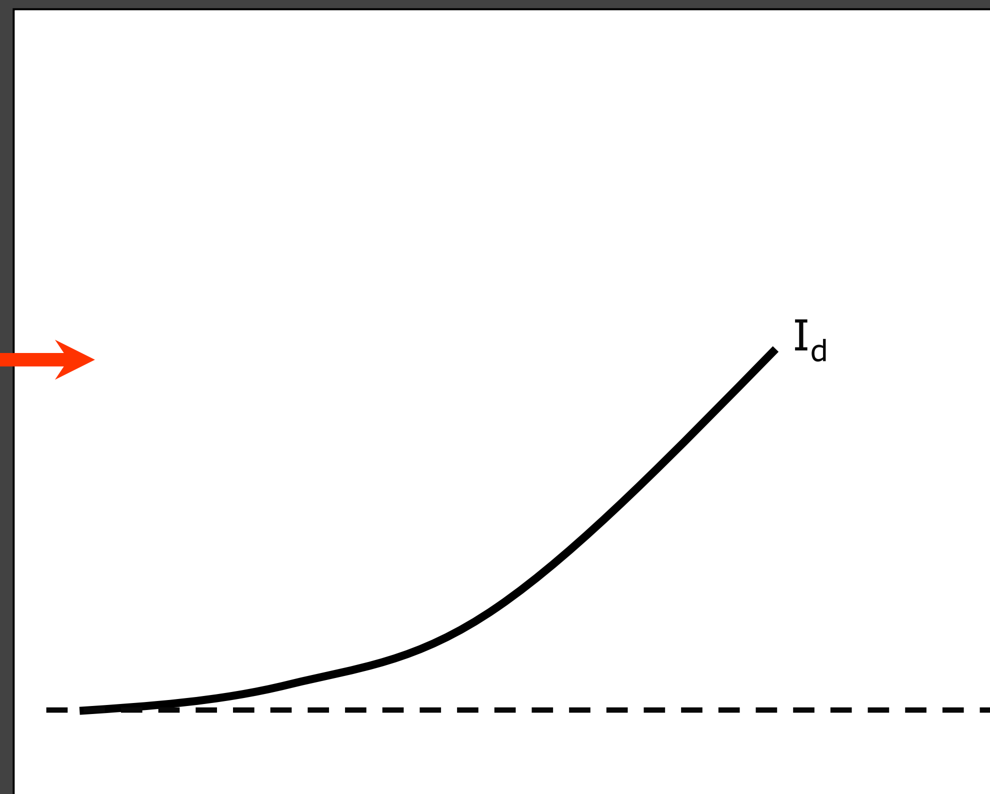
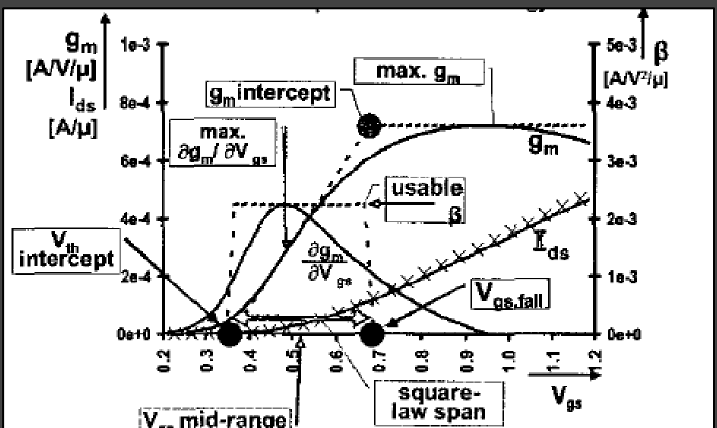


Measurement theory (I)

1. Measure I_d versus V_{gs}
2. Determine $\delta I_d / \delta V_{gs} = g_m$



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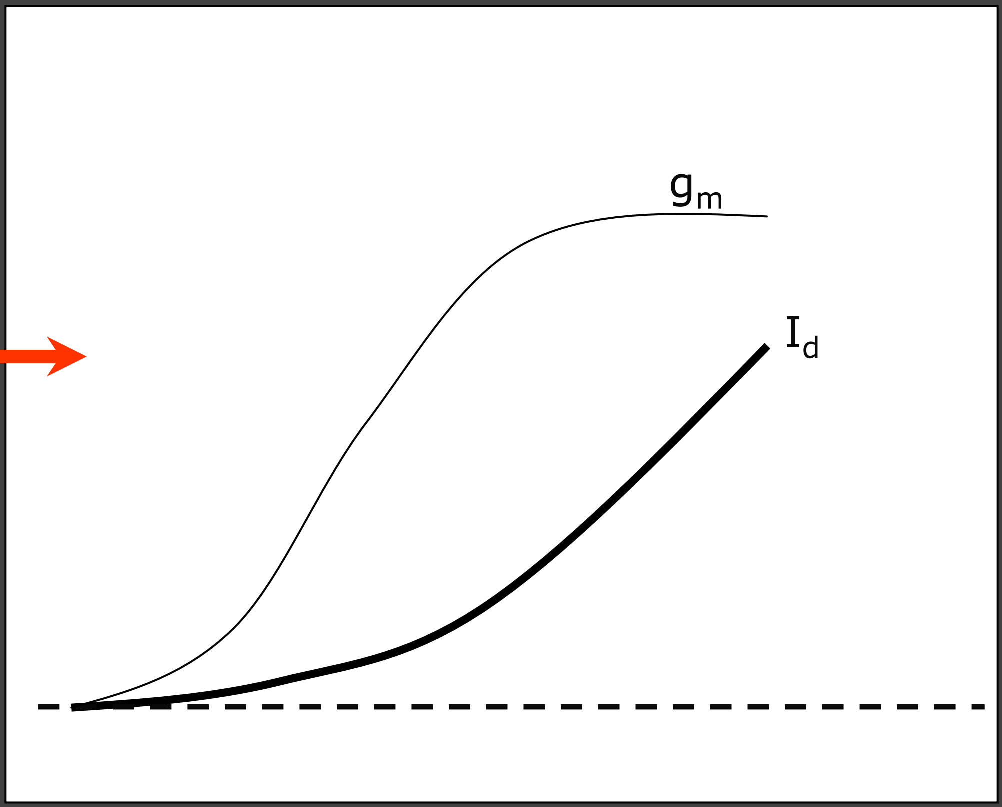

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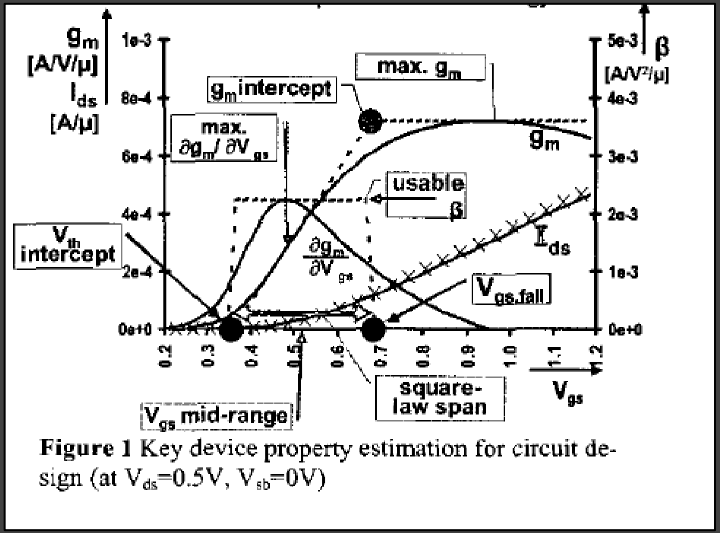
1. Measure I_d versus V_{gs}
2. Determine $\delta I_d / \delta V_{gs} = g_m$
3. Determine $\delta^2 I_d / (\delta V_{gs})^2 = \beta$ and maximum usable β



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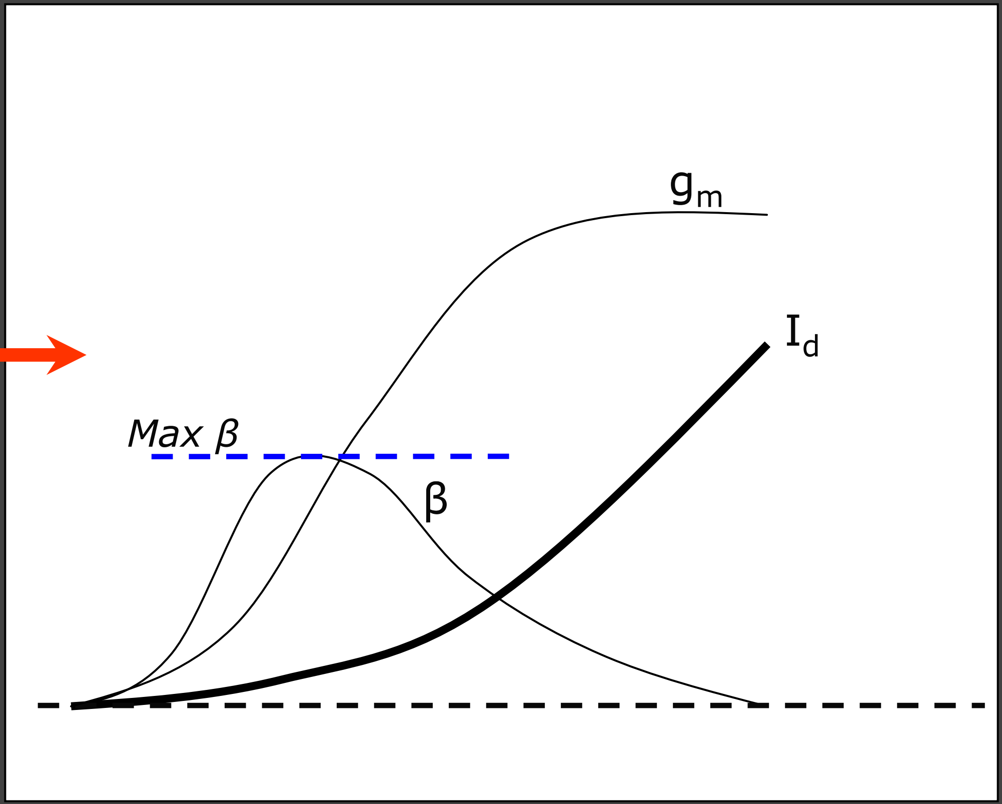

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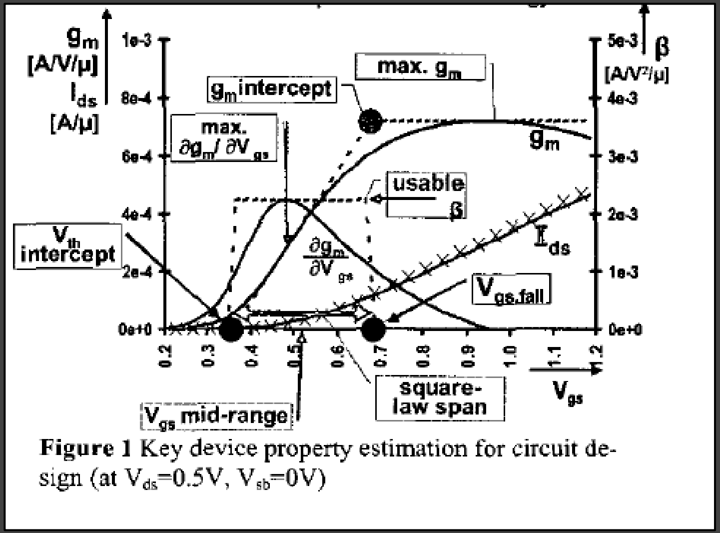
4. Estimate linear g_m at maximum usable β



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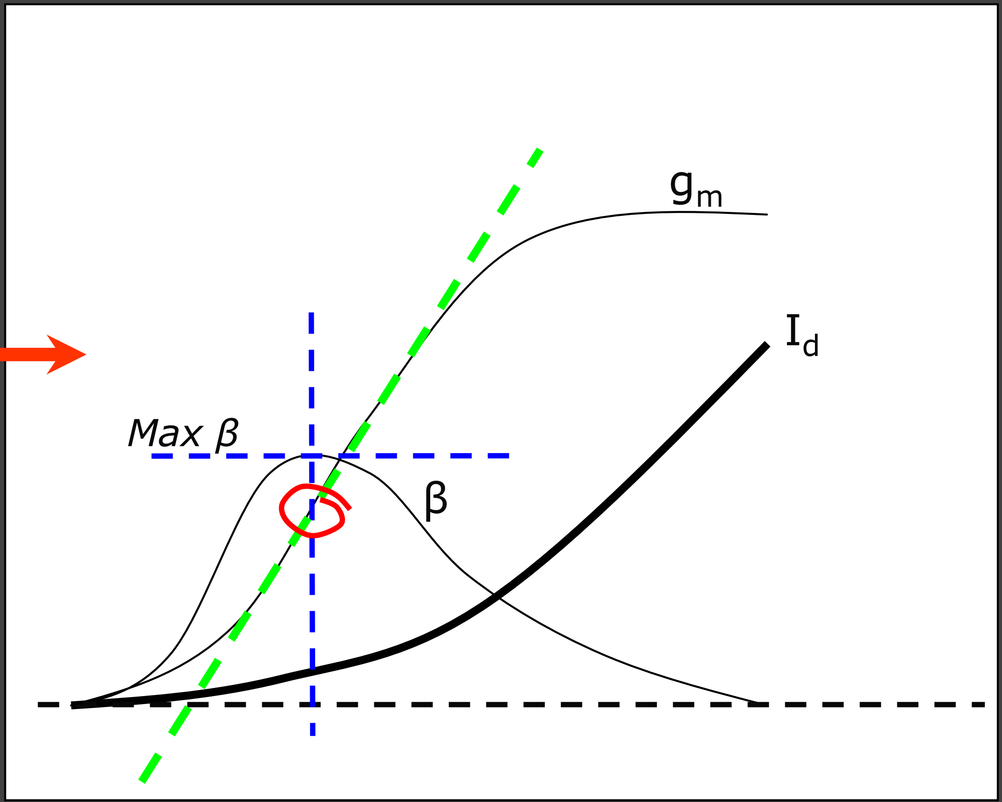

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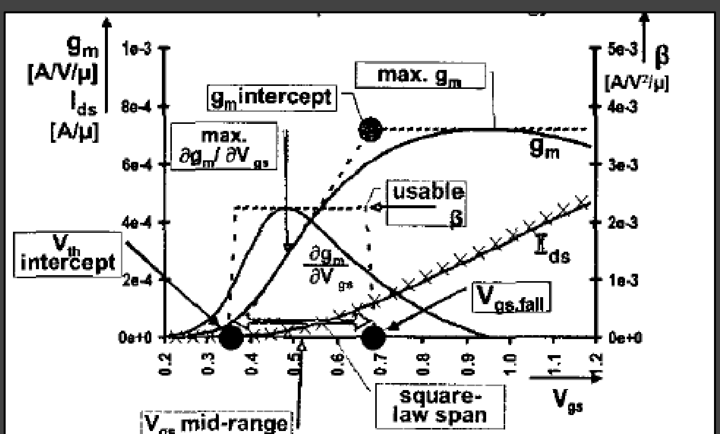
4. Estimate linear g_m at maximum usable β
5. Derive square law region from interception linear g_m with zero and max g_m



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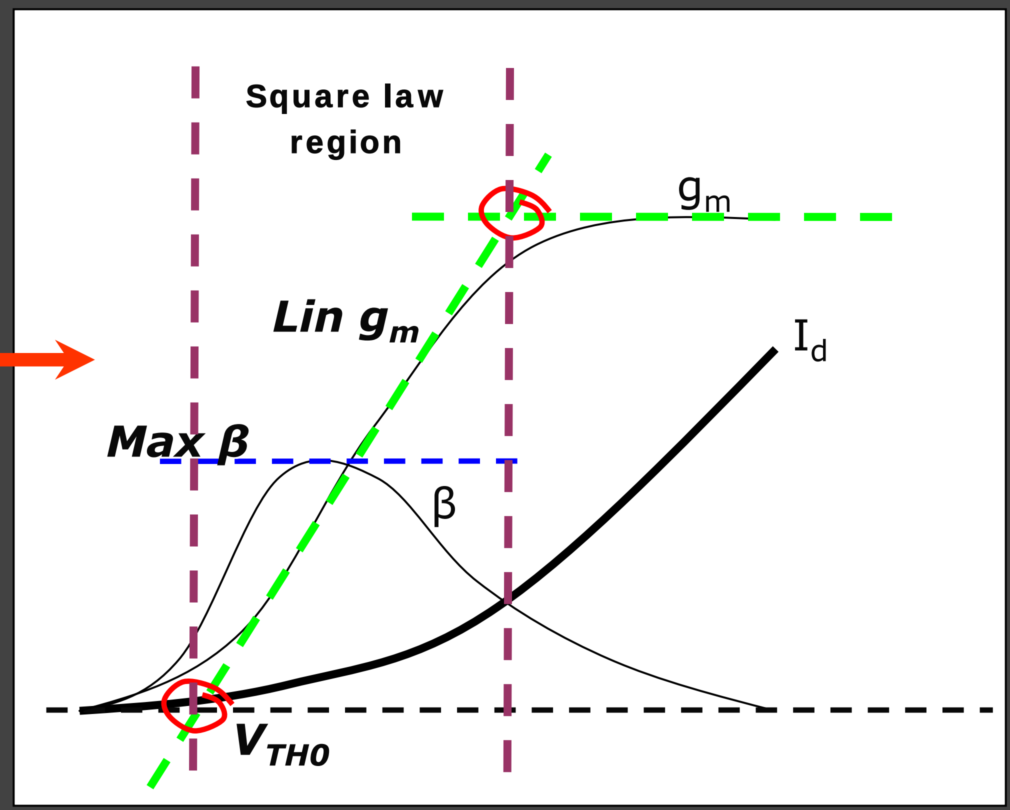

Measurement theory (II)

For the normal devices, first order effects of radiation can also be predicted by the square law model assuming a build up of charge on the side (i.e. LOCOS birds beak or STI) of the device.

Device current (saturation)

$$I_{d,SAT} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs} - V_{TH} + \frac{2Q_{rad/\mu m}}{C_{ox}}\right)^2$$

$$Q_{rad/\mu m} = Q_{rad}.L$$

Linear charge build up alongside length device

Dependencies

$$\frac{\partial V_{TH}}{\partial Q_{rad}} = \frac{\partial\left(\frac{\sqrt{I_d}}{\sqrt{\mu_n C_{ox}\frac{W}{L}}} - V_{gs} + \frac{2Q_{rad}.L}{C_{ox}}\right)}{\partial Q_{rad}} = \frac{2L}{C_{ox}}$$

$$\frac{\partial g_m}{\partial Q_{rad}} = \frac{\partial\left(\mu_n C_{ox}\frac{W}{L}\left(V_{TH} - V_{gs} + \frac{2Q_{rad}.L}{C_{ox}}\right)\right)}{\partial Q_{rad}} = \mu_n C_{ox}\frac{W}{L}.\frac{2L}{C_{ox}} = 2\mu_n W$$

$$\frac{\partial \beta}{\partial Q_{rad}} = \frac{\partial\left(\mu_n C_{ox}\frac{W}{L}\right)}{\partial Q_{rad}} = 0$$

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Intermediate summary

- Target technologies based on mixed-signal considerations → AMI Semiconductor 0.35µm and UMC 0.18µm good candidates

- Selected parameters are threshold voltage, transconductance and current factor: important analog parameters

- Parameter extraction based on design orientated extraction, requires only I_d versus V_{gs} curves (i.e. no CV measurements or interface state analysis used)

- Theory shows that if linear charge build up occurs along the length of the device the threshold shift should be worse for long devices, g_m variations are worse for wide devices and β should not be affected

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Test setup

- **Inputs:**
  Set common supply and sweep V_{gs}
- **Outputs:**
  Drain current measured over 50Ω measurement resistor
- Multiplexer switches 20 resistors to DMM to measure voltage drop over resistor
- 160 devices total, 50 sample points of $I_d(V_{gs})$, 10 samples/s

  → full measurement 15 min

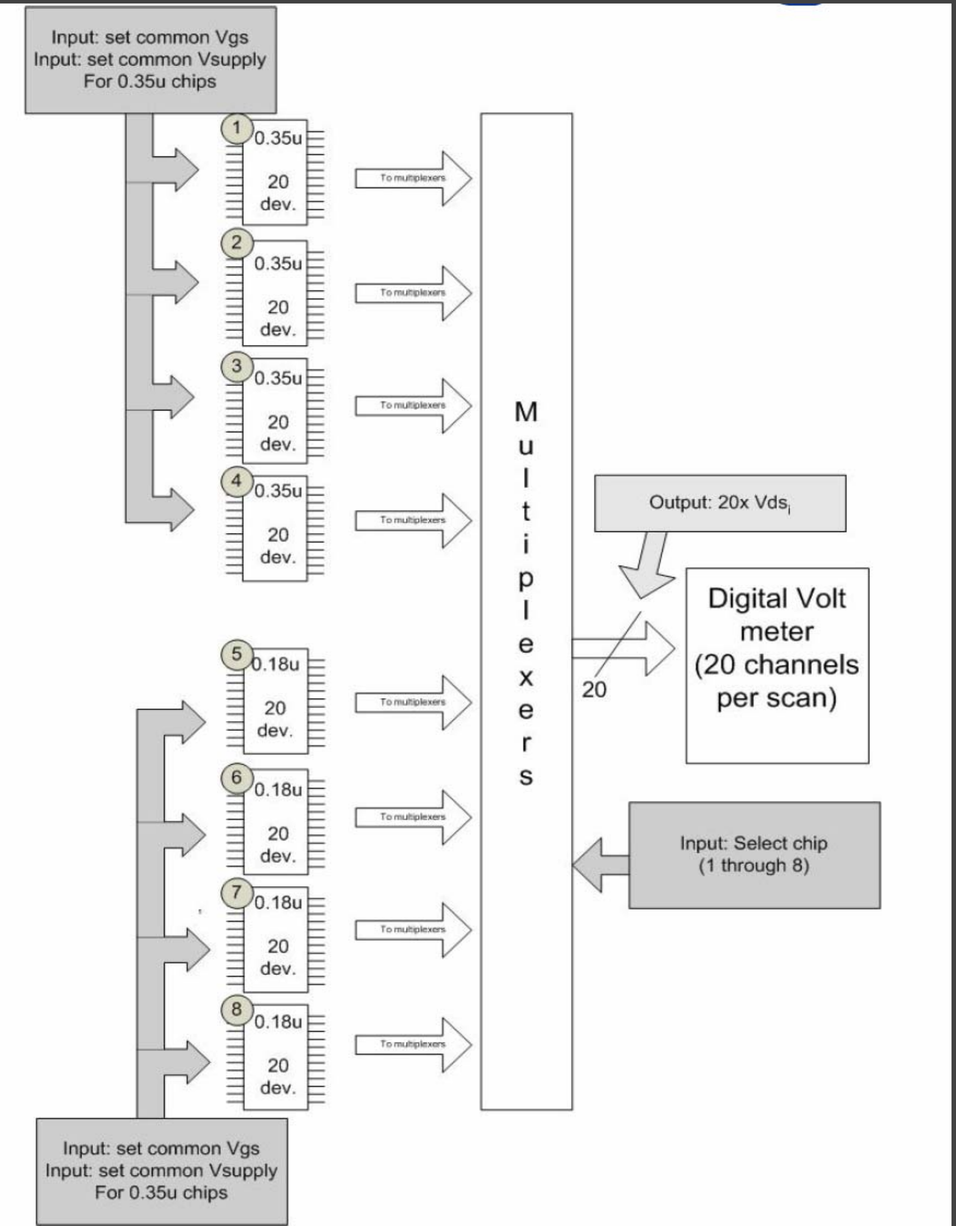
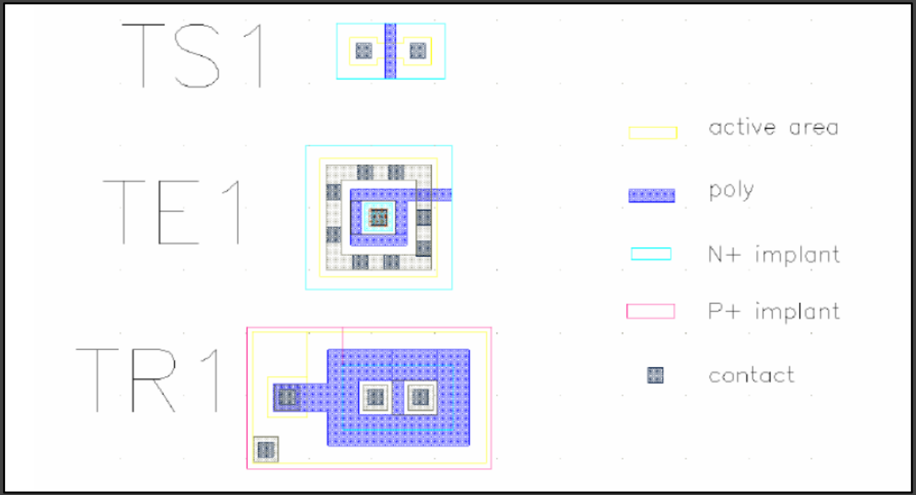


Figure 5: Global test setup

Devices under test

- 20 devices on each chip:
  - 7 normal layout (TSx)
  - 5 ELT (TEx)
  - 8 RET (TRx)



- 4 chips / technology

AMI 0.35u Semiconductor						UMC 0.18u					
Normal		ELT		RET		Normal		ELT		RET	
W [µm]	L [µm]	W [µm]	L [µm]	W [µm]	L [µm]	W [µm]	L [µm]	W [µm]	L [µm]	W [µm]	L [µm]
0.5	0.35	4.8	0.35	3.2	0.35	0.24	0.18	2.16	0.18	1.54	0.18
1	0.35	15	0.35	4.5	0.35	0.5	0.18	6	0.18	2	0.18
2	0.35	4.8	0.7	6.5	0.35	1	0.18	2.16	0.18	3	0.18
10	0.35	4.8	2	3.2	0.7	5	0.18	2.16	1	1.54	0.36
0.5	0.7	15	2	3.2	2	0.24	0.36	6	1	1.54	1
0.5	2			3.2	6	0.24	1			1.54	3
2	2			6.5	2	1	1			3	1
				13	6					6	2

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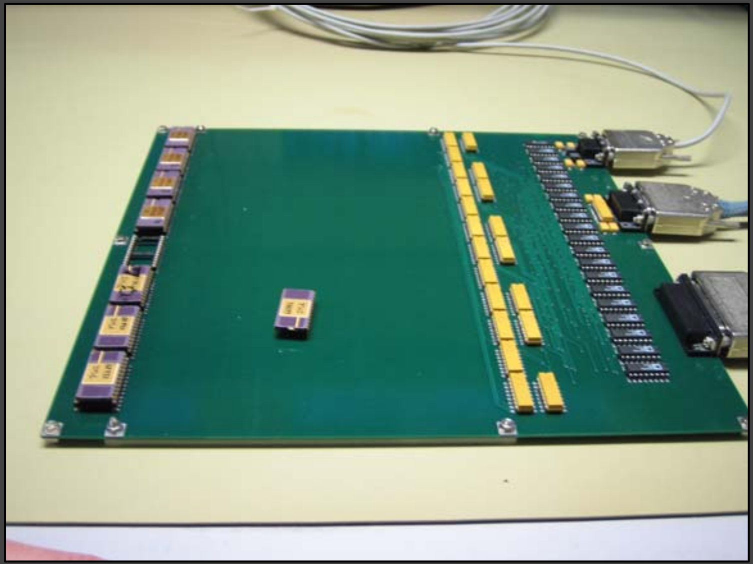
Test procedure



Testing at ESA-ESTEC Co-60 facility:

- Total dose 200kRad(Si)
- Dose rate roughly
  1.25 kRad/hr or 0.35 rad/s
- Closed lid packaging of test devices

Testprocedure:

- Online measurement of I_d versus V_{gs} curves (8m cable)
  → no annealing, fairly low dose rate
- Data analysis after 100kRad(Si) (hardly any damage found)
- Changed testboard orientation
  → incident beam from 0° angle to 90° angle
- Continued testing for next 100kRad(Si)

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Test results (I)

- Due to less effective shielding in the upright testboard position severe leakage currents appeared in the multiplexers. Since V_{dd} of the multiplexers is ±12V the IC technology is probably old and sensitive to total dose radiation. First run measurement were used (100kRad(Si)) to analyze the shifts.

- Parameters shifts for $\mathbf{V_{th}}$ and $\mathbf{g_m}$ were measured for the normal 0.35µm normal layout devices. Variations of β were within measurement resolution.

  For the RET and ELT devices and all 0.18µm devices the detected shifts were within the measurement resolution (±2% RMS)

- The parameter shift after 100kRad(Si) for the normal 0.35µm devices were at an average (over device size) of:
  - -5% for V_{th}
  - +7,5% for g_m

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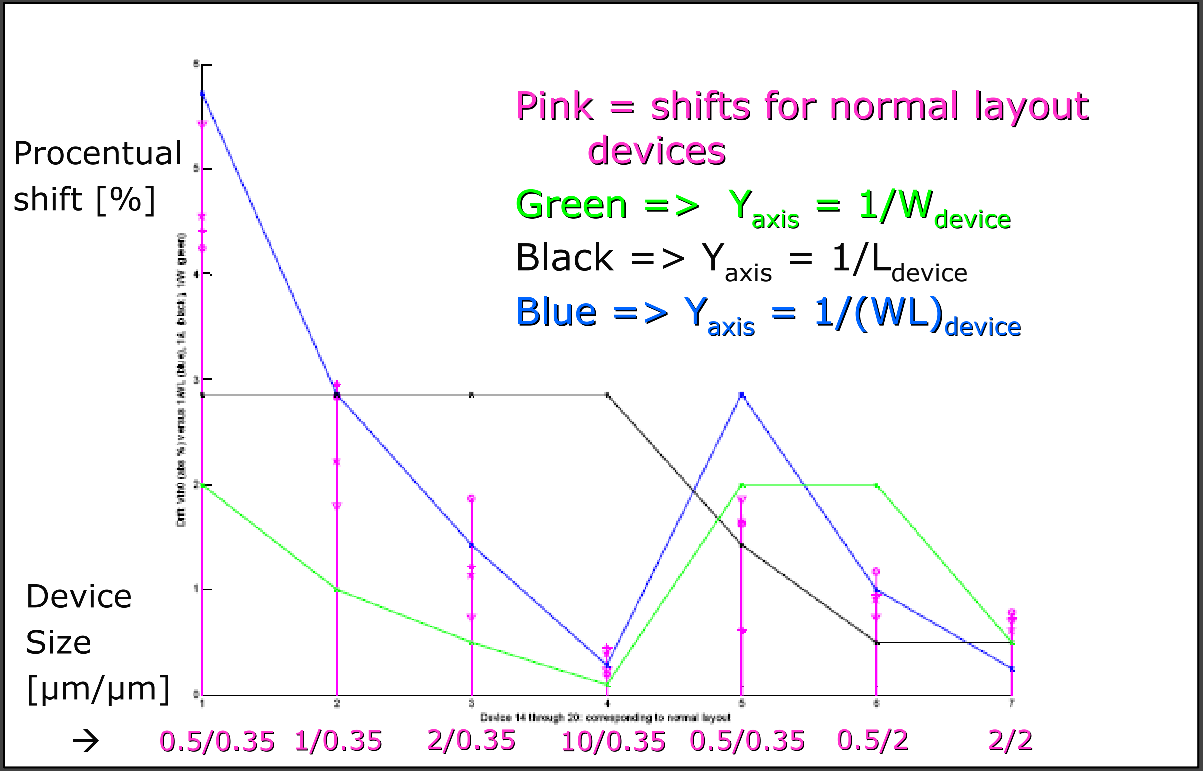
Test results (II)

- The dependency of the shifts on device size did not correspond with the linear charge build up model. An inverse dependency on device area was found for the shifts in the seven normal layout 0.35μm devices.



Y-Axis show percentual shift of V_{th}, X-Axis features different device sizes

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Test conclusions (I)

- Although the measurement resolution was fairly low, the expected parameter deviations due to mismatch/processing for the respective device sizes is in the same order of magnitude of measurement error.

  → This means that a simple, design orientated measurement procedure can be used to determine if either the radiation shift or (standard) mismatch and process error considerations dominate design trade offs.

- For standard layout 0.35μm devices radiation shifts should be taken into account for space application design.

Test conclusions (II)

- The 0.18μm devices and all RET and ELT devices did not suffer large deviations up to a dose rate of 200kRad.
- Online measurement did not provide any insight on the build up of charge during radiation and had a negative impact on measurement resolution (multiplexing, long cables, …).
- Since the parameter shifts are correlated with the inverse of the device area, data suggests that the charge build up is not solely alongside the device, but also in the thin oxide.

Future research

- **Maintain a design orientated point of view.**
  Radiation research on devices and materials is wide spread, utilizing these results in mixed-signal IC design for space applications should not be limited to the proposed guidelines.

  Also, from a design point of view, focus should be on analog parameters such as matching, noise, parameter shift, leakage, speed and so on.

- **Research RET transistor.**
  ELT transistors suffer from non-symmetry, modeling problems and arbitrarily small W/L ratios can not be achieved. These effects should not be as dominant for RET transistors, although RET transistors might suffer other drawbacks.

- **Practical changes in measurement setup**
  If online measurement is a must, rely on radiation tolerant readout components. Otherwise, focus on correct biasing and develop accurate offline dedicated readout equipment.