Radiation Testing of Innovative GPS-Receiver
Two ASICs designed in AMS 0.35 µm Technology

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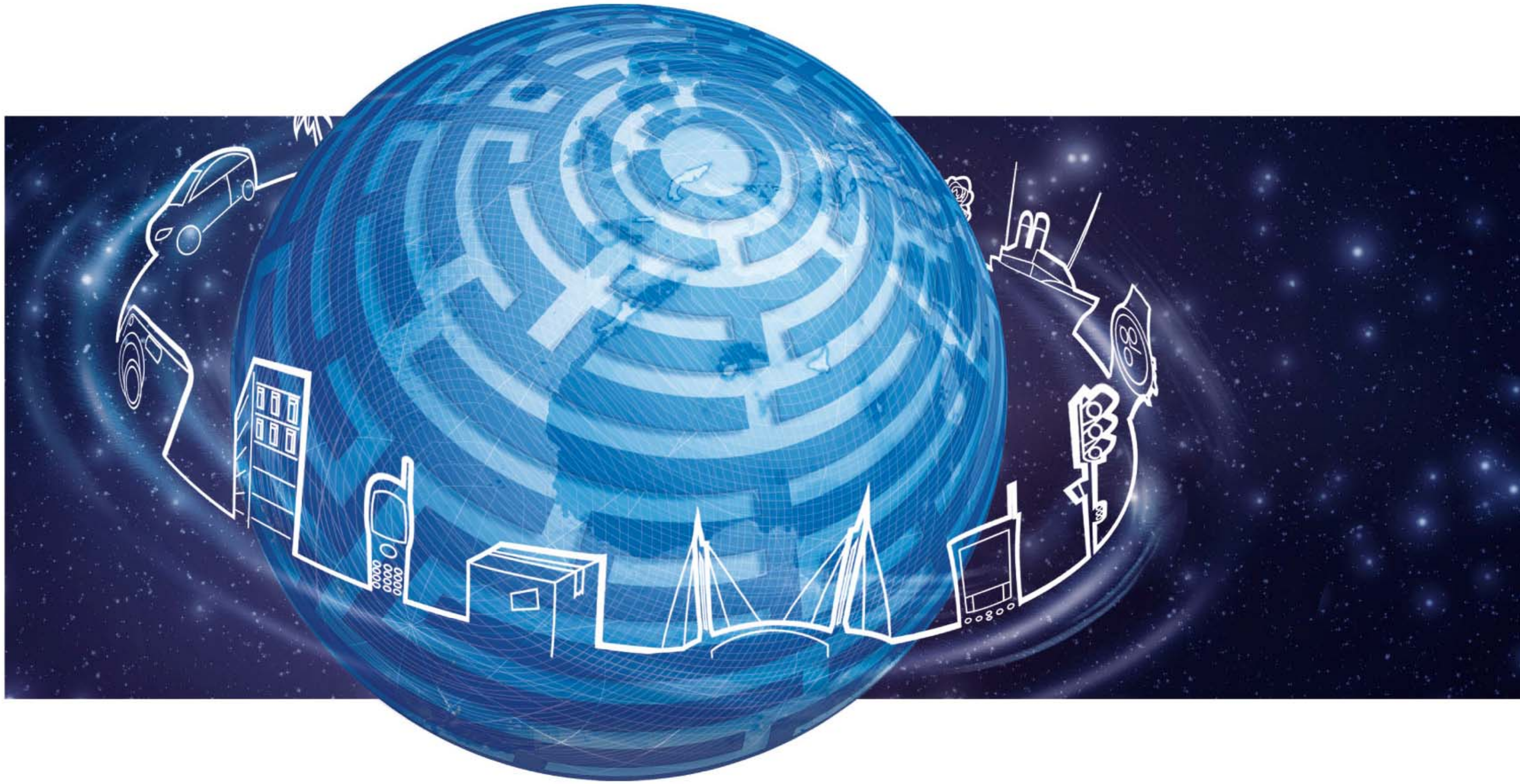


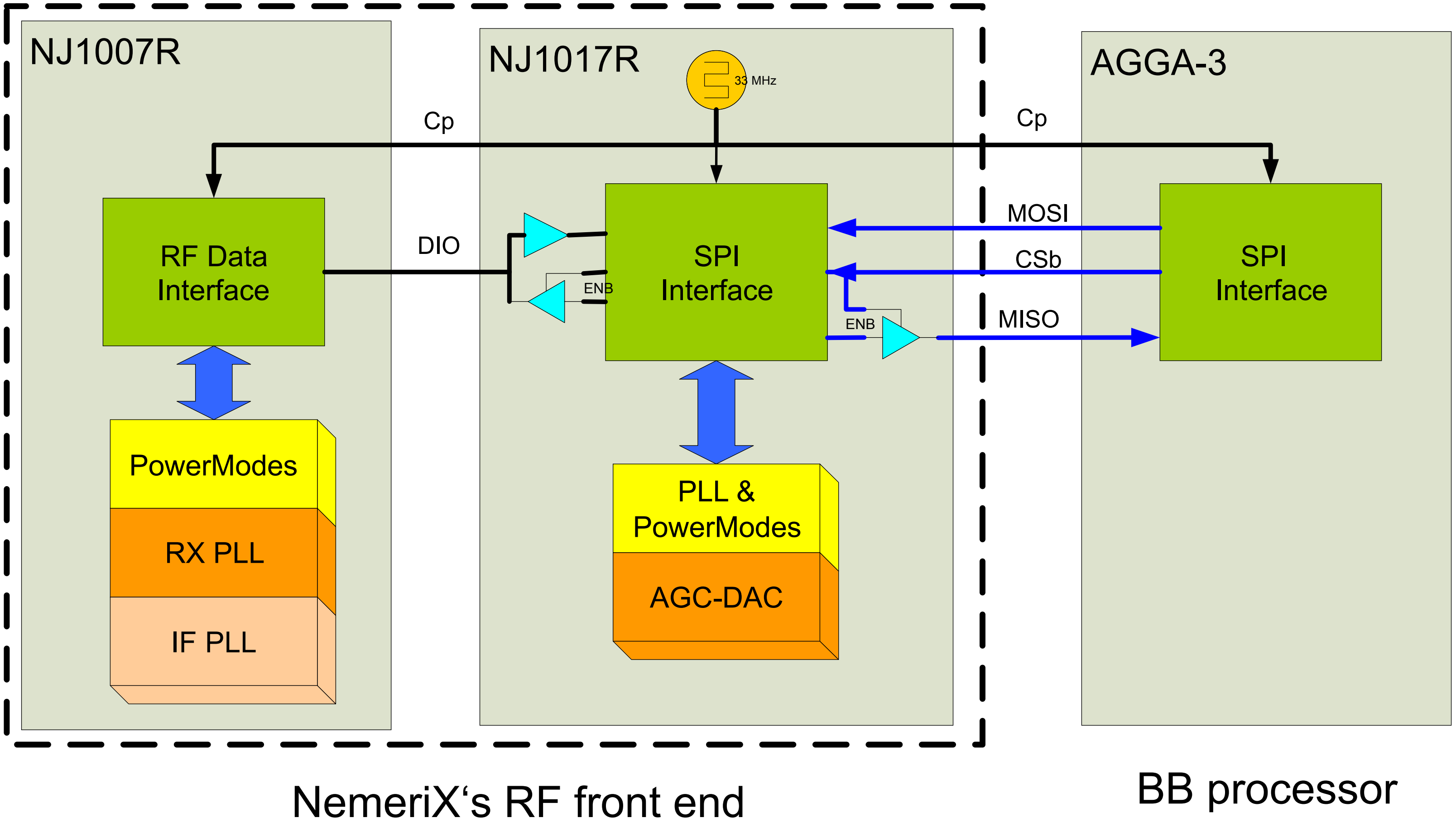
Angelo Consoli & Francesco Piazza
RADECS 2007

NEMERIX
WORLD'S LOWEST POWER GPS CHIPSETS

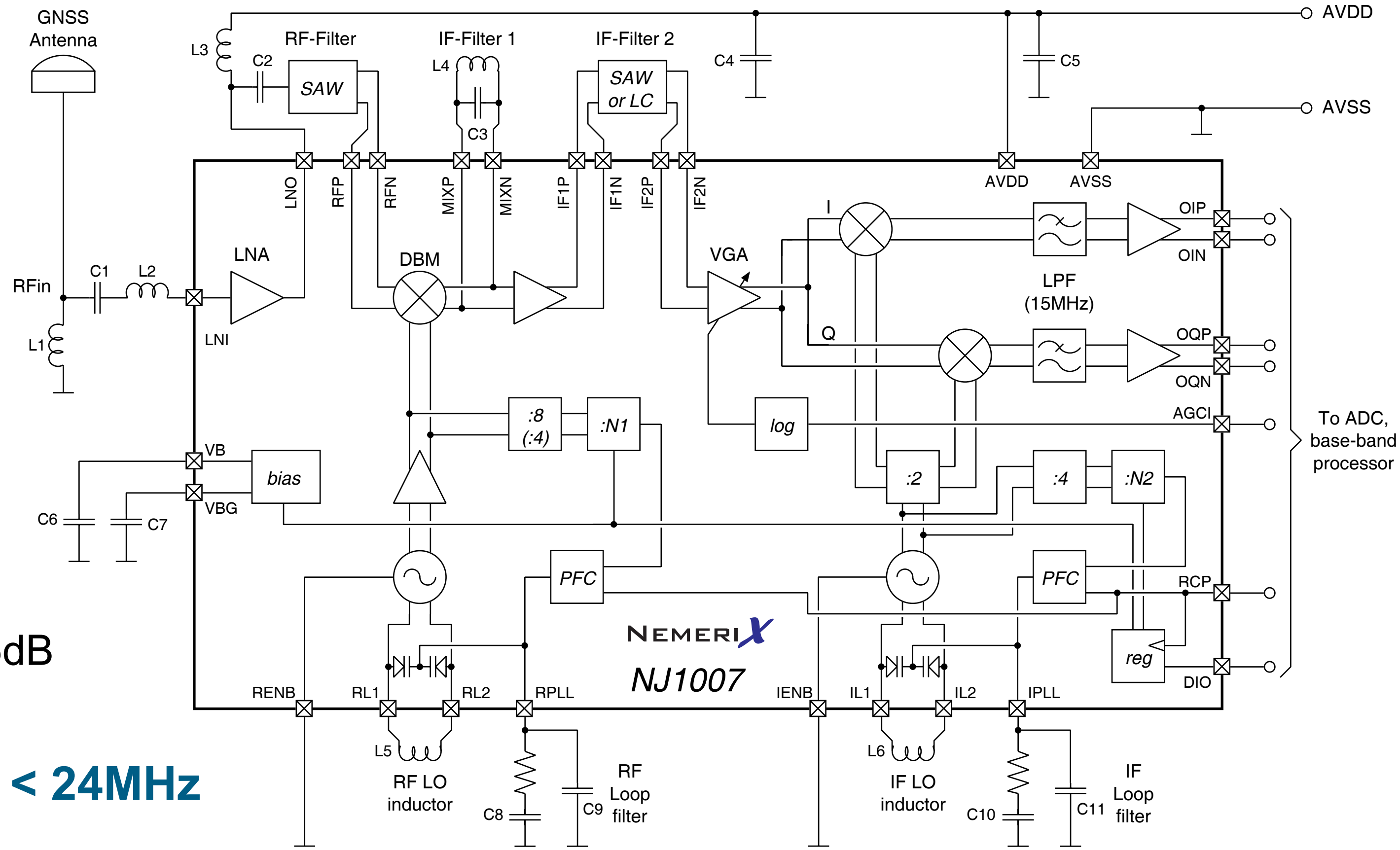
NemeriX's IGPS chipset

- **The chipset consists of 2 ASICs:**
  - NJ1007R: RF receiver front end.
  - NJ1017R: AD DA interface.
- **Requirements**
  - Multifrequency receiver GPS/Galileo/GLONASS.
  - High RF performances more important than integration level or cost effectiveness.
  - Radiation tolerant design for space borne applications.
- **Technology selection criteria:**
  - Shall have good RF performance.
  - Shall be available also in small quantities.
  - Shall be either radiation tolerant or allow radiation tolerant circuits to be designed.

System configuration



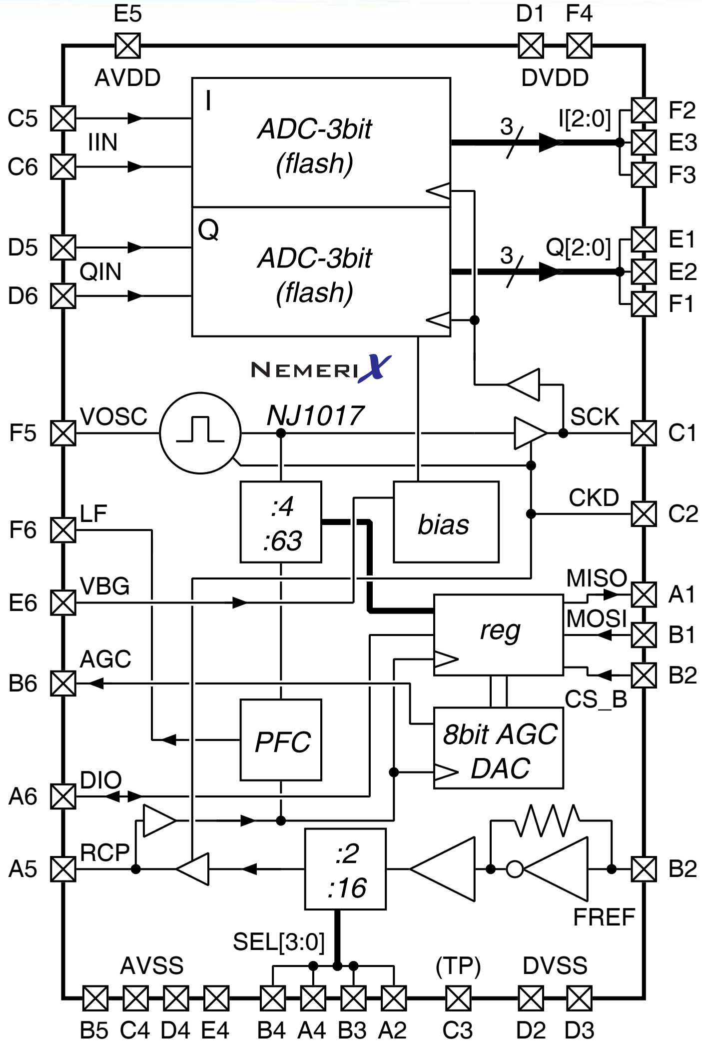
NJ1007R – RF receiver front end



- **LNA**
  - Gain: 19dB
  - Noise Figure: 1.6dB
- **External filters**
- **Signal Bandwidth < 24MHz**
- **I/Q outputs**
- **Die dimensions: 1.2x1.2mm**

NJ1017R – AD DA Interface ASIC

- **2 ADCs (for GNSS signal)**
  - 3-bit
  - Sampling frequency < 50MHz
- **8-bit DAC (for AGC)**
- **Other support functions for NJ1007R**
- **SPI-like interface to the base band processor**
- **Die dimensions: 1.2x1.2mm**



Process selection

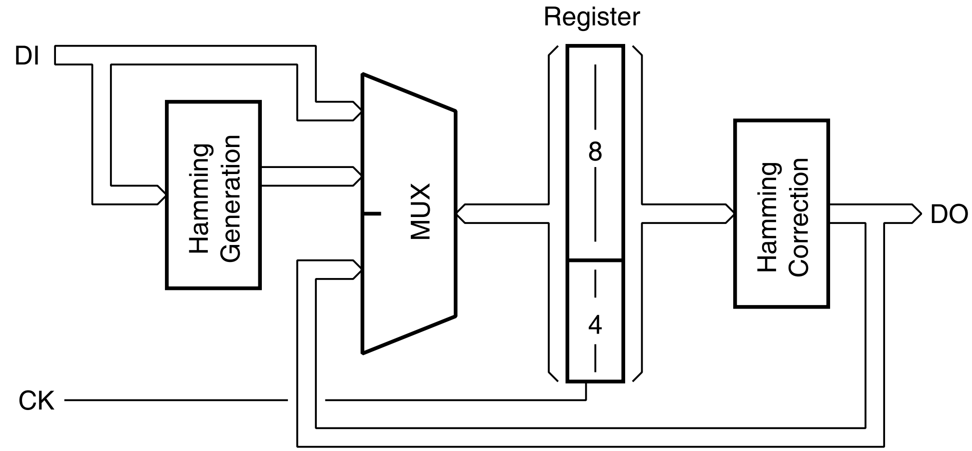
- **General:**
  - Thin layers (wells, diffusions, oxides). Thick N-well may improve latch-up.
  - Retrograded well or buried layer and epi improve latch-up resistance.
  - SOI has no mechanism to generate a latch-up.
  - Deep trenches improve latch-up somewhat.
- **BJT:**
  - Thin base and emitter more robust than thick base (less β degradation).
  - Poly emitter (thinner) more robust than a diffused one.
- **MOS:**
  - Thin gate oxide better than thick oxide (less charge trapping, less device degradation).
  - Shorter channel transistors (stronger) give improved SEE resistance.

Process: AMS S35, 0.35µm SiGe HBT

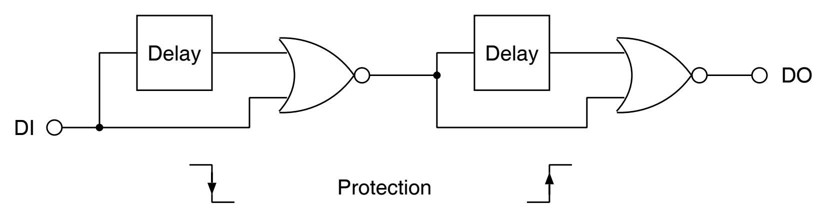
Circuit techniques for rad. tolerance

Analog circuits (e.g. enable lines) are sensitive to transients: need protection against SEU and SET

- **SEU : error correction**
  - **Hamming code**
  - **Output after error correction matrix**



- **SET : transient suppression logic**
  - **Combinational delays**
  - **Removes positive and negative glitches**



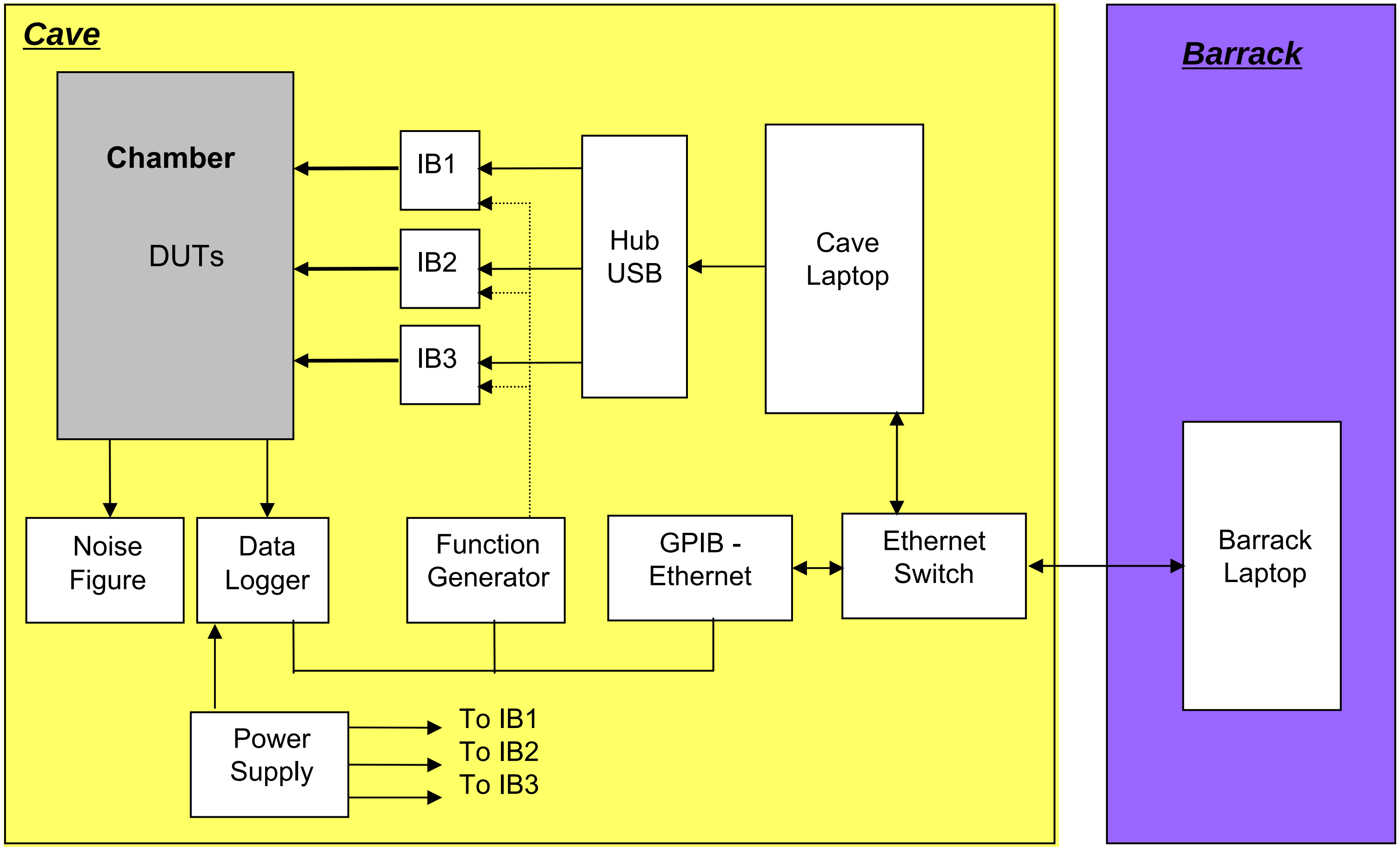
Layout techniques for rad. tolerance

- **Minimization of the length of N-well edges facing N diffusions.**
- **Increase of distances between N and P diffusions; N diffusion and N-well, P diffusion and P substrate (decreases β of lateral parasitic NPN BJT).**
- **Increase of overlap of N-well contact and N-well.**
- **Use of continuous guard-rings around both P and N sections of the circuit.**
- **Use of N pick-ups (collector of parasitic NPN BJT) to protect P-channel transistors that may be subject to reverse bias (mainly pad drivers and ESD protection).**

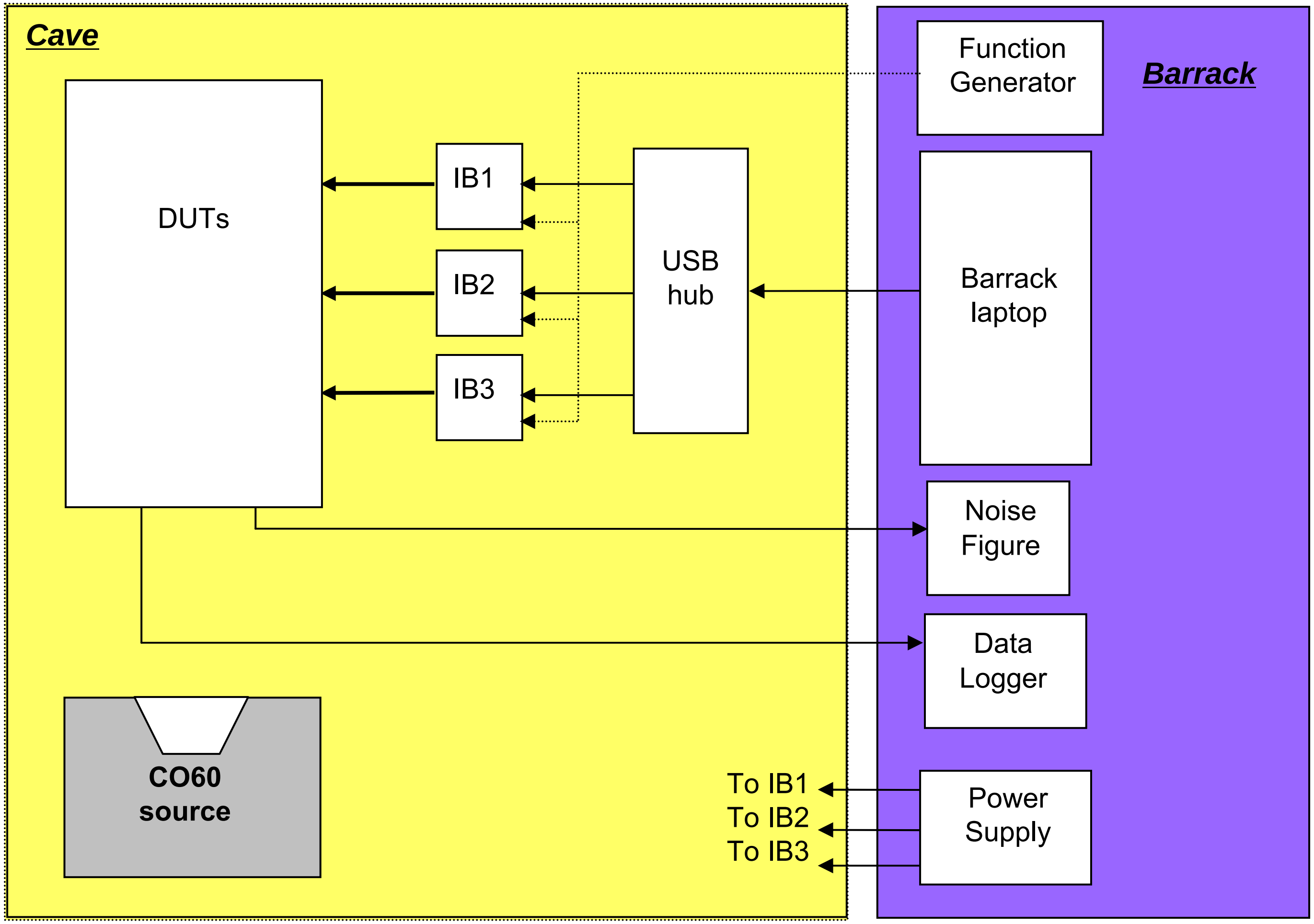
The irradiation test sessions

May 2004	First total dose test with Co-60 on G3RF ASIC at the ESTEC facility in Noordwjik.
February 2005	Cf-252 heavy ions test on G3RF ASIC at the ESTEC facility in Noordwjik.
December 2006	Final total dose test with Co-60 on both ASICs, G3RF and G3AD, performed at the ESTEC facility in Noordwjik.
December 2006	Final heavy ions test session on both ASICs, G3RF and G3AD, at the particle accelerator of the University of the Department of Physics, Jyväskylä, Finland.

Heavy ions system connection



Total dose system connection



Tests performed

Heavy ions tests

DUTs biased

Ions used:

- Argon (40Ar12+)
- Krypton (82Kr22+)
- Xenon (131Xe35+)

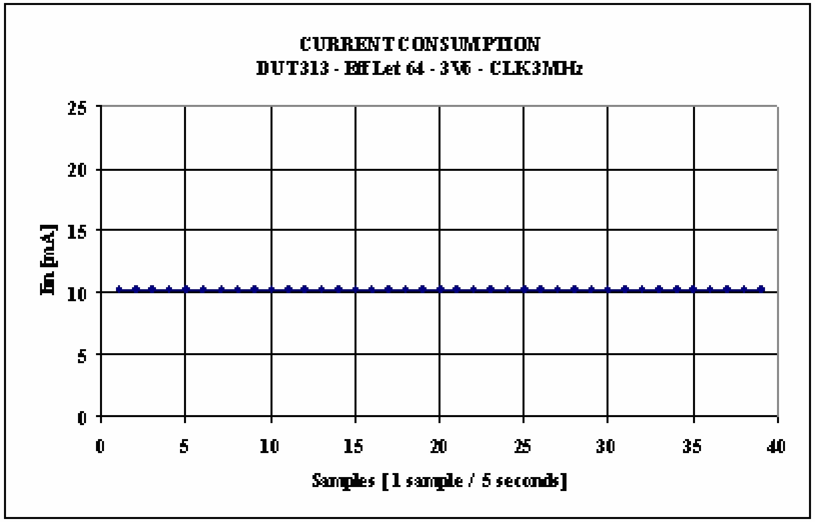
Total dose tests

4 DUTs biased, 4 DUTs notbiased

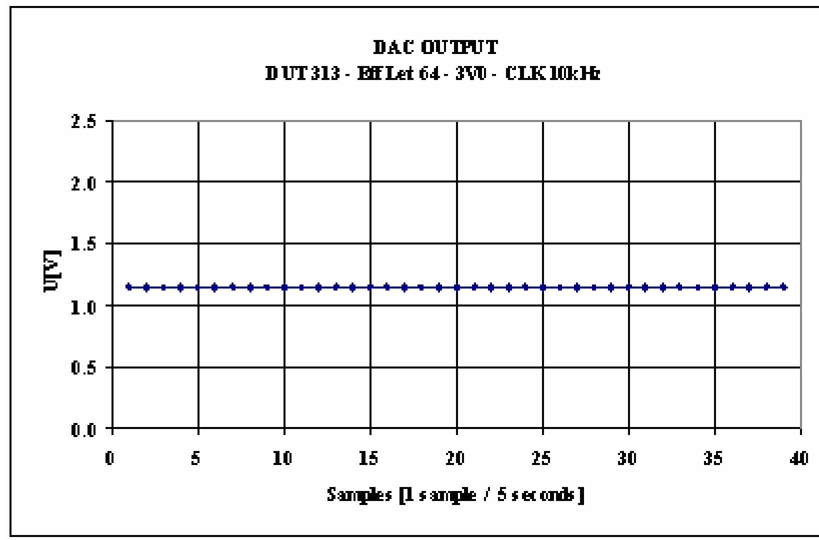
Co-60 source:

- Dose rate: 11,500-11,840 rad/min
- Exposure time: 143.5 hours
- Total dose: ca. 100 krad (Si)

Heavy Ions (Kr) test results

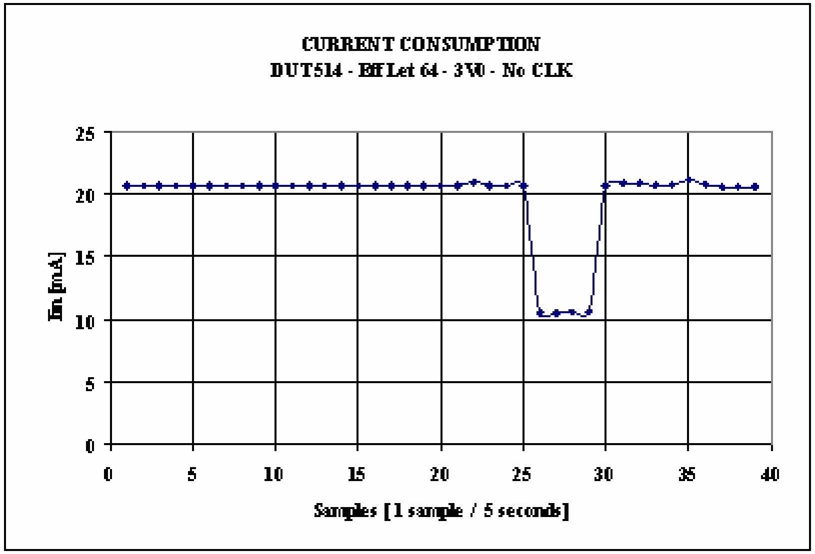


Current consumption measurement of a DUT, with error correction

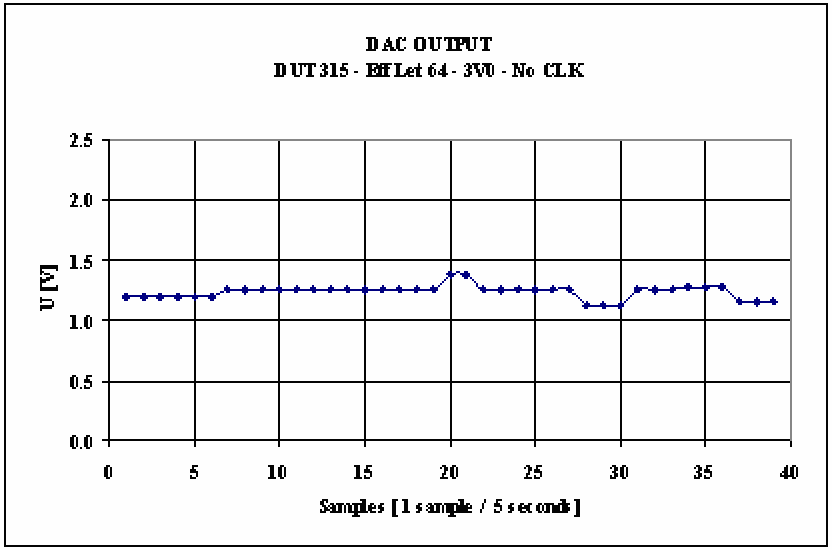


DAC output of G3AD

Heavy Ions (Kr) test results

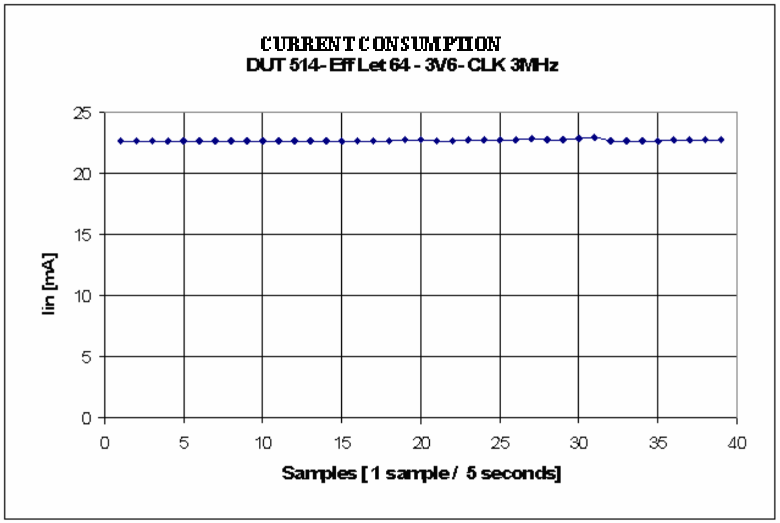


Register changes in the ASIC, error correction disabled

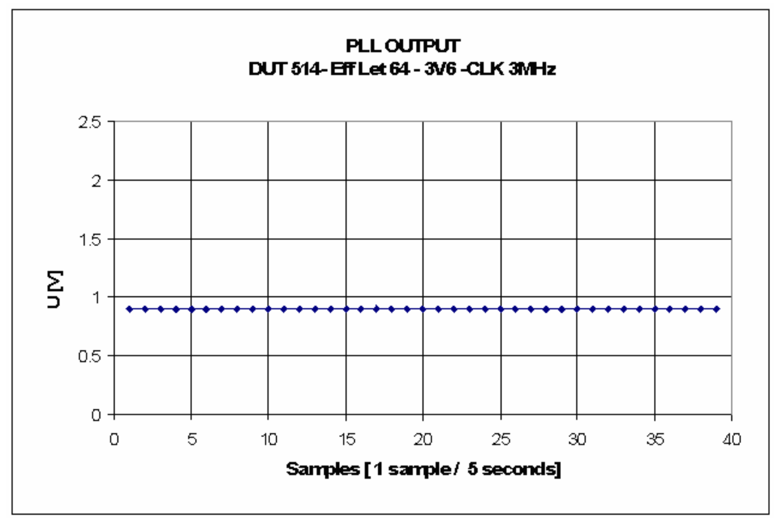


DAC output changes in the G3AD ASIC, error correction disabled

Heavy Ions (Xe) test results

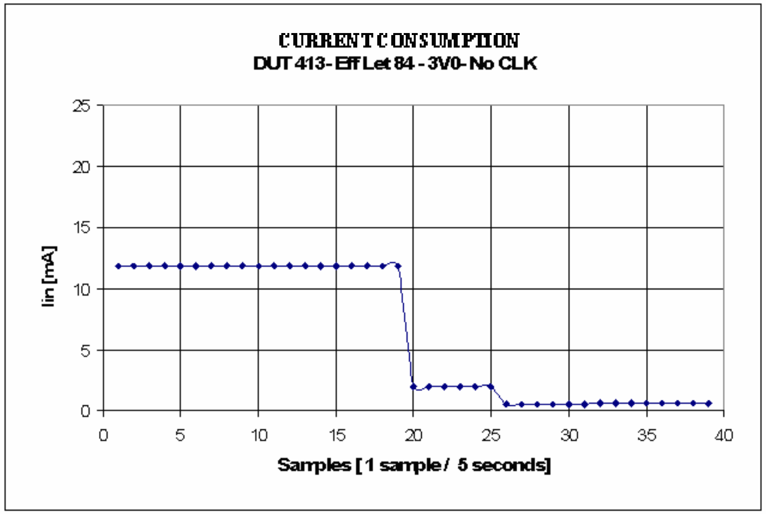


Current consumption at Let84, 3V6, clock=3MHz

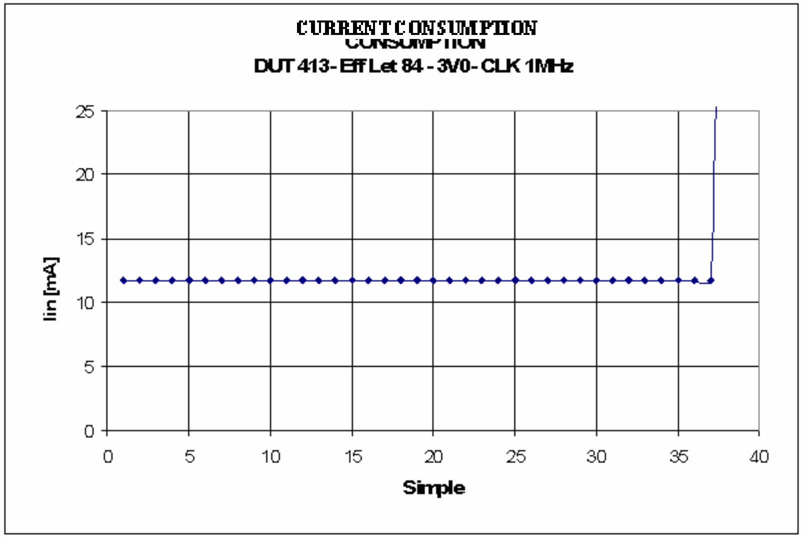


PLL output; Let84, 3V6, clock=3MHz

Heavy Ions (Xe) test results

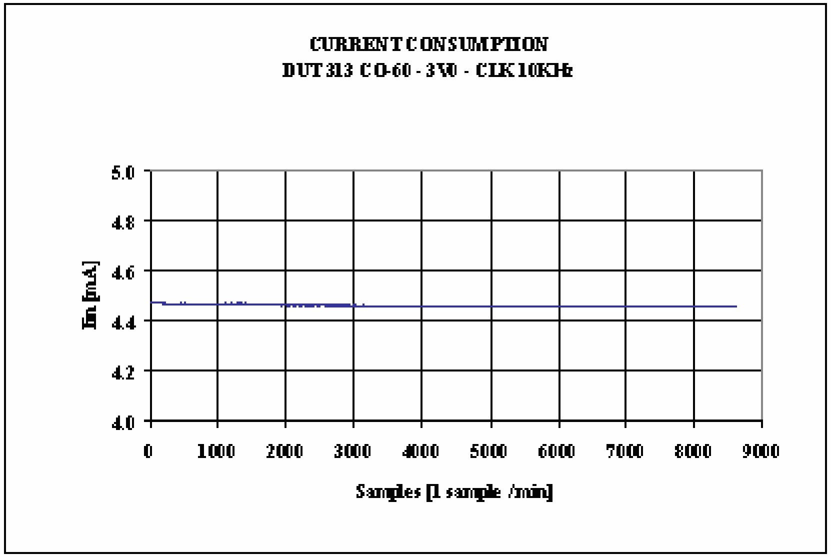


SEU in power register at Let84, 3V6, clock=0Hz (no error correction)

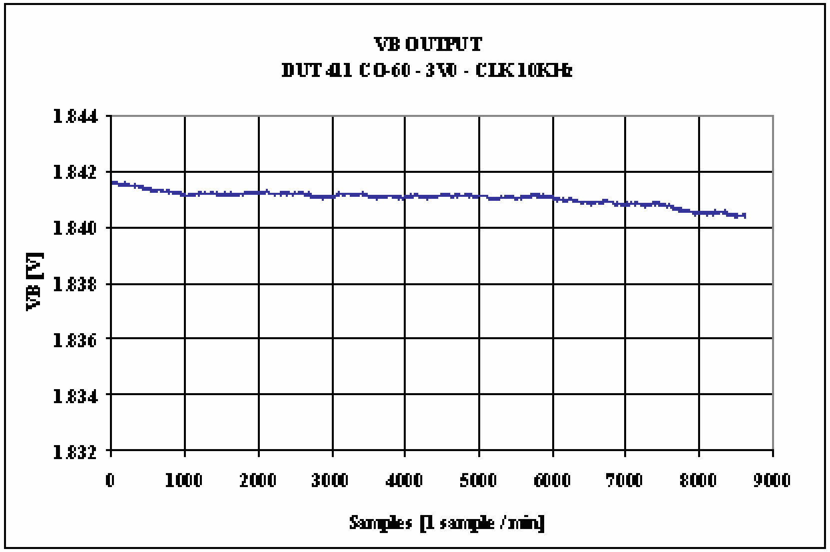


Latch-up at Let84, 3V0, clock=1MHz

Total dose test results



Current consumption at 3V0, clock=10kHz



Bandgap reference output voltage at 3V0, clock=10kHz
Variation: 1.8mV over 1 week !

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Conclusion

- The NemeriX's design rules for radiation hardening were successfully
- ASICs passed both total dose and heavy ions tests with no damageand noparametric shift.

Radiation Tolerance	Total Dose	100	krad(Si)
	Heavy Ions	84	MeV/mg/cm^2

Acknowlegments

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- **And all the staff at both irradiation facilities ESTEC and RADEF for the highly appreciated support**