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New insights into SEE ground testing on power Mosfets.

EADS ASTRIUM - CNES

D. Peyre, Ch. Binois, R. Mangeret : Astrium
F. Bezerra, E. Lorfèvre, R. Ecoffet : CNES
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1. Aim of the study

Raise potential issues related to space conditions representativity of SEE power MOSFETs ground-level testing, according to MIL STD-750 spec, or other related (ESA SCC25100, ASTM F-1192..).

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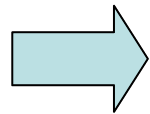
2. Test definitions & procedure (MILSTD-750) (1)

SEGR definition

§1.1.i Single-event gate rupture (SEGR): A single-ion-induced condition that causes a localized defect in the gate dielectric resulting in a catastrophic device failure, characterized by an increase in gate current that exceeds the manufacturer's rated leakage current at the gate electrode.



Comment: typically, Igss max rated = 100 nA. Designs withstand such "degradation".

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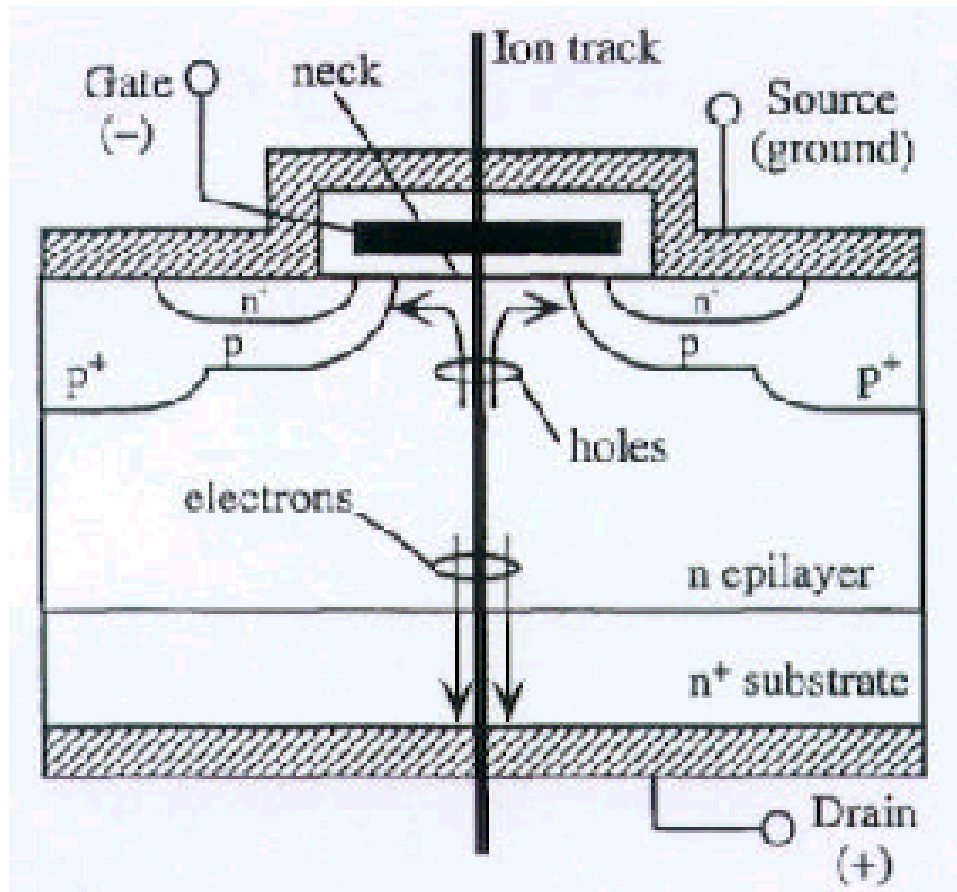
2. Test definitions & procedure (MILSTD-750) (2)

- Reminder: SEGR (Single Event Gate Rupture : N & P channels)



- **SEGR is caused by an ion strike in the neck region of the power MOSFET.**
- **The most complete study so far has shown that SEGR should not become a significant concern if the gate oxide electric field is limited below 5 MV/cm.**
- **Today, this phenomena is assumed as being probabilistic.**

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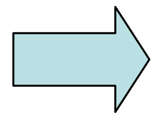
2. Test definitions & procedure (MILSTD-750) (3)

SEGR post gate stress test definition

1.1.m. SEGR post gate-stress test: After the heavy ion irradiation, a test is conducted to verify the gate integrity by applying the maximum specified VGS.



Comment: absolute max rating on Vgsoff is mostly +/- 20V, with almost no margin.

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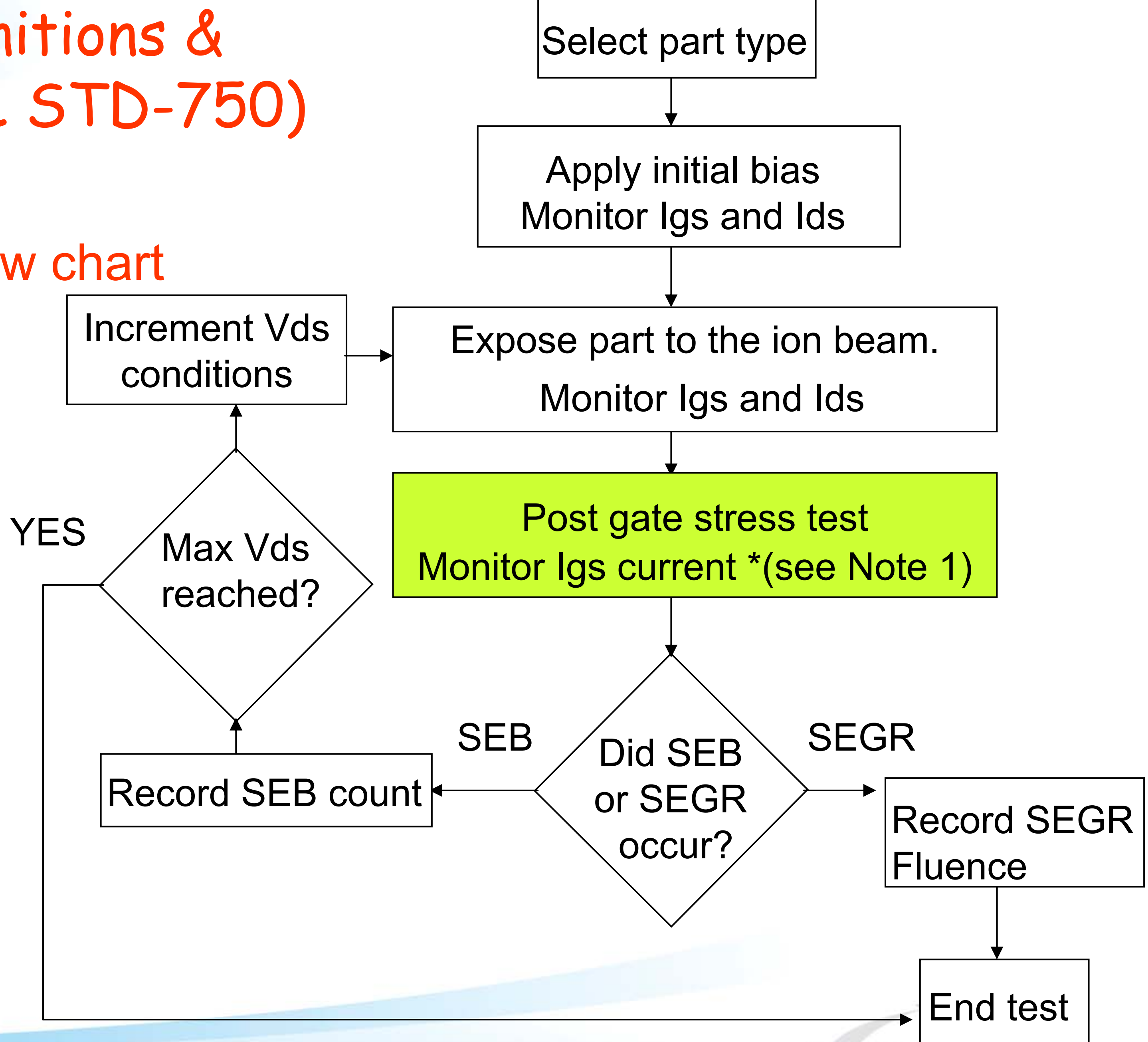
2. Test definitions & procedure (MIL STD-750) (4)

Characterisation Flow chart



*Note:
Measurement conditions
Igss : Vgs=20V
Vds=0V

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3. Status

Most of the designs use MOSFETs with |Vgsoff| ~ 0 V, in compliance with RHA golden rules.

Wealth SEE data on power MOSFETs exist in the literature, websites,…:

- NSREC 1998 Data Workshop, …
- Manufacturer data…
- …

These data are obtained according to MIL-STD-750 from experiments performed in static mode.

At Vgs=0V (No over-blocking conditions), the conclusion is SEGR occurrence:

Fluence ~ > 10^5 p/cm²

Flux ~ > 3.10^4 p/cm²/s

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4. Experimental results analysis (1)

Experiments are performed on N & P channels with varying parameters :

- Vgs (static or switched)
- Flux

Recorded parameter : Igs, Vds (burnout checked).

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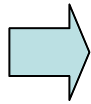
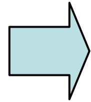
4 Experimental procedure (2)

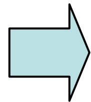
- **PROBLEM ? Continuous drift ?** Or **?sharp increase?** of gate current



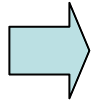
- To be able to measure continuously the Gate leakage current while the Ion beam is focused on the component die.



- Characterize the current drift versus the ion fluence



- Measurement has to be done in static and switching modes (DC-DC applications)



- The fluence shall be available at monitoring system level

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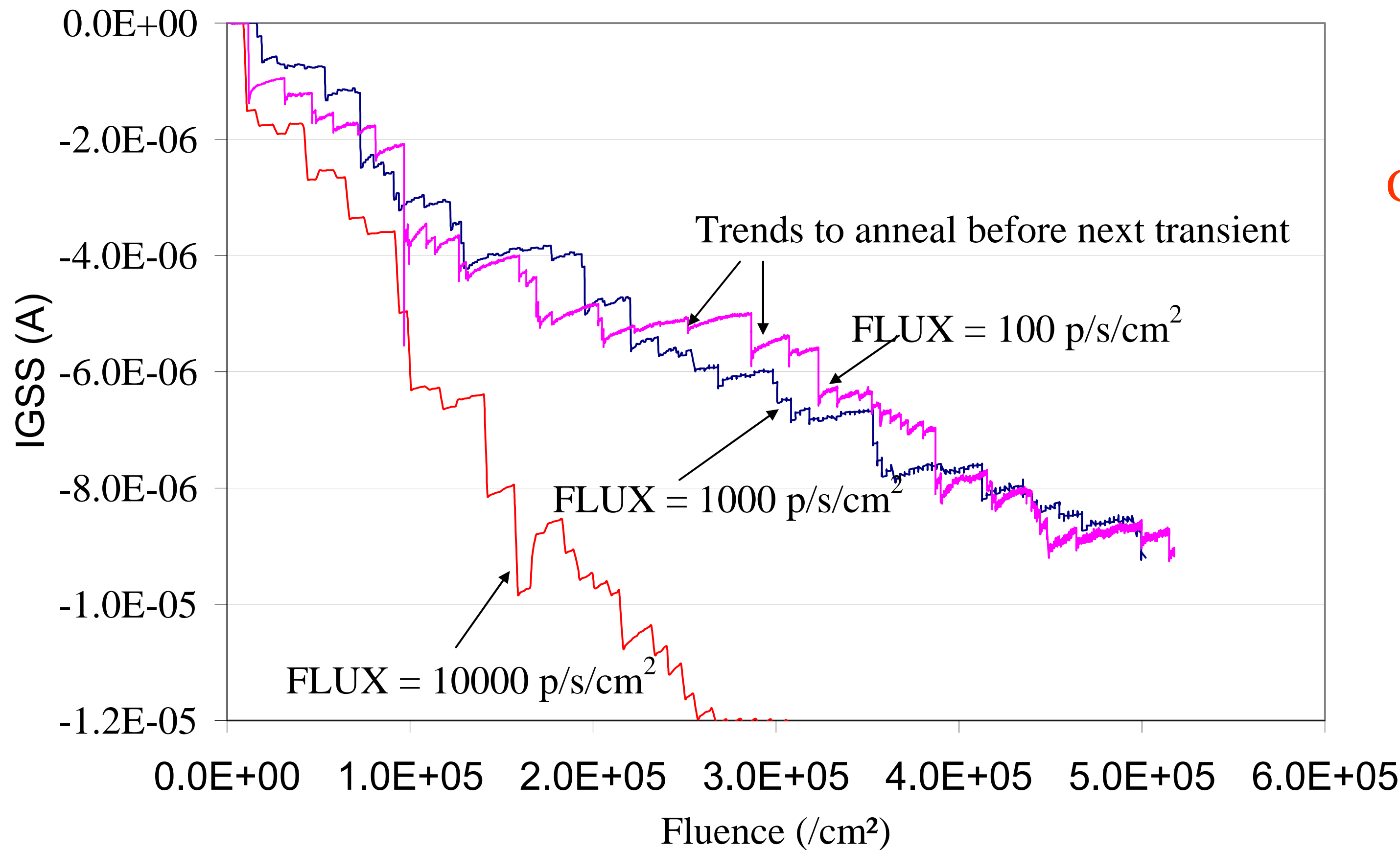
4. Experimental results : Flux effect in switched mode (N channel) (3)

IRFF110 (N channel) LET = 55.9 MeV.cm2/mg (Xe), Range = 43 µm,
Vds = 80 V, Vgs switched= [-5 V; 10V] , Igss current measured with Vgs = -5 V..



Competition between anneal and flux ?

The highest the flux, the highest degradation rate.

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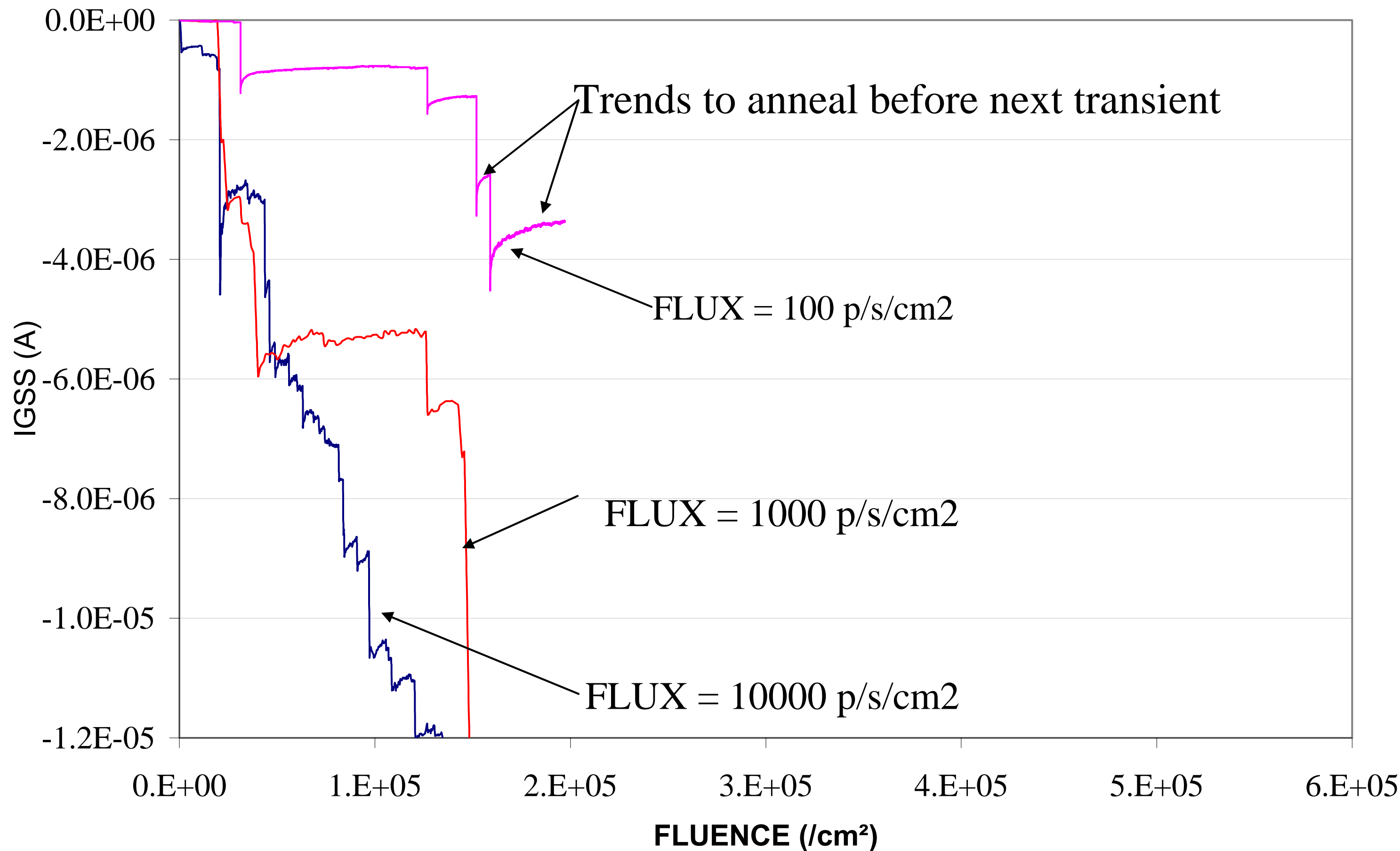
4. Experimental results : Flux effect in static mode (N channel) (4)

IRFF110 (N channel) LET = 55.9 MeV.cm²/mg (Xe), Range = 43 µm, Vds = 80 V, Vgs = -5 V, Igss current measured with Vgs = - 5 V.



Competition between anneal and flux?

The highest the flux, the highest degradation rate.

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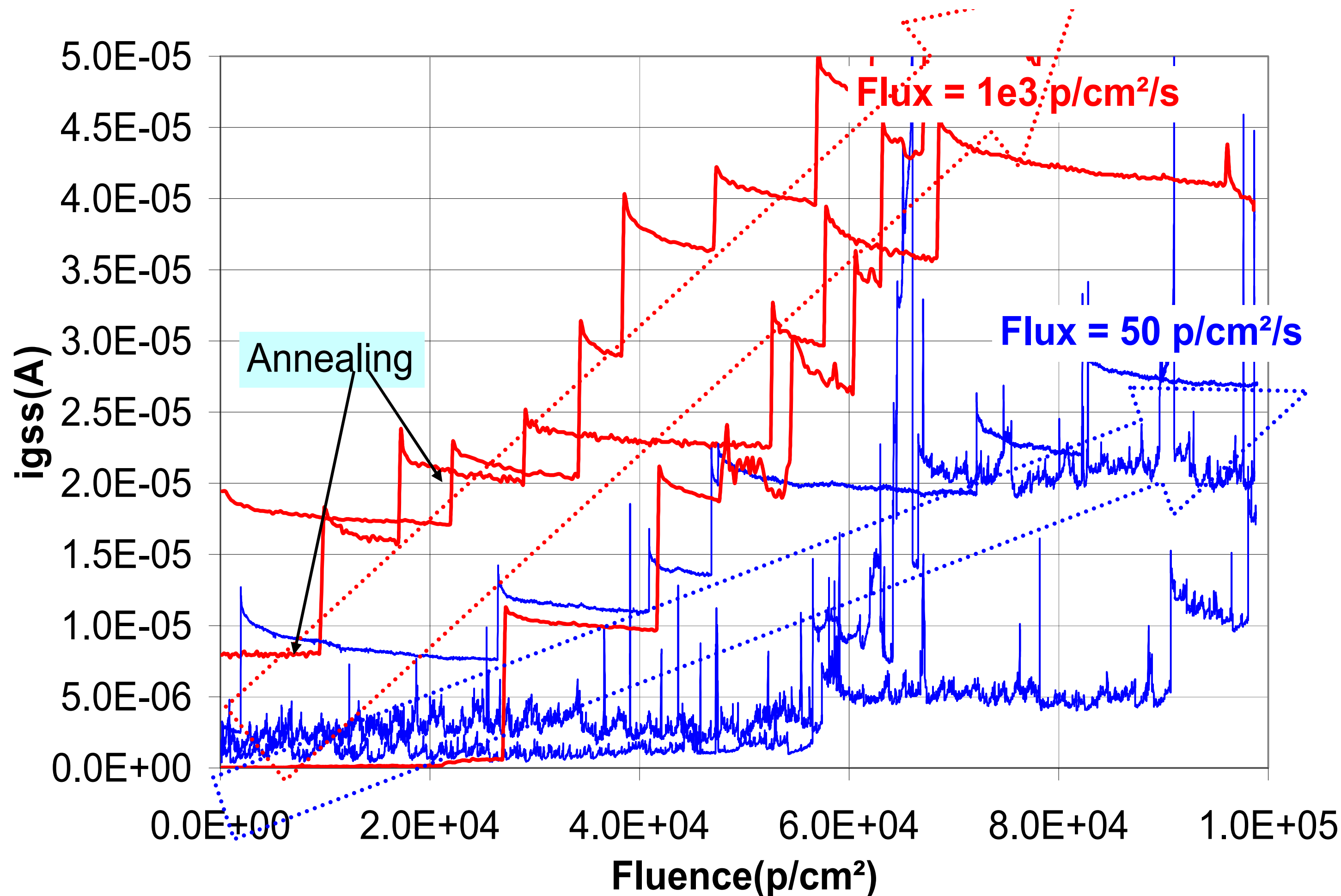
4. Experimental results : Flux effect (P channel) (5)

IRFF9120 P channel gate degradations.
LET = 34 MeV.cm²/mg (Kr), Range = 43 µm, Vds = 100 V, Vgs = 15 V



Competition between anneal and flux?

The highest the flux, the highest degradation rate.

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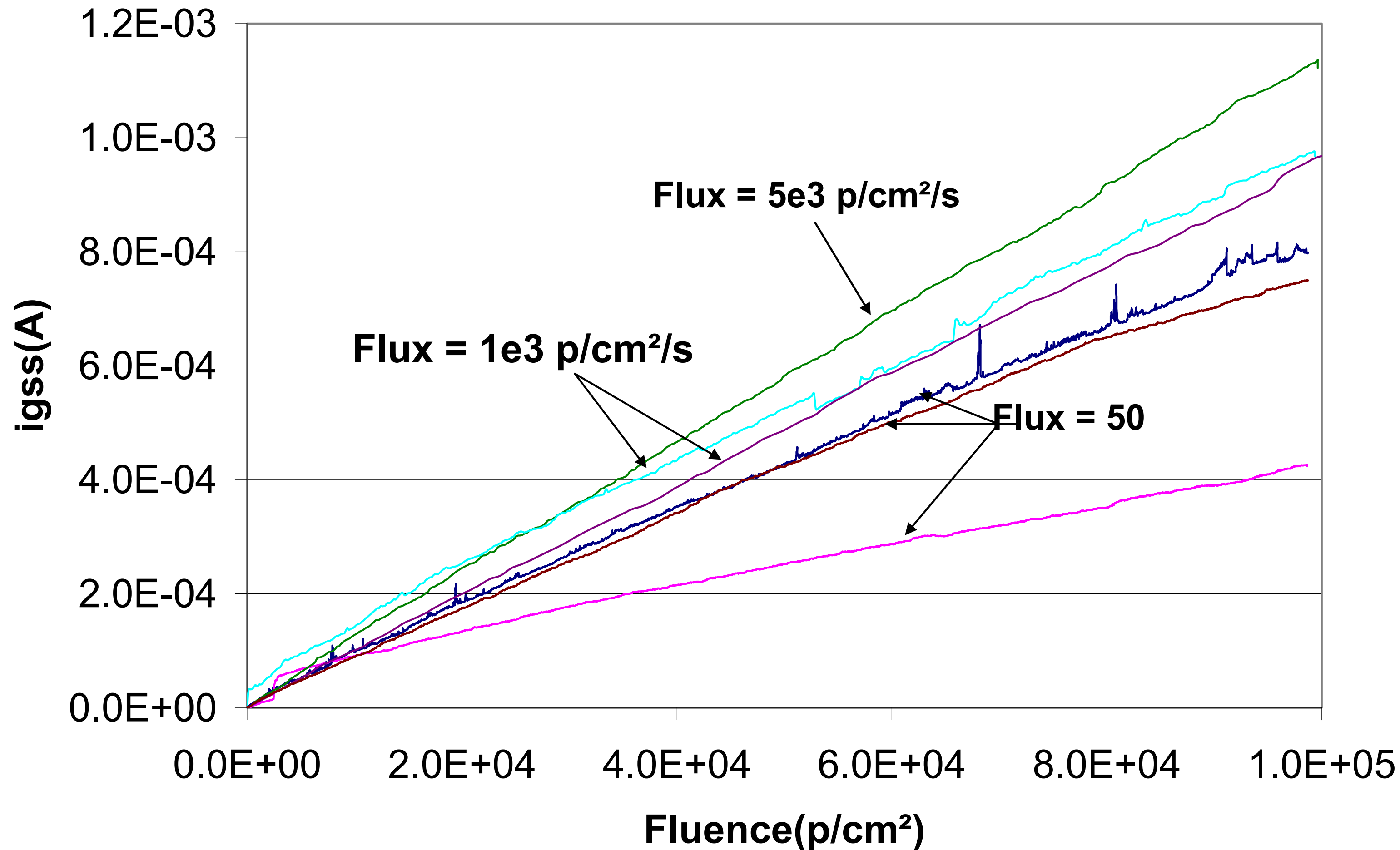
4. Experimental results : Flux effect (P channel) (6)

STB80PF55 gate degradation for several fluxes. Vds=-55V, Vgsoff=15V. Kr (LET =34, Range = 43 µ)



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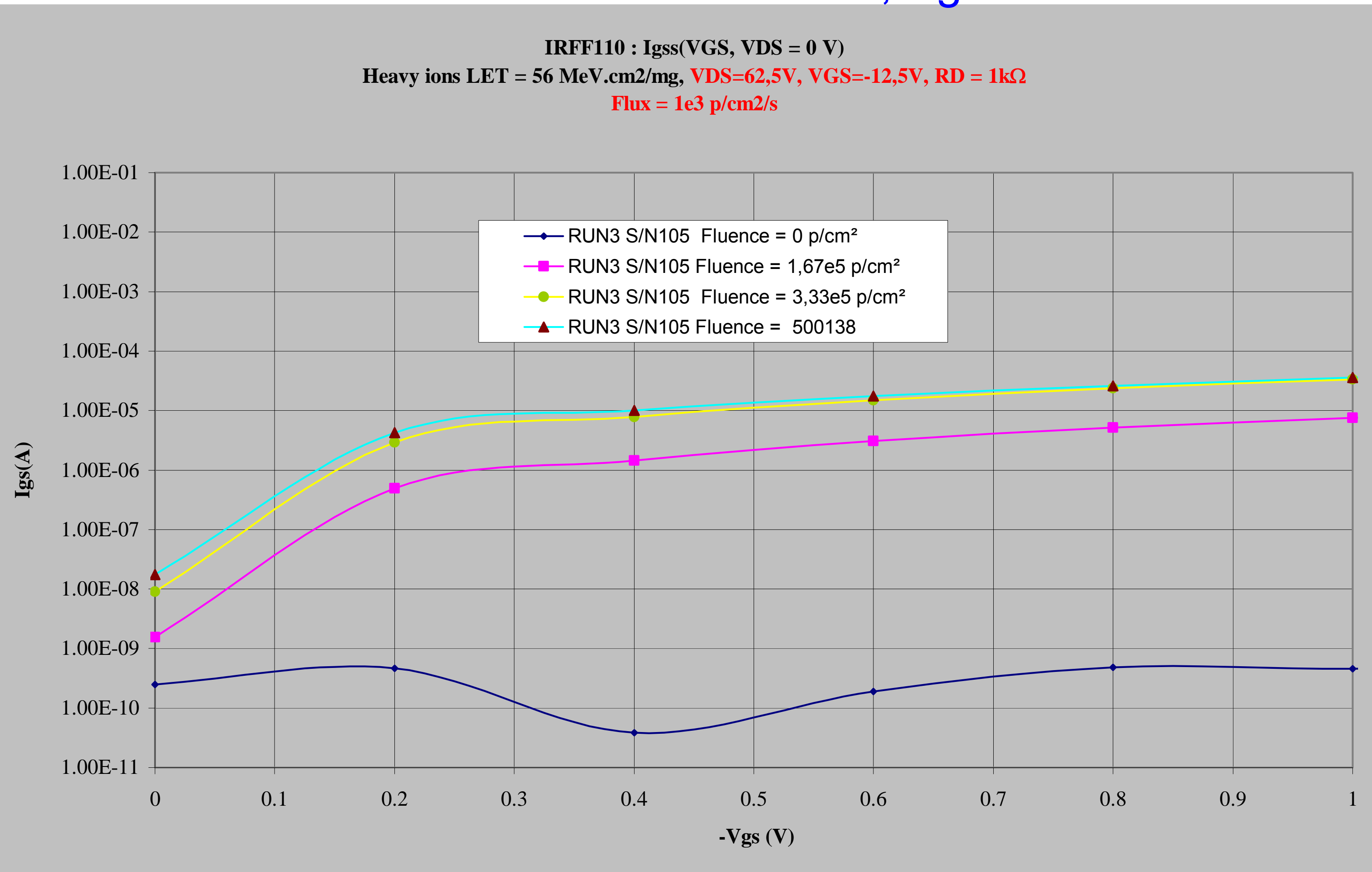
4. Experimental results : Post gate stress test (IRFF110, 100V N channel) (7)

Igs(Vgs, Vds=0V) post-irradiation measurement.
Irradiation conditions: Vds=62V, Vgs=-12V

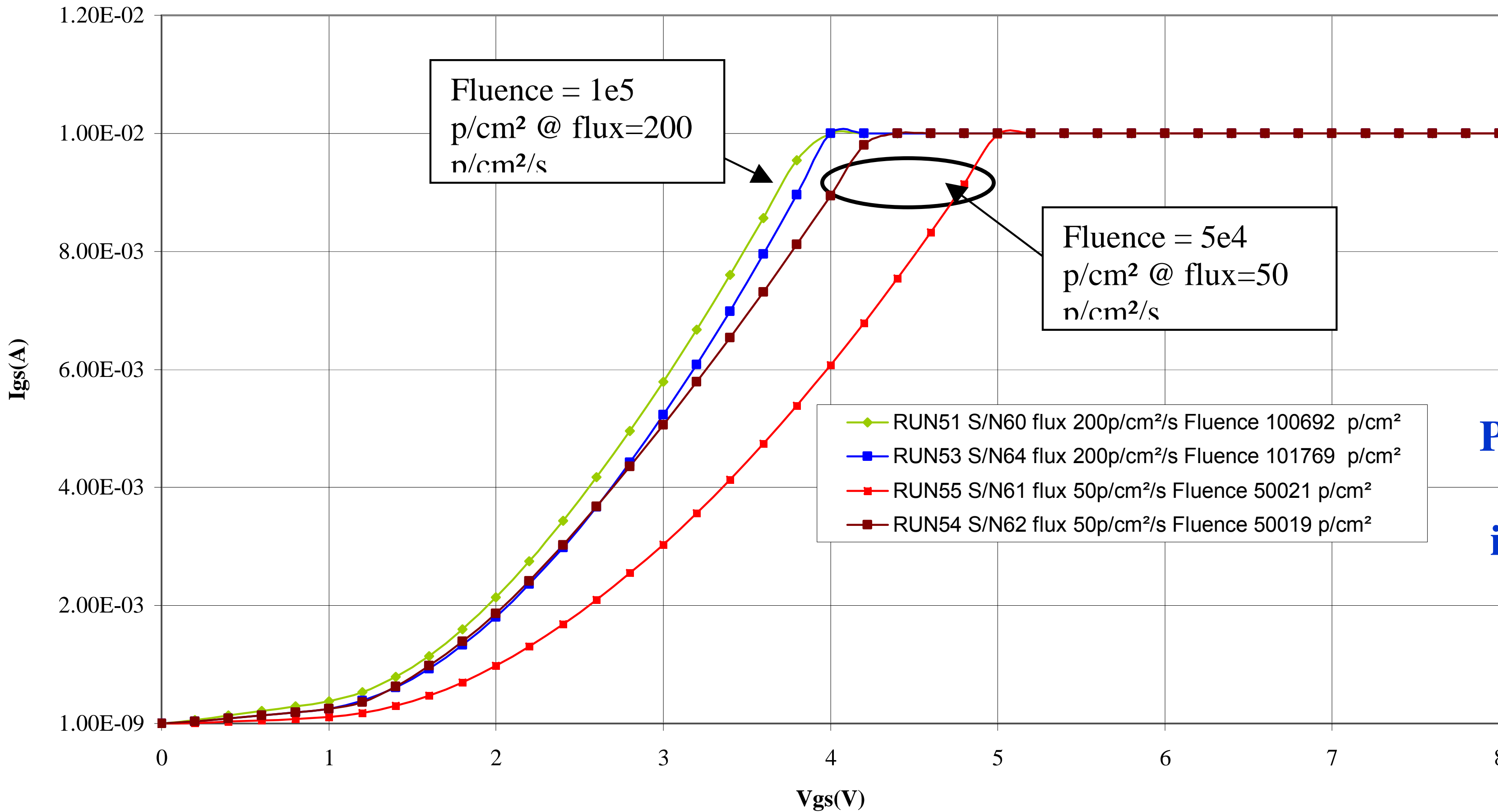


« SEGR » status is dependent on the Vgs

At Vgs = 0V, Negligible leakage.

Perfectly working transistor in switched mode (Vgsoff=0)

4. Experimental results : "Post gate stress test" (STP80 NF10, 100V N channel) but with Vds ≠ 0 (8)



Igs (Vgs=0) negligible

Perfectly working transistor in switched mode (Vgsoff=0V)

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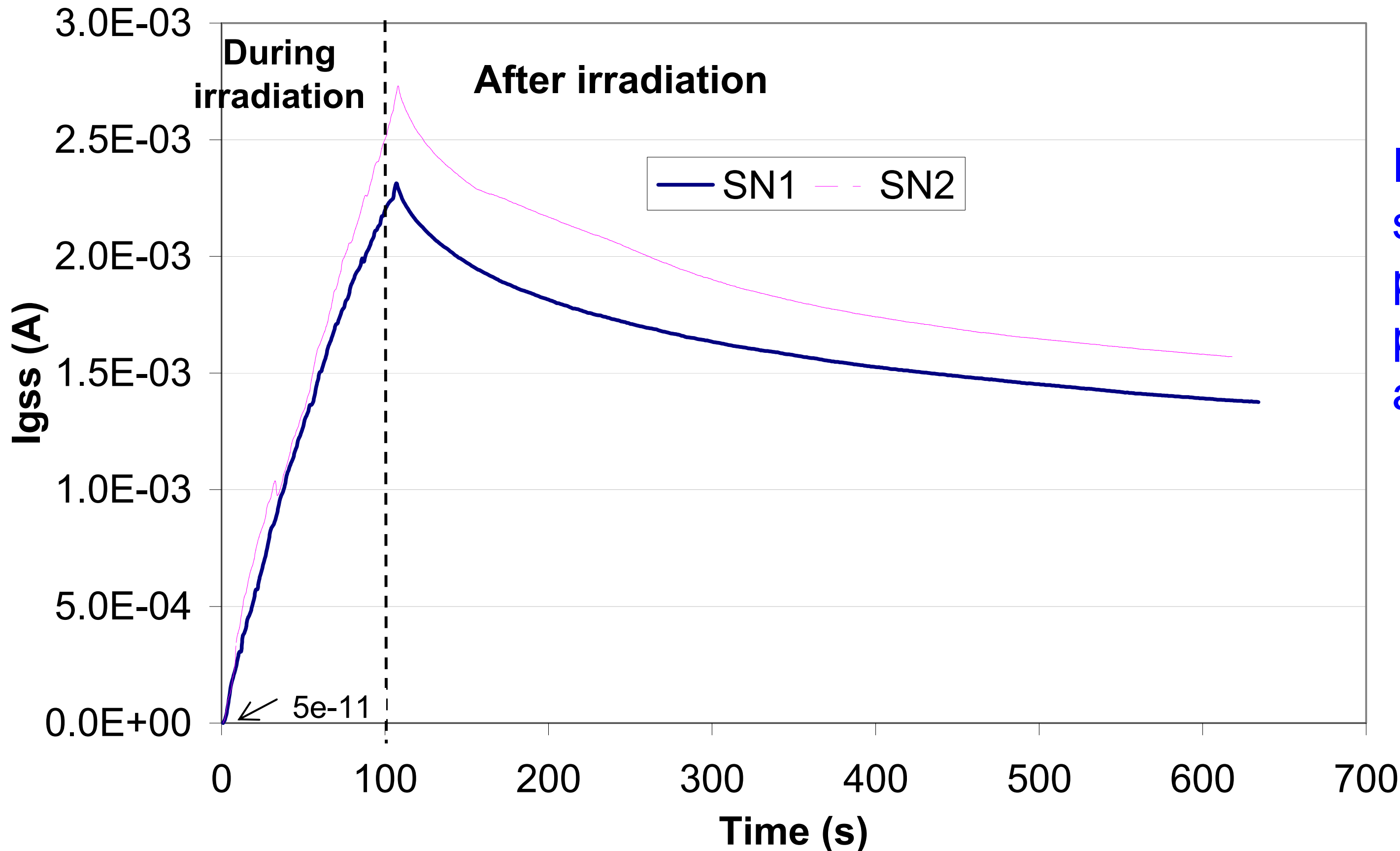
4. Experimental results : ΔIgss Annealing (P channel) (9)

Igss evolution during and after irradiation STB80PF55,
(P channel, Vds = 80%, Vgs = +5 V), Kr (LET =34, Range =92µ) ,
flux = 500 p/cm²/s , Fluence ~ 5e4 p/cm²



Igs(Vgs) would lead to same type of curve as previously (STP80NF10) if performed immediately after irradiation.

4. Experimental results : ΔIgss Annealing (P channel) (10)

STP80PF55 Igss anneal

Igss (A)

3.0E-03
2.5E-03
2.0E-03
1.5E-03
1.0E-03
5.0E-04
0.0E+00

At the end of irradiation

After irradiation in static mode

500 p/cm²/s

50 p/cm²/s

100 nA = Spec level defining "SEGR" limit

300 µA

Igss init | Igss_irr @ End irr | Irr + few min | Irr + 2 days | Irr + 14 days | Irr + 24 days

Competition between anneal and flux

Igs(Vgs) would lead to same type of curve as previously (STP80NF10) if performed immediately after irradiation.

This curve would be different after anneal

Flux effect on P channel STB80PF55 gate degradation annealing, after 5e4 p/cm², LET=34, Range=92µ.

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4. Experimental results : preliminary conclusion on gate degradation (11)

ΔIgss negligible at Vgs=0V

Switched mode exhibits lower degradation rate

Every parts could perfectly switch [Vgsoff=0, Vgson]

Anneal at ambient T° showed an Igss recovery of >~2 mA :

a ΔIgss≥~100 nA (spec. definition of "SEGR") is expected to recover.

According to MIL STD-750 spec, parts would be rejected since ΔIgss > 100 nA after several 10^5 p/cm² !

No proof that gate degradation measured at Vgsoff max-rated (post gate stress test, i.e. almost dielectric avalanche conditions) is related to a "single ion".

The lower the flux, the lower the gate degradation rate: a cumulative phenomena is highlighted, especially far from avalanche conditions.

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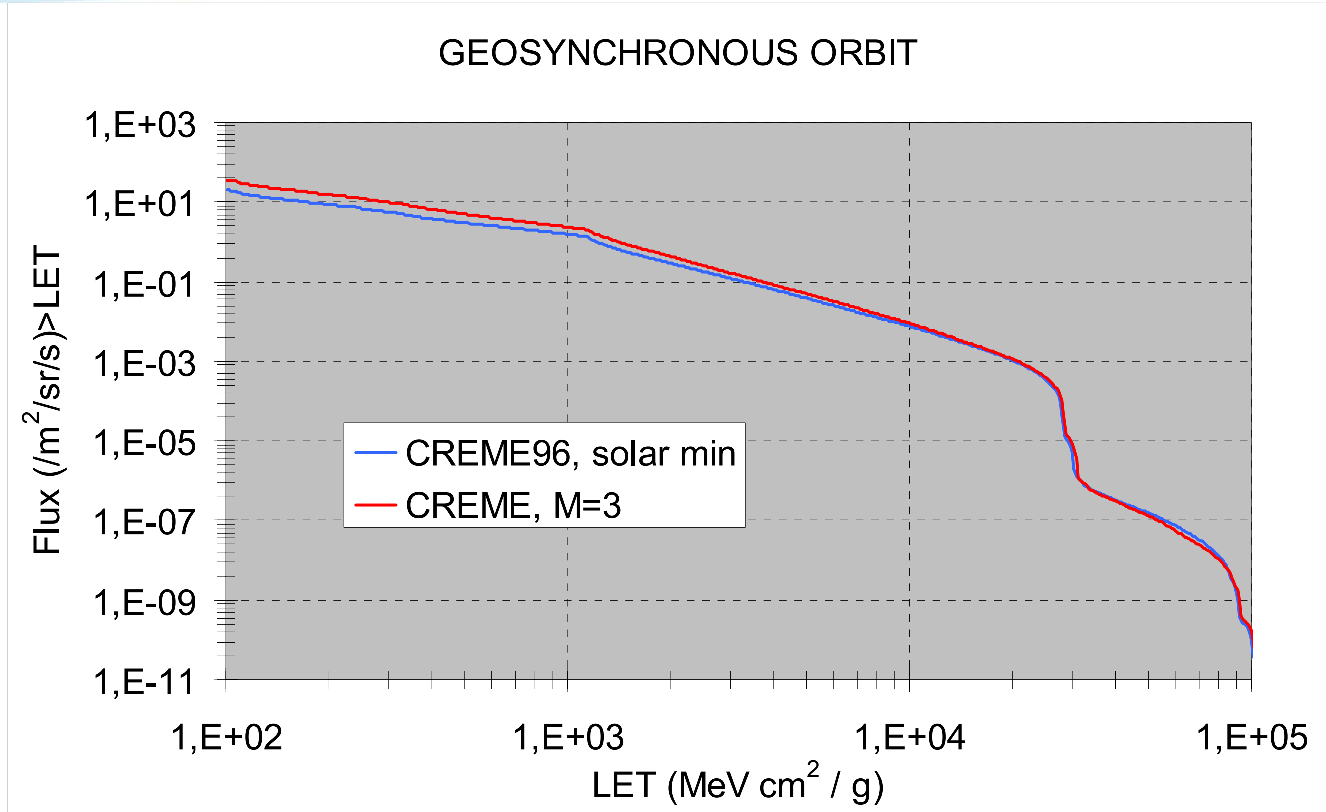
5. CONSEQUENCES (1)



- Mission duration : 15 years

Total fluence @ LET ~ 5,6e4 MeV/cm²/g , after 15 years @ M=3:

Space fluence : Φ = 5e-2 p/cm², at space flux ~ 1e-10 p/cm²/s to be compared to test fluence : Φ = 1e5 p/cm² at test flux [1e3 ; >1e4] p/cm²/s

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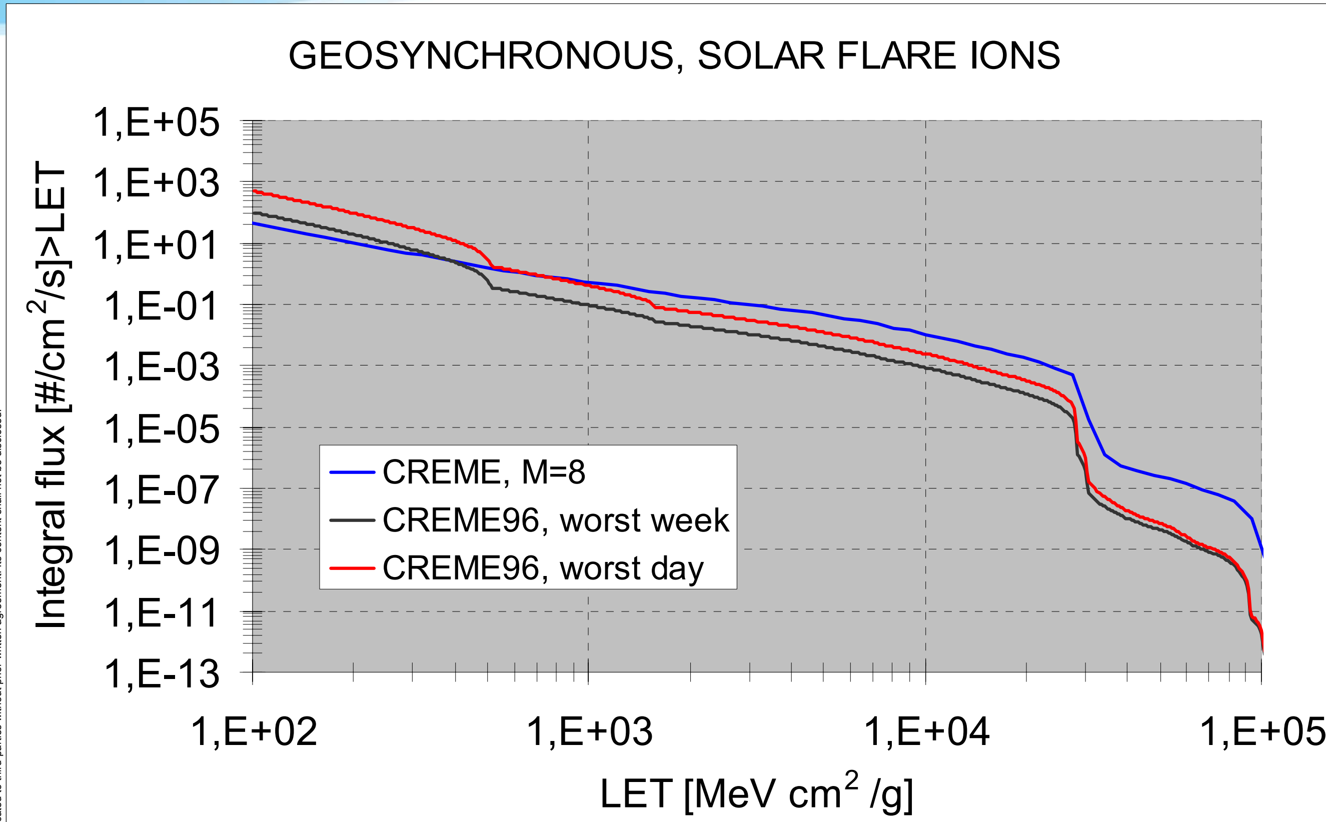
5. CONSEQUENCES (2)



- Flare duration = 4*4days in 15 years

- **Total fluence @ LET ~ 5,6e4 MeV/cm²/g after 16 solar flare days :**

Space fluence : Φ = 0.20 p/cm², at space flux ~ 1e-7 p/cm²/s to be compared to test fluence : Φ = 1e5 p/cm² at test flux ~ [1e3 ; >1e4] p/cm²/s

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6. CONCLUSION

Based from these experimental results, one can conclude the following:

- Gate degradation appears to be a cumulative effect mainly driven by the high flux used for ground testing.
- Gate degradation as being defined by specification as single ion related appears to be questionable (Post-gate stress test).
- "SEGR" defined as a pure probabilistic phenomenon is questionable.
- « SEGR » phenomena is expected as improbable in SPACE conditions, especially within no over-blocking conditions (far from dielectric avalanche conditions).
- Non RH Channel P Mosfet could be used for space applications (GEO and LEO) especially if used far from dielectric avalanche conditions
- Further investigations are necessary that will most probably lead to an upgrade of the testing standards.

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