HIREL EXPERTISE
HIREX
ENGINEERING
Alter Technology Group

SEE testing of Advanced Memories - Part 1

- Test approach and hardware evolution from SDRAM to DDR2
- Sample preparation

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Plan

- Work context
- Overview of DRAM technologies
- SEE test approach of SDRAM, DDR and DDR2
- Application to SDRAM
- Evolution to DDR2 SDRAM
- Sample preparation

Context of the work

- To answer ESA needs on evaluation of new generations of SDRAM, DDR, DDR2
- March 2006 → Kick-Off of a ESA contract to evaluate SDRAM, DDR and DDR2 memories to SEE
- June 2006 → SEE tests of SDRAM in UCL/HIF
- November 2006 → SEE tests of DDR2 in UCL/HIF
- *November 2006 → SEE tests of DDR2 in Los Alamos/LANSCE (outside ESA contract)*
- January 2007 → first presentation of DDR2 preliminary results at QCA Day 2007

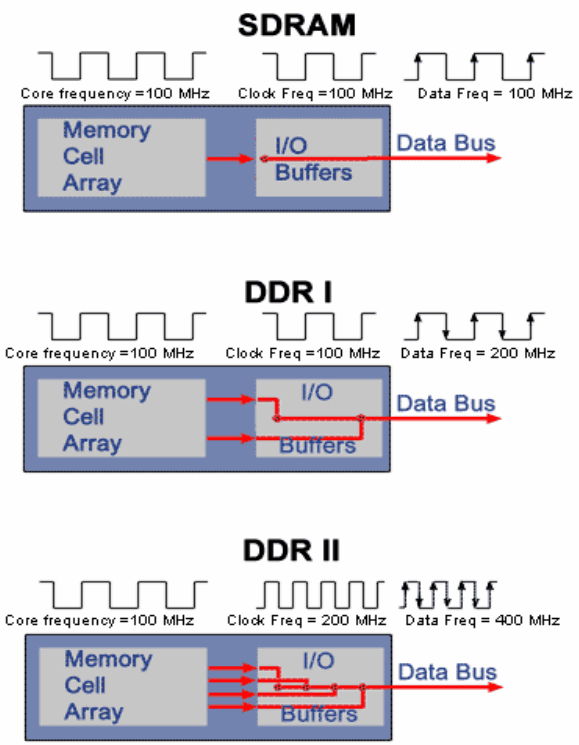
Overview of SDRAM technologies (1/2)

- Definition
  - SDRAM → Synchronous Dynamic Random Access Memory
  - DDR SDRAM → Double Data Rate SDRAM
  - DDR2 SDRAM → upgraded DDR

- Main common points
  - Synchronous
  - Volatile memory → periodic refresh needed
  - Access is burst oriented
  - Address defined by a row, column and bank
  - Auto Refresh and Self Refresh modes

Overview of SDRAM technologies (2/2)

- Main differences



- 3.3V
- TSOP package
- 133 MHz max

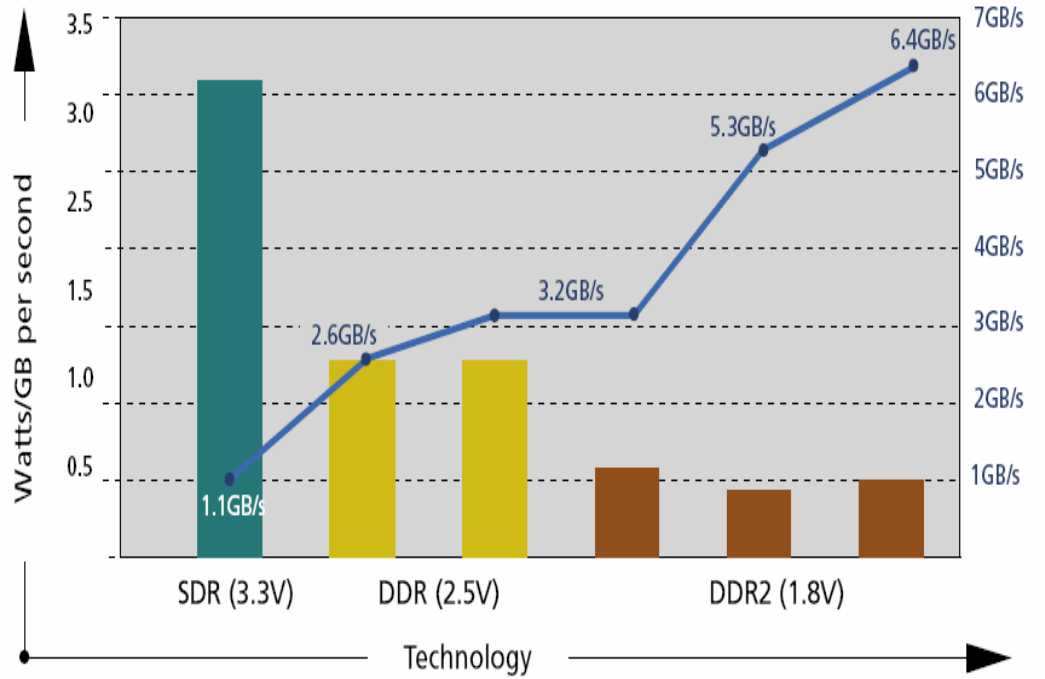
- 2.5V
- TSOP and FBGA packages
- 90 MHz min, 200 MHz max*
- Differential signals

- 1.8V
- FBGA package
- 125 MHz min, 333 MHz max*
- Differential signals

+ data rates, capacities increased... due to new generations

Interests of new generations of SDRAM for space applications

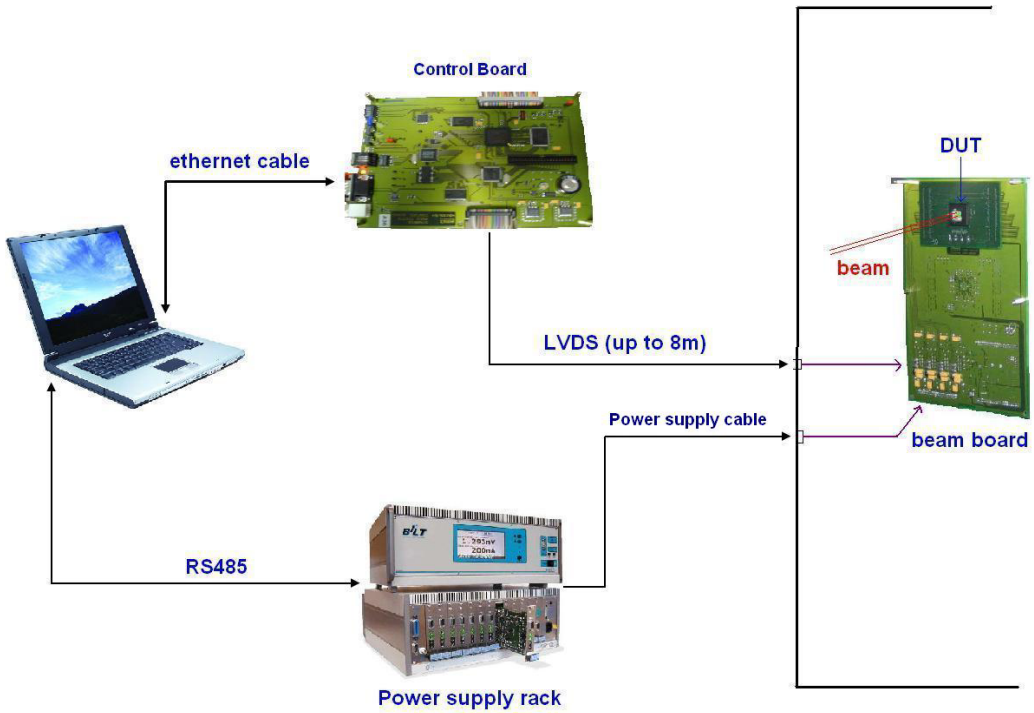
- Obsolescence
- Consumption
- Capacity, data rate



Source: Micron website

SEE test approach of SDRAM, DDR and DDR2

- Current Hirex digital test system



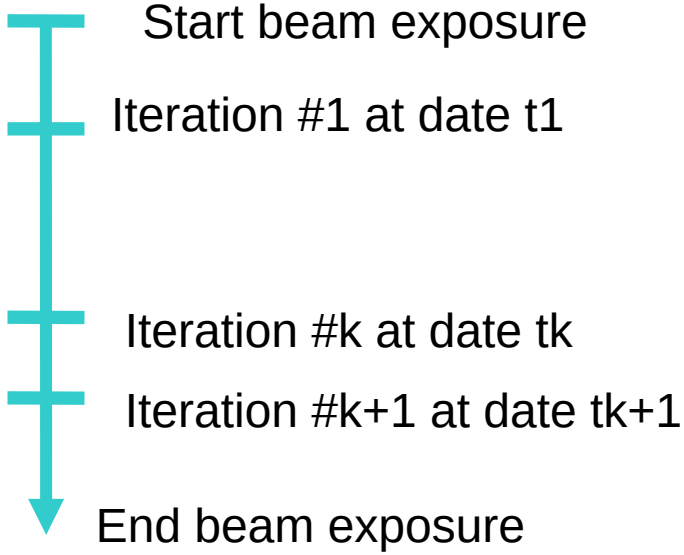
- Compatible with most of facilities (neutron, protons, heavy ions, alphas, laser)
- 120 I/Os up to 100MHz from 0.8V to 5V
- 4 supplies up to ±5V/1A with µs latchup processing and recording
- more than 100K SEE error records
- Heating up to 125°C
- TCP/IP@10M network
- Robust hardware & software
- Fully remote configuration

SEE test approach of SDRAM, DDR and DDR2

- What is a SEE run ?

A run = 1 test configuration (DUT, supply values, pattern, test mode, etc.)

T=0, Test initialisation



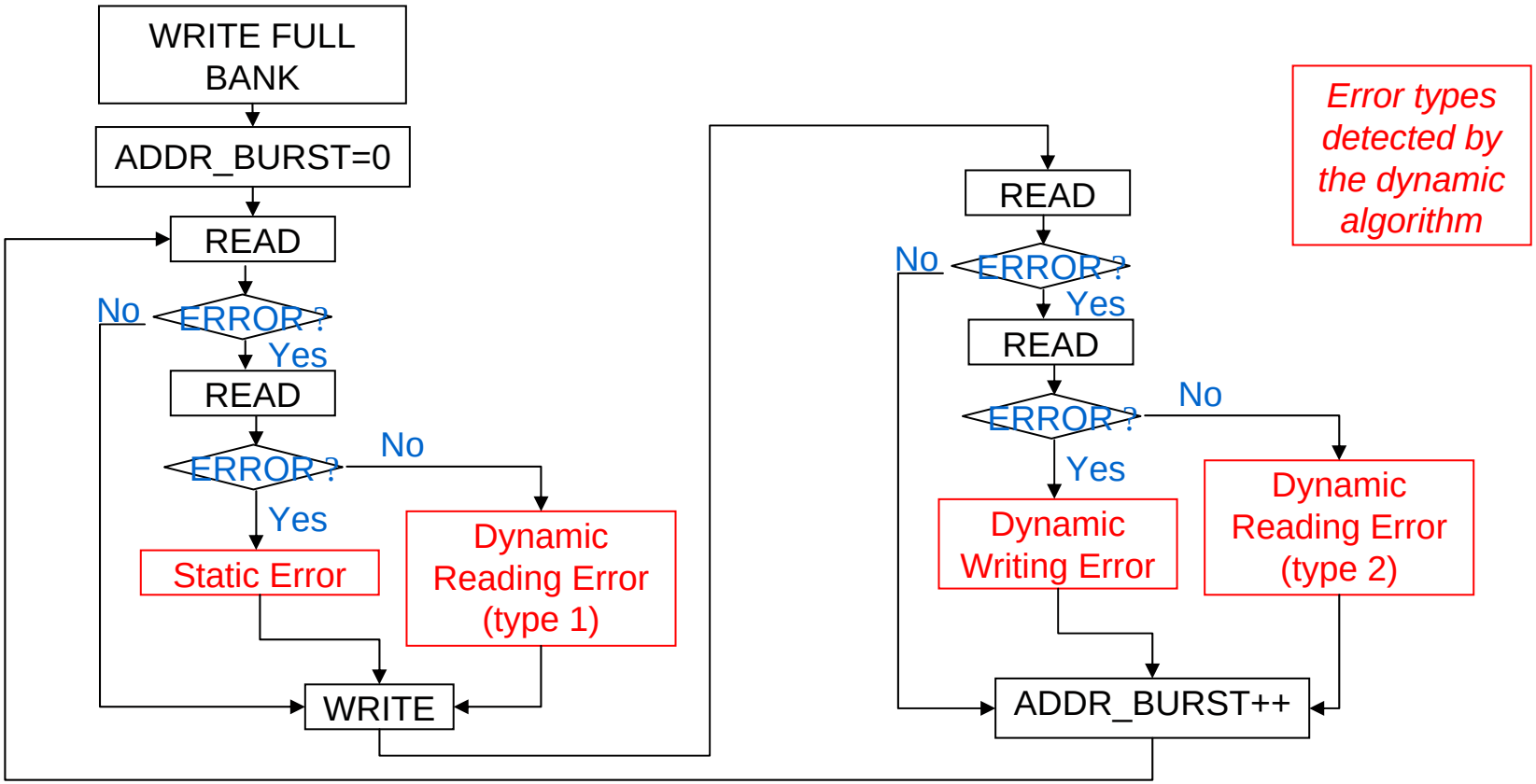
Note: a common static iteration is a bank(s) write(s), an exposure time while refreshing and a bank(s) read(s)/comparison(s)

SEE test approach of SDRAM, DDR and DDR2

- Run Test Modes
  - Static (use of a shutter during write and read)
    - Consecutive write from 1 to 4 banks
    - Refreshing during exposure time (self or parametric auto refresh)
    - Consecutive read of selected banks
    - Idem for the next iteration
  - Dynamic
    - Consecutive burst access of a selected bank with a no iteration time
- Pattern (ALL0, ALL1, Checkerboard and inverted...)

SEE test approach of SDRAM, DDR and DDR2

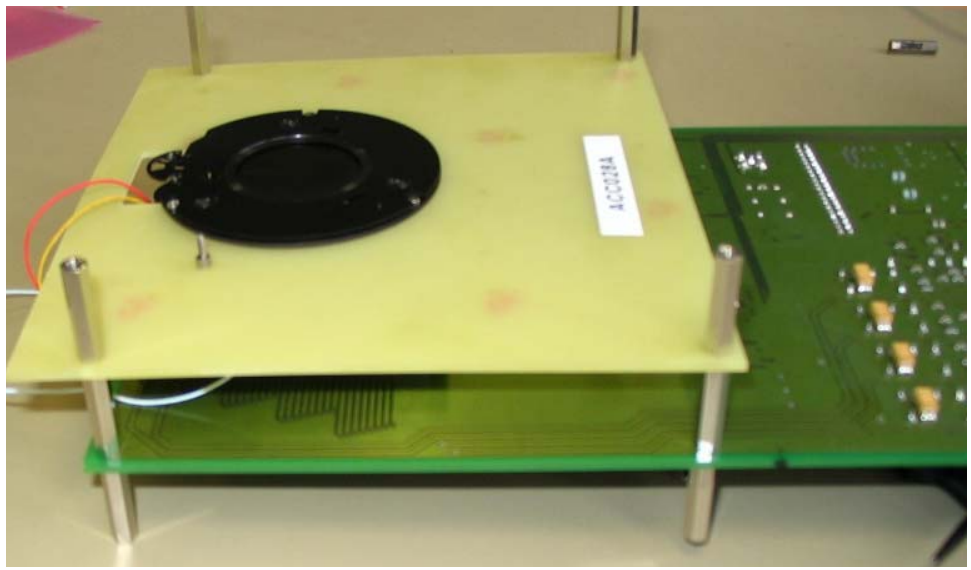
- Dynamic mode Algorithm



⇒ Detects both static errors and dynamic errors

SEE test approach of SDRAM, DDR and DDR2

- Protections against entering into an unknown state
  - For the DUT(1/2)
    - Use of a photographic obturator for static tests during Write and Read (automatically controlled)



⇒ Physical protection (heavy ions only)

SEE test approach of SDRAM, DDR and DDR2

- Protections against entering into an unknown state
  - For the DUT(2/2)
    - Automatic detection of unknown state during read
      - Reload of the memory registers
      - Reread of the memory without rewriting it
        - if unknown state can be recovered by software → Count a “Soft SEFI”
        - if unknown state can only be recovered by power off the DUT (automatic power OFF and re-power ON) → Count a “Hard SEFI”
  - For the control circuitry under harsh environment (protons, neutrons)
    - Periodic reload of the FPGA which drives the memory

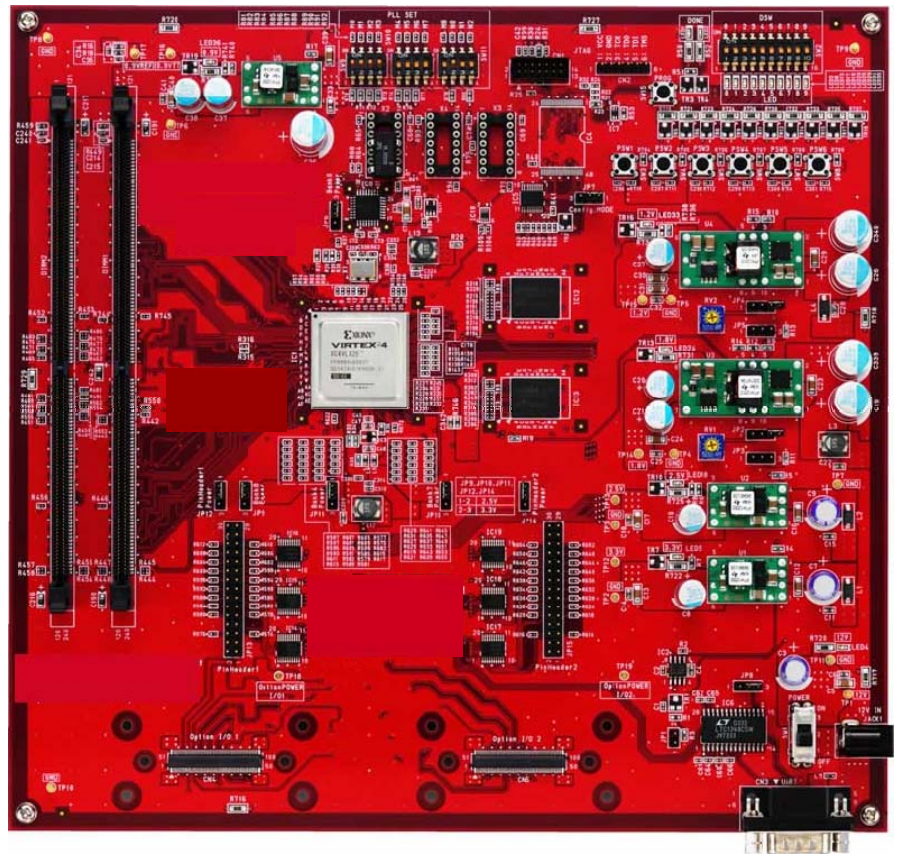
⇒ Software protections

SEE test approach of SDRAM, DDR and DDR2

- Detected errors types
  - SEU: Single Bit error
  - MCU: Multi Cell Error (scrambling info needed)
  - MBU: Multi Bit Error (in the same word)
  - Row/Column error
  - Read errors, Write errors, Cell errors
  - Soft SEFI (registers modification possible)
  - Hard SEFI (when power reset is needed)
  - SEL

Application to SDRAM and DDR2

- SDRAM
  - Current Hirex test system based on a Xilinx FPGA Virtex2
- DDR2
  - Current Hirex test system
  - + one additional board based on a Xilinx FPGA Virtex4



Performances of the test systems

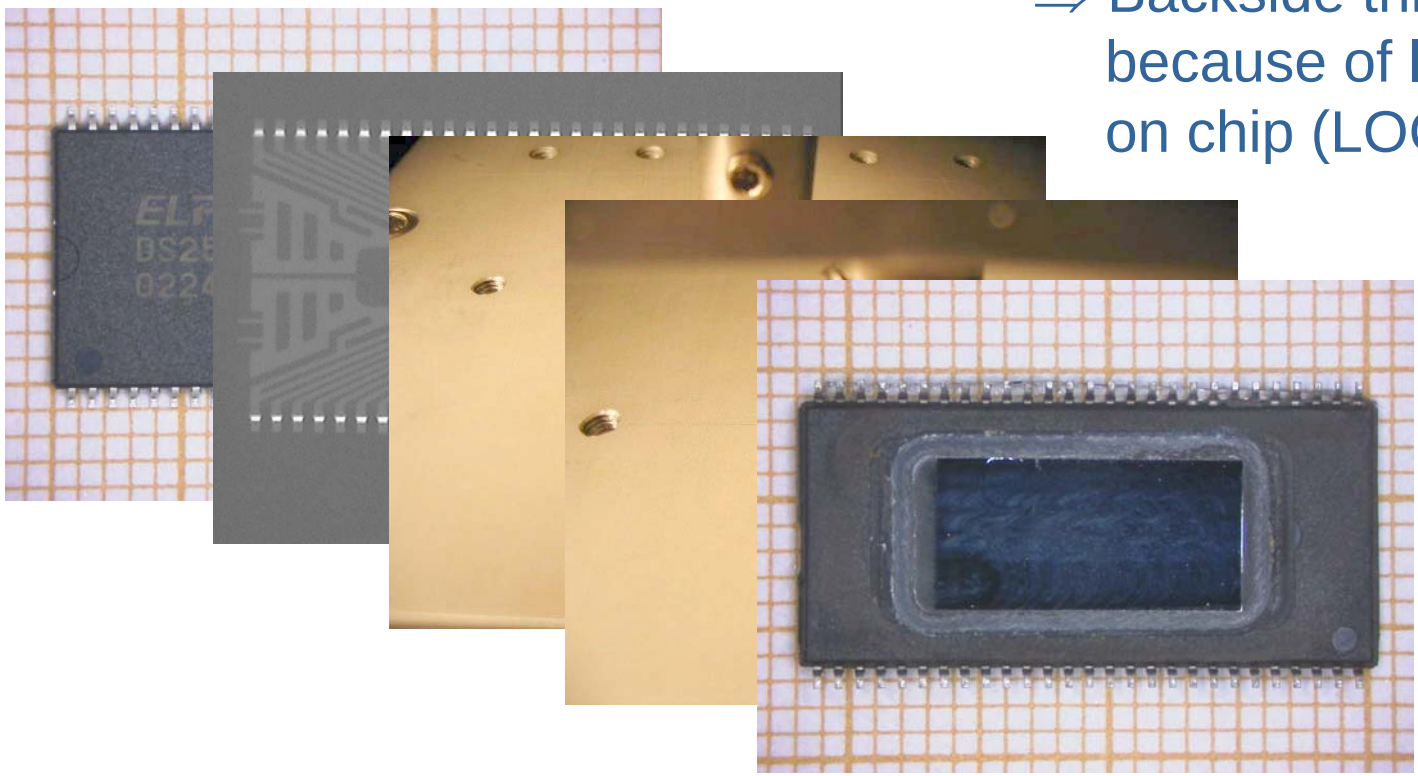
Test SEE of	SDRAM	DDR2	DDR2	DDR2
Campaign	UCL - June 2006	UCL - Nov. 2006	Los Alamos - Nov. 2006	Expected in 2007
Frequency	25 MHz	166 MHz	200 MHz	200 MHz
% accessing time	-	~30%	~25%	~50%

Sample preparation

- Using Hirex Physical Analysis Lab resources (equipped for Construction Analysis, DPA, Failure analysis)
- Preparation of SDRAM/DDR2 memories for heavy ions radiation testing:
  - Chemical etching (jet etcher)
  - Die thinning (ASAP1 / mechanical lapping)

Sample preparation

- Application to SDRAM

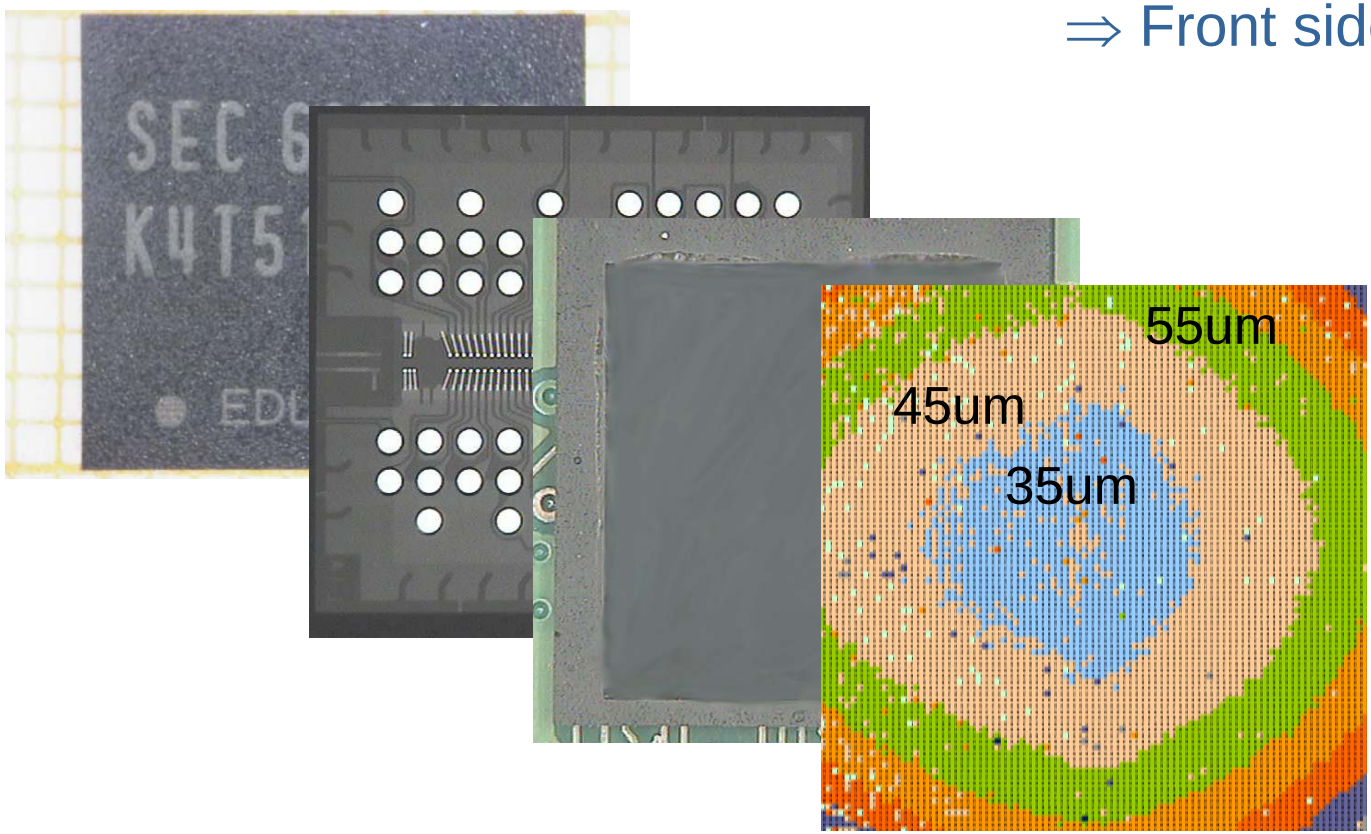


⇒ Backside thinned because of lead frame on chip (LOC)

Sample preparation

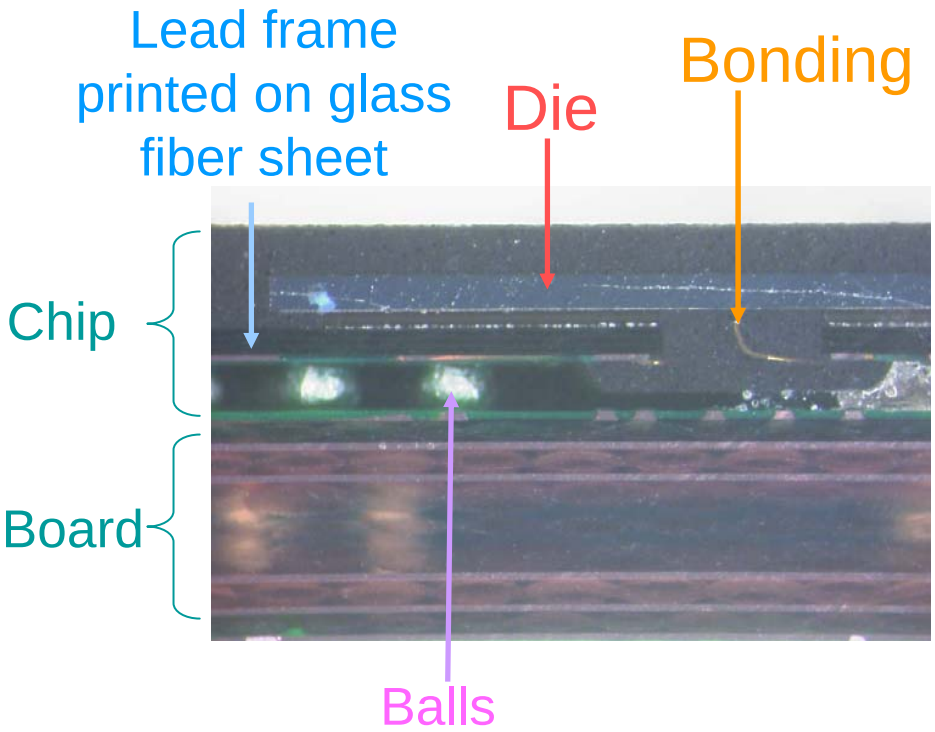
- Application to DDR2 (1/2)

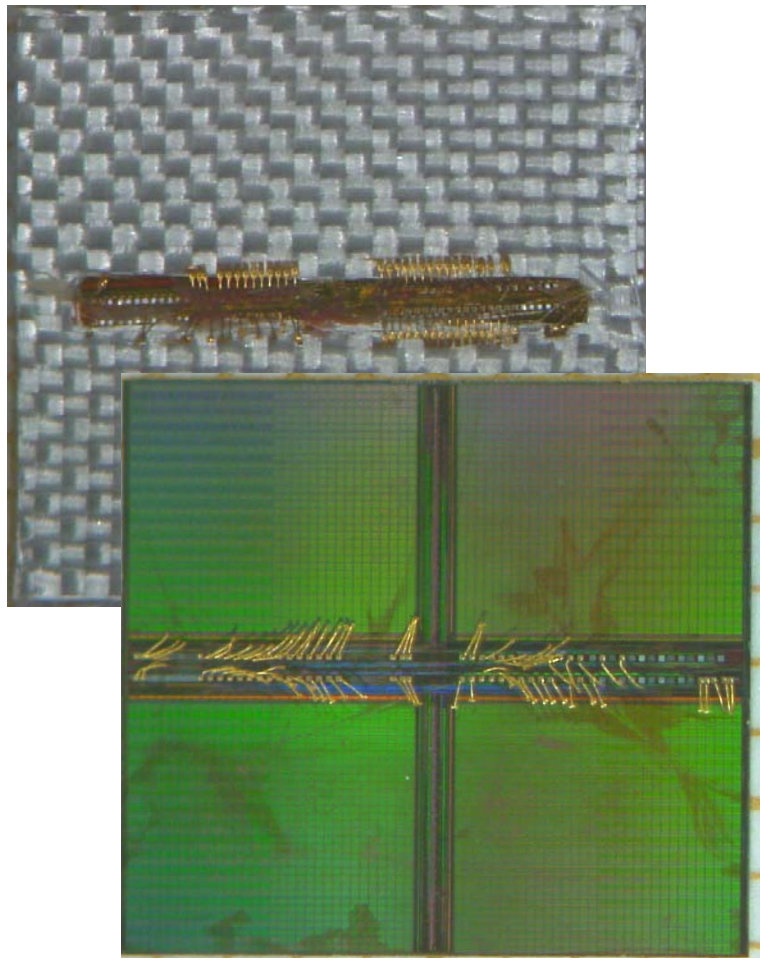
⇒ Front side thinned



Sample preparation

- Application to DDR2 (2/2)





Conclusion

- Achievements
  - SEE tests of 3 SDRAM and 2 DDR2 (heavy ions and neutrons)

⇒ First results for DDR2. See « SEE testing of Synchronous Dynamic RAM - Part 2 » presentation

  - Conception and validation of a prototype for an upgraded test system

⇒ Allow SEE tests of new generations of advanced memories (DDR2 up to 400Mb/s, RLDRAM, QDRAM...)

  - Validation of the different error detection and process (Soft SEFI, Hard SEFI...)
- Next
  - Design and production of improved ASERT test board (4 power supplies, 488 I/Os, up to 500 MHz for FPGA clock speed...)
  - In depth radiations tests on different DDR2 memories