HIREL EXPERTISE
HIREX
ENGINEERING
Alter Technology Group

SEE testing of Advanced Memories - Part 2

- SEE tests results on SDRAM (heavy ions)
- Preliminary SEE tests results on DDR2 (heavy ions and neutrons)

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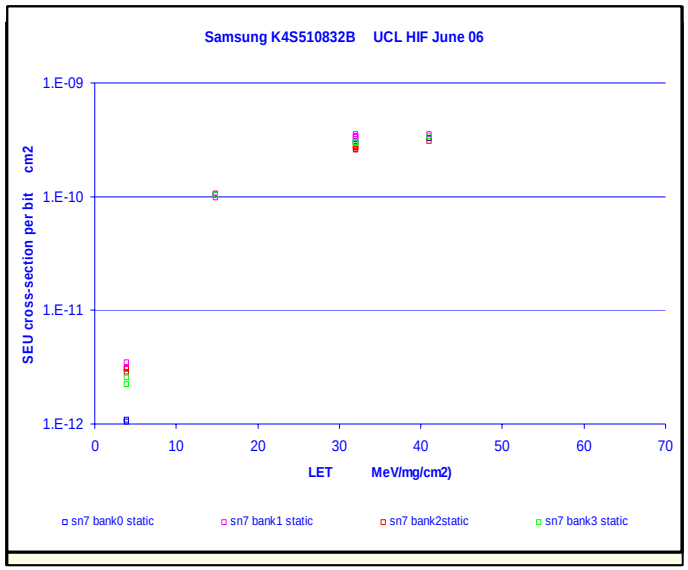
Plan

- Tested devices
- SEE test data analysis
- Effective LET correction
  - Effective LET correction
  - Descrambling process
- SDRAM heavy ions results
- Preliminary DDR2 results (heavy ions and neutrons)

Test devices

- SDRAM (heavy ions)
  - Hyundaï HY57V651620BLTC-10S → 64Mbits - 16 bits - TSOP-54
  - Samsung K4S510832B-TC75 → 512Mbits - 8 bits - TSOP-54
  - Hitachi/Elpida HM5225805BTT-75 → 256Mbits - 8 bits - TSOP-54
- DDR2 (heavy ions and neutrons)
  - Samsung K4T51083QC-ZCD5T → 512Mbits - 8 bits - FBGA-60
  - Infineon HYB18T512800AF-3.7 → 512Mbits - 8 bits - FBGA-60

SEE Test results analysis per run



- Supplies recording and SEL detection / supply
- Beam flux and fluence monitoring

⇒ *effective fluence (shutter, SEL and SEFI process time…)*

- SEU physical mapping / bank

⇒ *check for all types of error, selection of zones with adequate die thickness,...*

- SEU repartition / data bits

⇒ *check for Stuck bits, Row/col errors*

- SEU Cross section per bit versus LET

⇒ *sensitivity of the device cells*

Effective LET correction (1/4)

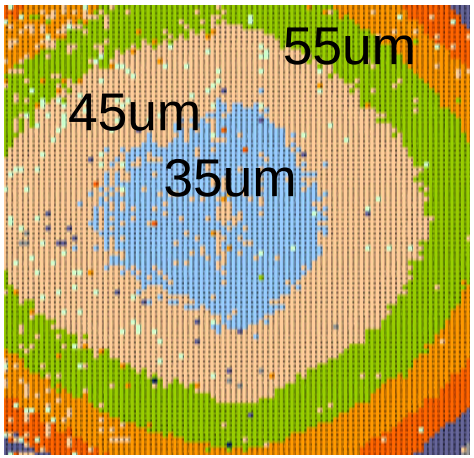
- Need because die thickness could vary along die area

→ Effective LET varies → SEU count varies → Cross section varies because of thickness sample and not because of beam parameters

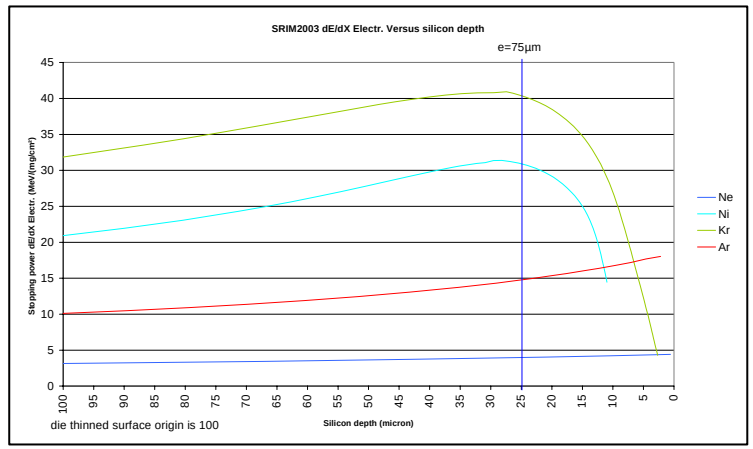
⇒ SEU Cross-section per bit is computed using die thickness cartography + physical mapping of the errors

Effective LET correction (2/4)

- Effective LET correction cartography of the thinned die



Thickness mapping

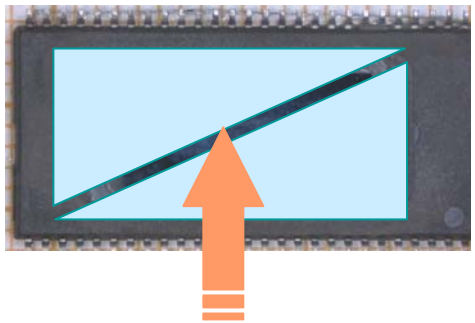


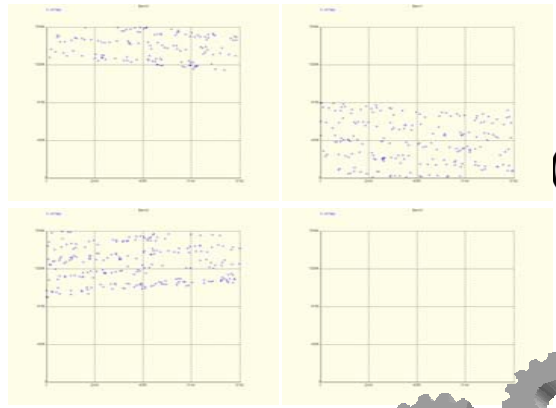
Effective LET versus thickness
source: SRIM simulation

Effective LET cartography
of the thinned die

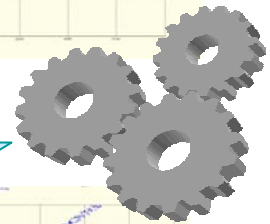
Effective LET correction (3/4)

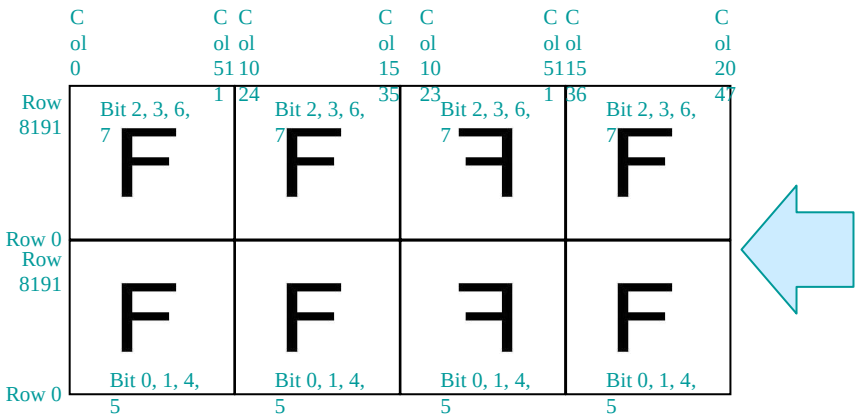
- Need of the physical scrambling of the addresses and bits on the die

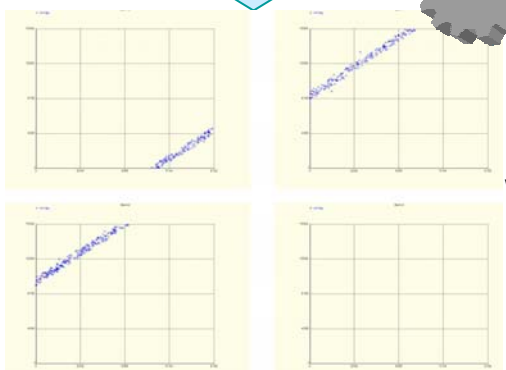




SEU mapping (logic address)



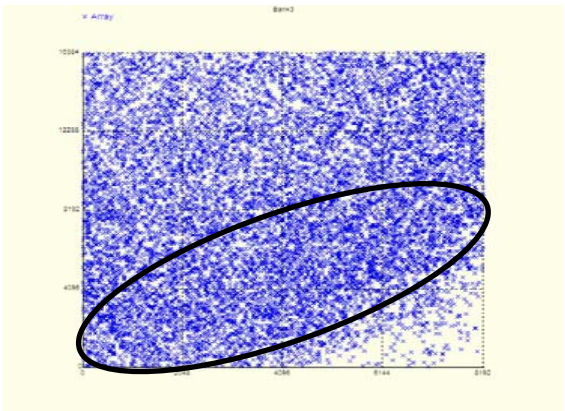




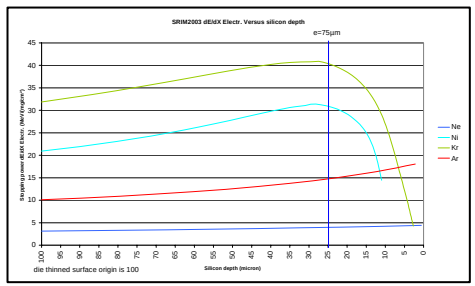
SEU mapping with scrambling algorithm

Effective LET correction (4/4)

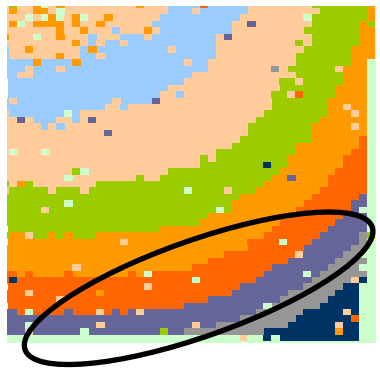
- Effective LET cartography + SEU mapping scrambling
  - ⇒ Corrected cross section of SEU versus LET
  - ⇒ Explanation of areas with more SEU than others + selection of better die areas for SEE analysis
- Example of over SEU on a dedicated area



Bank n°4 SEU mapping



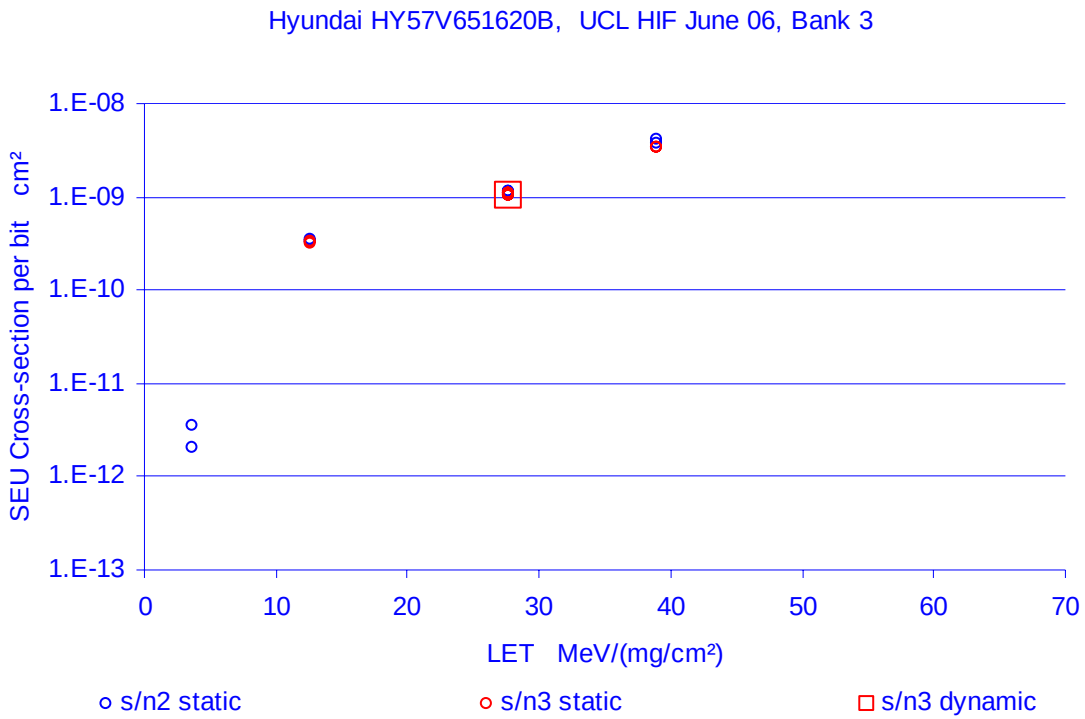
LET Eff. Vs thickness



75um

Bank n°4 Thickness

Hyundaï HY57V651620BLTC SDRAM heavy ions results



No SEL event up to a LET of ~ 39 MeV/(mg/cm²)

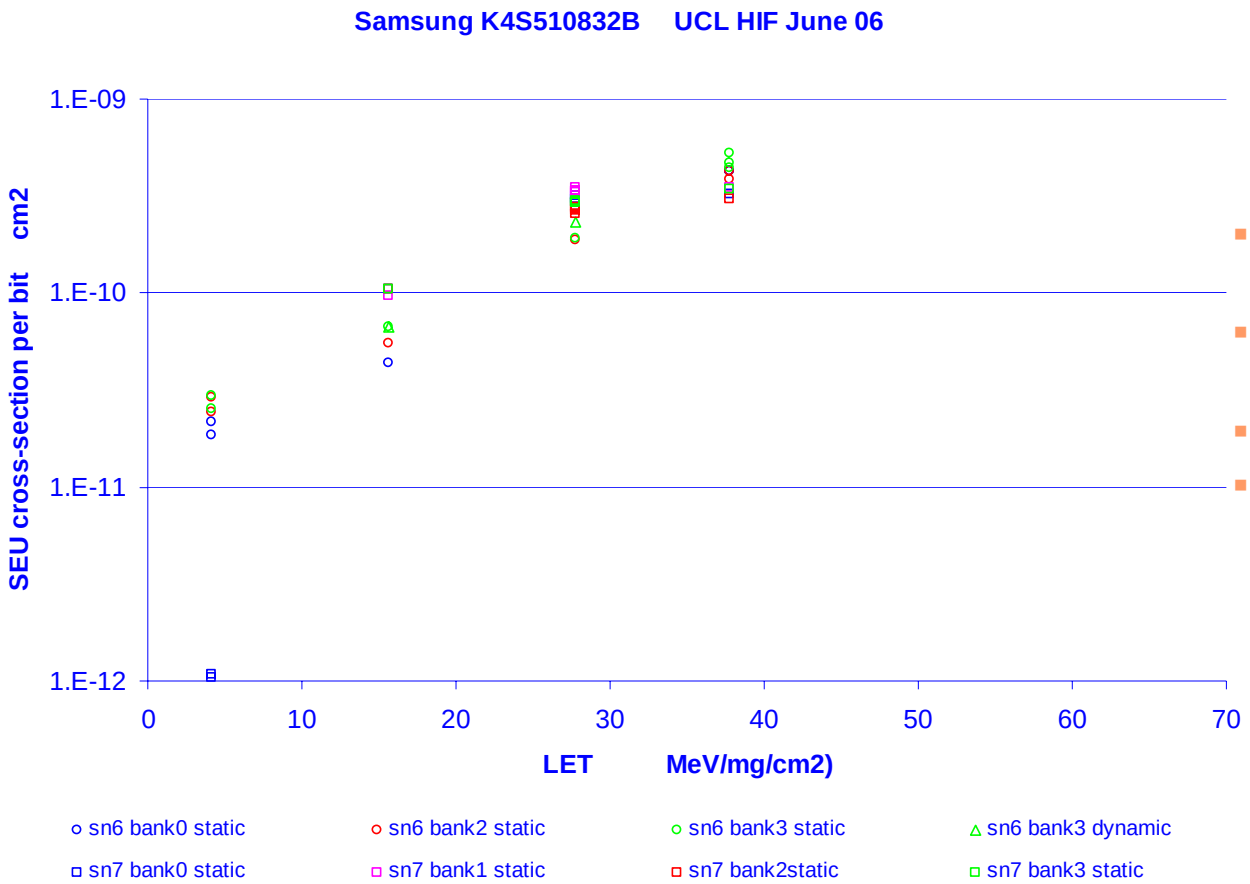
SEU error cross-section / bit ~ 3.5 E-9 cm²

ROW errors and « hard » SEFIs

No significative influence of variations of :

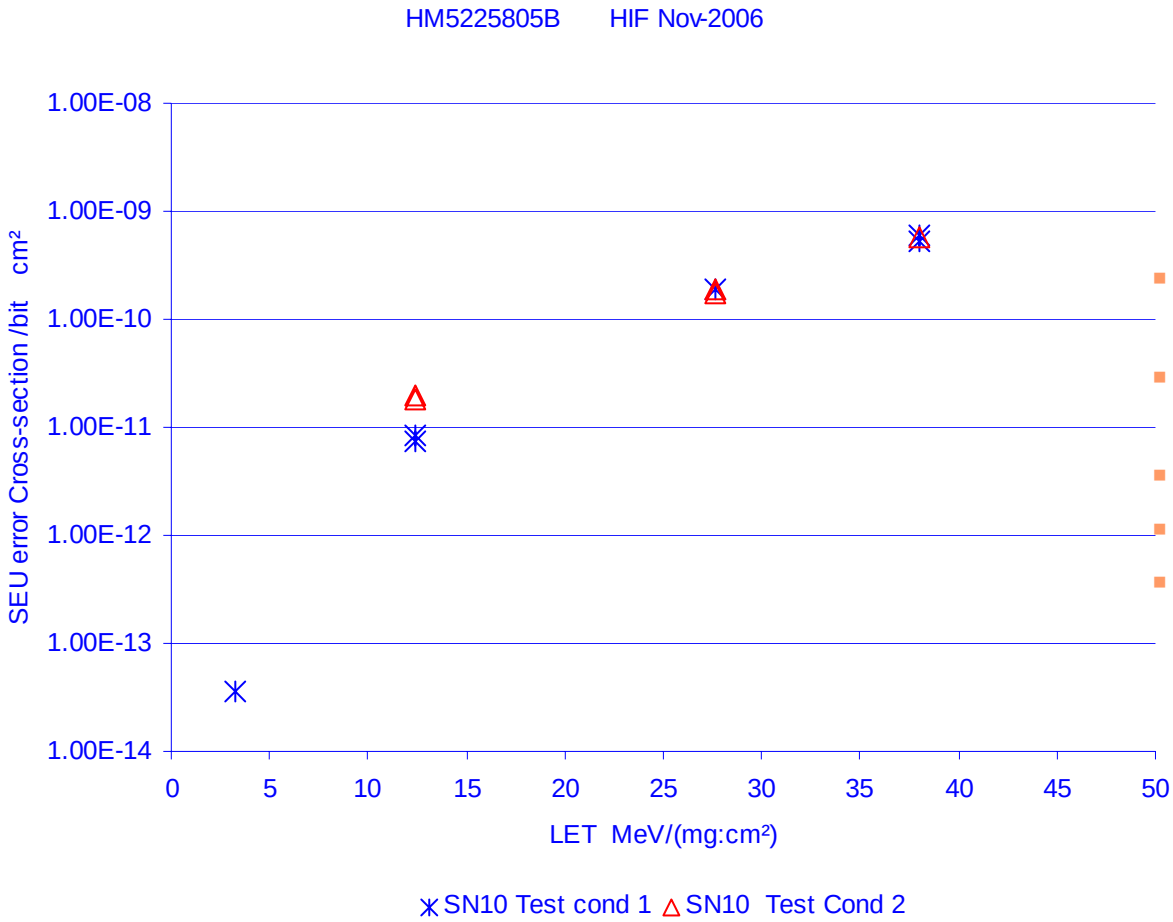
- Temperature (Up to 70°C)
- Static/dynamic test mode at 25MHz
- Refresh mode
- Refresh period
- Test pattern

Samsung K4S5120832B SDRAM heavy ions results



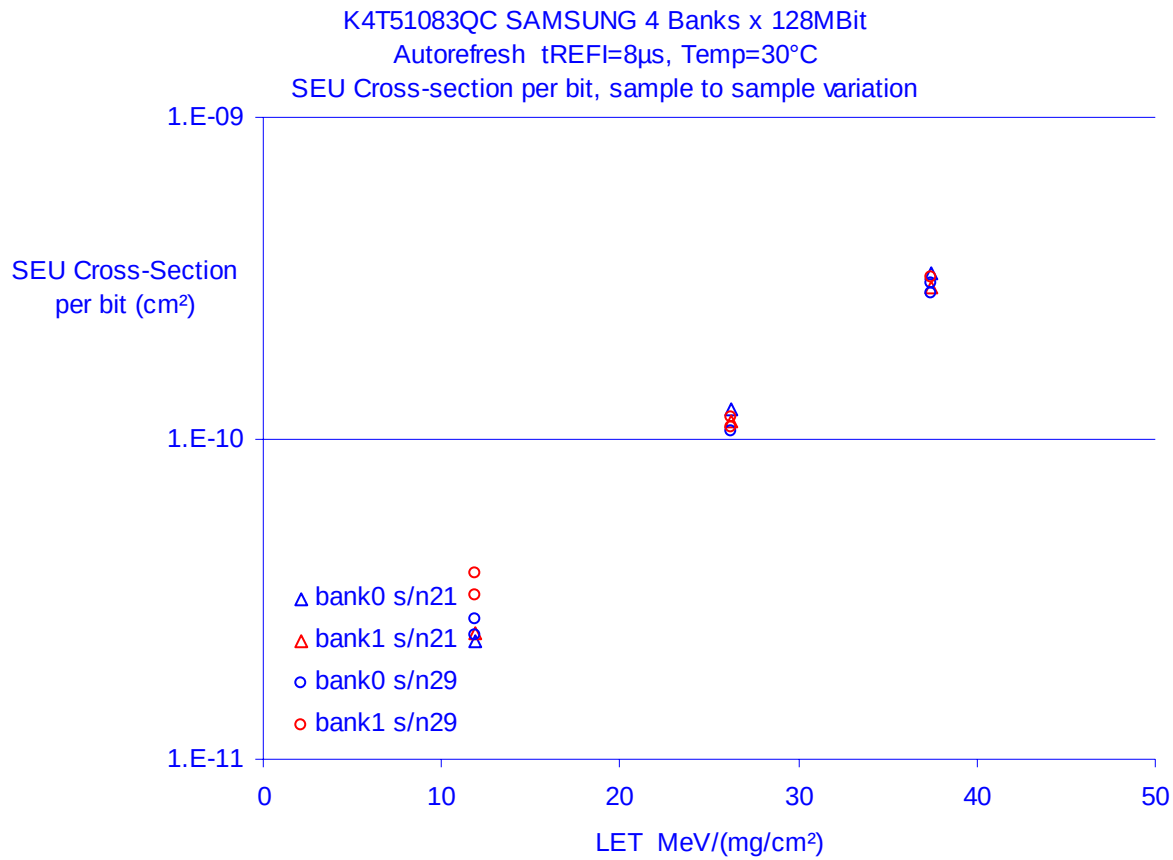
- No SEL event up to a LET of ~ 39 MeV/(mg/cm²)
- SEU error cross-section / bit ~ 3.5 E-10 cm²
- ROW errors and « hard » SEFIs
- No significative influence of variations of :
  - Temperature (Up to 70°C)
  - Static/dynamic test mode at 25MHz
  - Refresh mode
  - Refresh period
  - Test pattern

Hitachi/Elpida HM5225805BTT SDRAM heavy ions results



- No SEL event up to a LET of ~40 MeV/(mg/cm²)
- SEU error cross-section / bit ~ 6 E-10 cm²
- ROW errors
- Stuck Bits occurrences
- No significative influence of variations of :
  - Temperature (Up to 70°C)
  - Static/dynamic test mode at 25MHz

Samsung K4T51083QC DDR2 heavy ions results



- No SEL event up to a LET of ~37.5 MeV/(mg/cm²)
- SEU error cross-section / bit ~3 E-10 cm²
- ROW errors and « hard » SEFIs
- No significative influence of variations of :
  - Temperature (up to 85°C)
  - Auto Refresh period
  - Refresh mode
  - Static/dynamic test mode at 166 MHz

Infineon HYB18T512800AF DDR2 heavy ions results

- No SEL event up to a LET of ~37.5 MeV/(mg/cm²)
- Very low SEU error cross-section per bit in the range of ~5 E -14 cm²
- High proportion of MBUs compared to SEUs

⇒ Very likely, presence of an internal EDAC (Error Detection And Correction)

- COLUMN Errors as well as « hard » SEFIs

Samsung K4T51083QC DDR2 neutrons results

- Test at Los Alamos, Neutron white spectrum
- SER < 4 FIT/Mbit
- Occurrence of stuck bits (secondary beam effects ?)
- Dynamic Read (First Read) errors (might be related to stuck bits?). Operating frequency of 200 MHz (data rate 400 Mb/s)
- ROW errors and « hard » SEFIs

Infineon HYB18T512800AF DDR2 neutrons results

- Test at Los Alamos, Neutron white spectrum
- No Single Bit Upset
- No Stuck bit
- Assumed that an internal EDAC is implemented on this device
- Hard SEFI and COLUMN errors

Conclusion

- Achievements
  - About Test setup for DDR2 and further synchronous DRAMs
    - dynamic operation up to 200 MHz
    - SEFI processing
  - About analysis process
    - Descrambling
    - Thickness measurement
    - ⇒ comutation of SEU cross section per bit
  - About tests results
    - No significant influence of parameters variations
    - Good behavior of DDR2 → DDR not evaluated
- Next
  - Evaluate quantitatively SEFIs occurrence over LET range
  - Test with Xenon at RADEF, JYFL
  - More radiation types (proton, TID...)
  - Other families (Micron...)