CENTRE NATIONAL D'ÉTUDES SPATIALES

Compendium of 2006 radiation evaluation on commercial memory

CNES – January 24th 2007

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Agenda

- How to deal with SDRAM obsolescence :
  - SEE test results on two monolithic 512Mb SDRAM.
  - Overview of DDR-SDRAM project.
- Overview of NVRAM radiation study.
- Short description of new integrated SEE tester for memory.

How to deal with SDRAM obsolescence ?

- SDRAM market share is on decline (slower than foreseen nevertheless).
- Monolithic 1Gb SDRAM will never exist at all.
- Only few major manufacturer are still involved in SDRAM :
  - Elpida (ex-Hitachi)
  - Samsung (but not any new introduction since 2004)
  - Qimonda (ex-Infineon)
  - Micron
- Natural alternative is to follow computer market through using DDR-SDRAM memory. But this is not so obvious :
  - SDR-SDRAM and DDR-SDRAM aren't compatible in term of electrical interface, package, frequency.
  - DDR-II will replace DDR-I in near future.

SEE test results on two monolithic 512Mb SDRAM (1/4)

- Tested Devices :

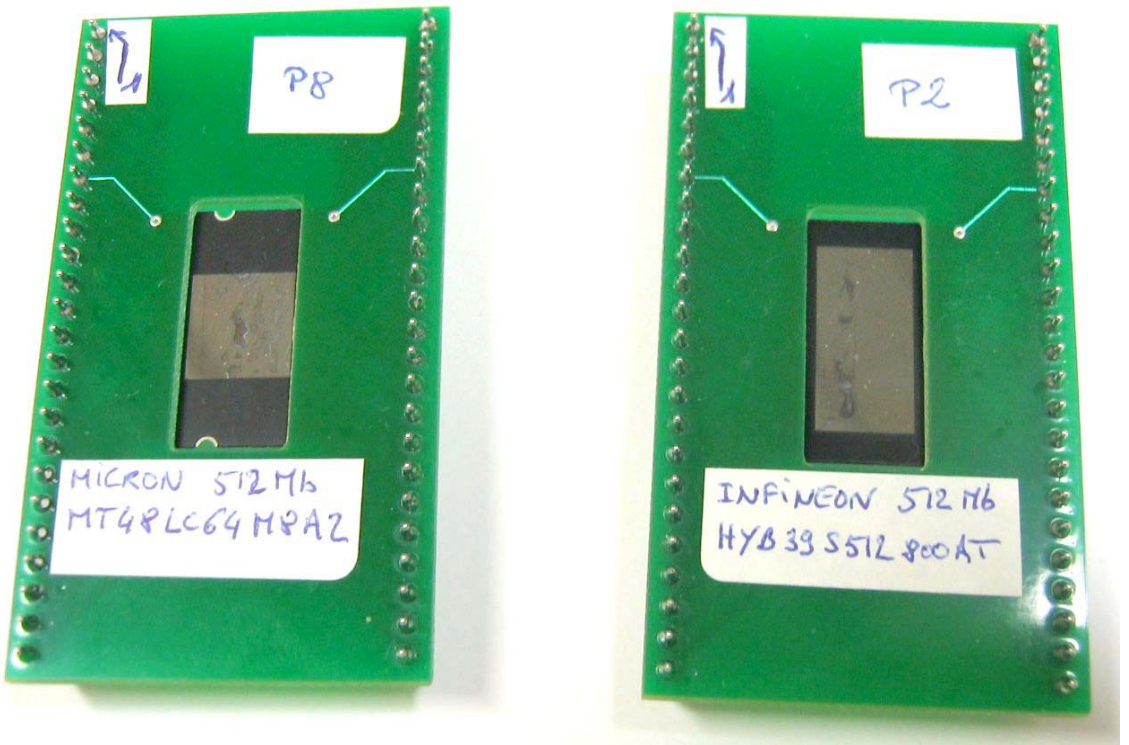
Manufacturer	Type	Features	package
MICRON	MT48LC64M8A2 TG-75	512Mb, 64M x 8bits, 3.3V	TSOP-54
INFINEON	HYB 39S512800AT-7.5	512Mb, 64M x 8bits, 3.3V	TSOP-54

- Cocktail used (**GANIL W47-2006 / UCL W26-2006**):

Ion	Energy (MeV)	Range (µm Si)	LET MeV(mg/cm²)
$^{108}Pb^{56+}$	1624	258	72.6
$^{83}Kr^{25+}$	756	92	32.4
$^{58}Ni^{18+}$	567	98	20.6
$^{40}Ar^{12+}$	372	119	10.1
$^{22}Ne^{7+}$	235	199	3.3
$^{13}C^{4+}$	131	266	1.2

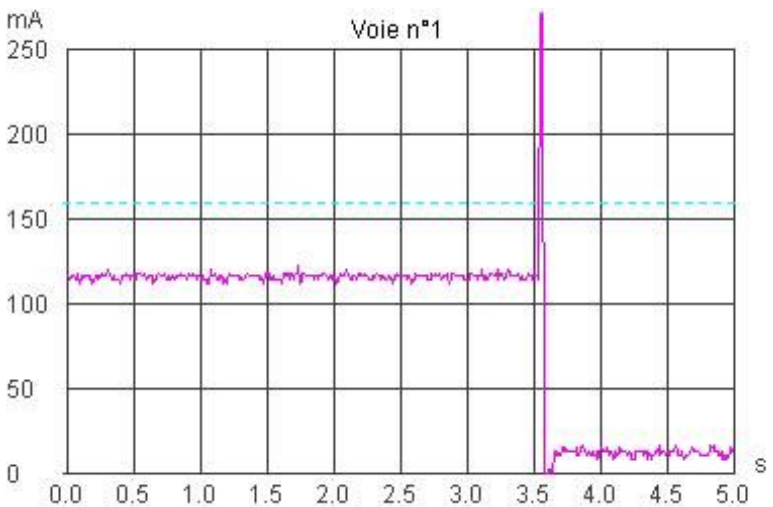
SEE test results on two monolithic 512Mb SDRAM (2/4)

- Samples are irradiated backside, thinned down to 60/80µm.
- Sensitivity to SEU,MBU, SHE,SEFI and SEL have been assessed

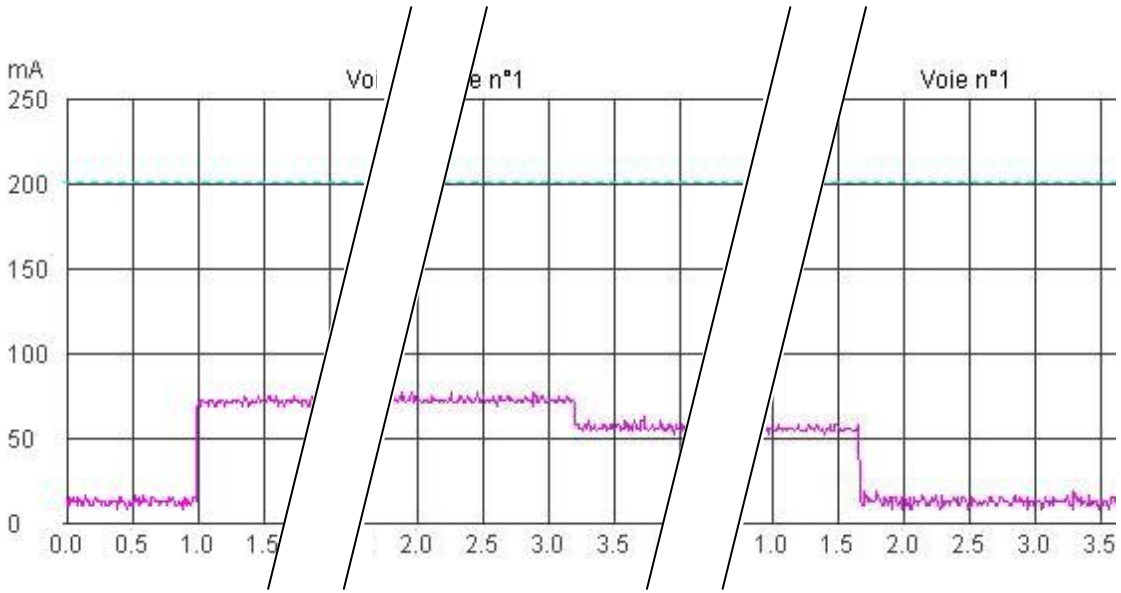


SEE test results on two monolithic 512Mb SDRAM (2/4)

- **Micron MT48LC64M8A2TG** :
  - No SEFI detected at all.
  - No SEL at LET 32,5 for 1.10^7p/cm² / 4 SEL at LET 72,4 for $2,7.10^6$p/cm²
  - Some current increase, probably µSEL and/or bus conflict.



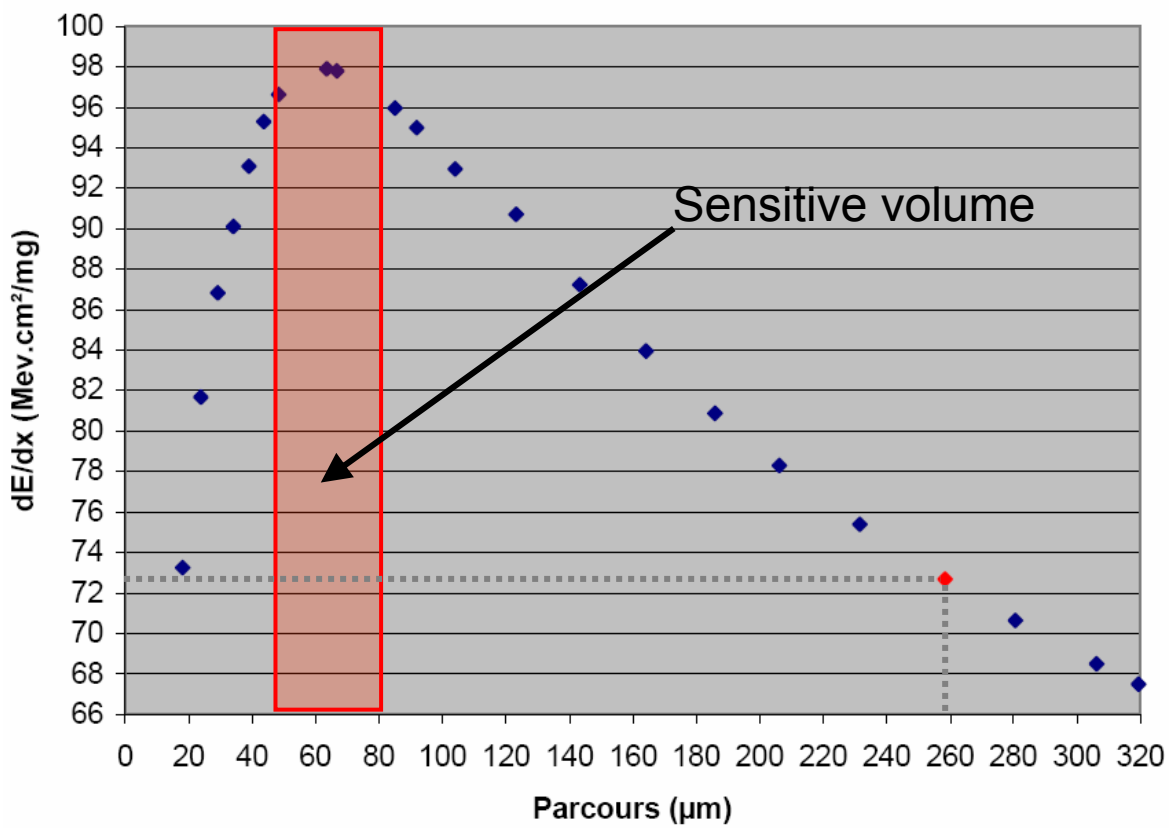
True SEL



Current variation during static tests

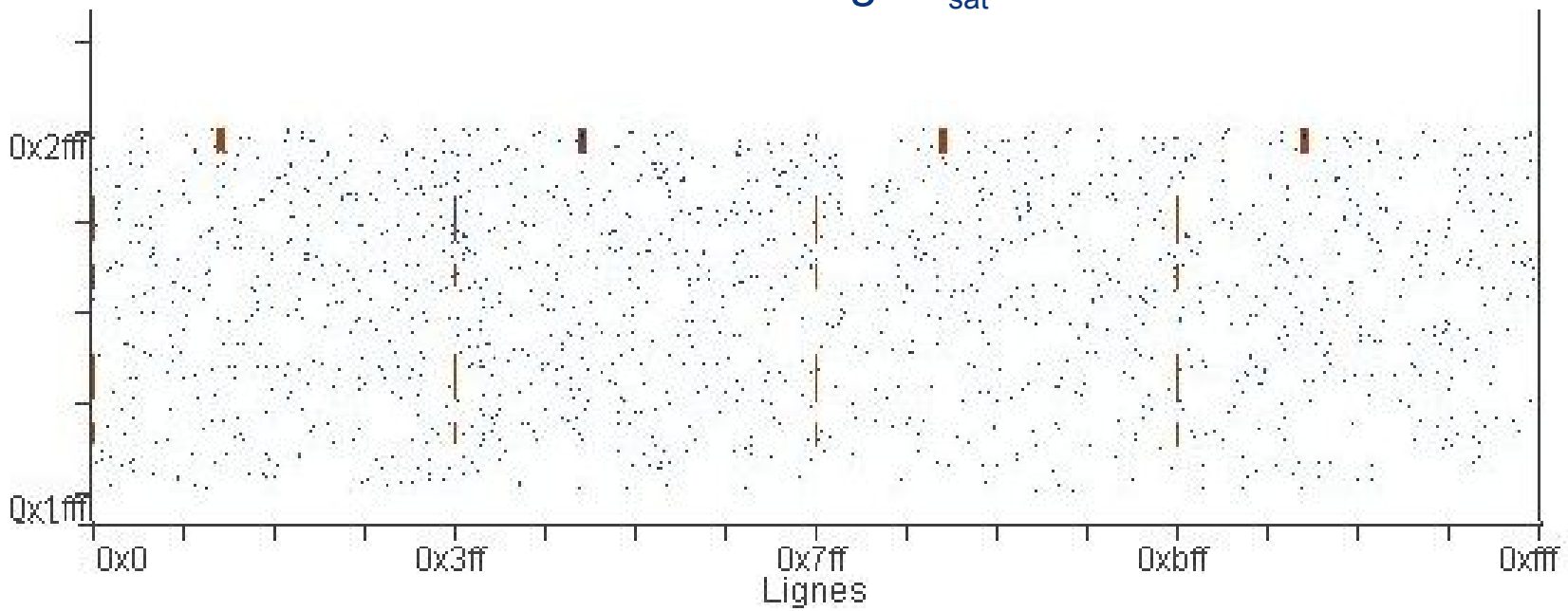
Digression : LET value of Ganil ion beam

- The beam characteristics reported here for the Ganil test is LET = 72,4MeV(mg/cm²) ; Range = 258µm. But in reality, considering the dE/dx curve, LET value in sensitive volume is around 97MeV(mg/cm²) !



SEE test results on two monolithic 512Mb SDRAM (3/4)

- **Micron MT48LC64M8A2TG** (cont.) :
  - High sensitivity to SEU LETth ≈ 3,3 / $Sigma_{sat}$ ≈ $10^{-9}cm^2$/bit
  - Some SHE detected by the tester but always in clusters and it disappear immediately after init (without power cycling) => suspected cause is SEU in periphery.
  - Sensitive to MBU : hard to determine $Sigma_{sat}$ due to cluster of errors.



SEE test results on two monolithic 512Mb SDRAM (4/4)

- **Infineon HYB39S512800AT** :
  - This device have revealed an relatively high sensitivity to Latch-Up :

    LETth ≈ 10MeV(mg/cm²). For 5.10^6 p/cm² ; LET 20,6 => 19 SEL
  - Event rate in orbit will be not so high but this device cannot be used without SEL mitigation. For a solid state recorder (1000's of devices) this is unacceptable.
  - And, if you are not convinced :
    - This part is also sensitive to SEFI with LETth ≈ 10MeV(mg/cm²)
    - Infineon no longer involved in SDRAM, new name is Qimonda...

Is DDR-SDRAM the solution for the futur ?

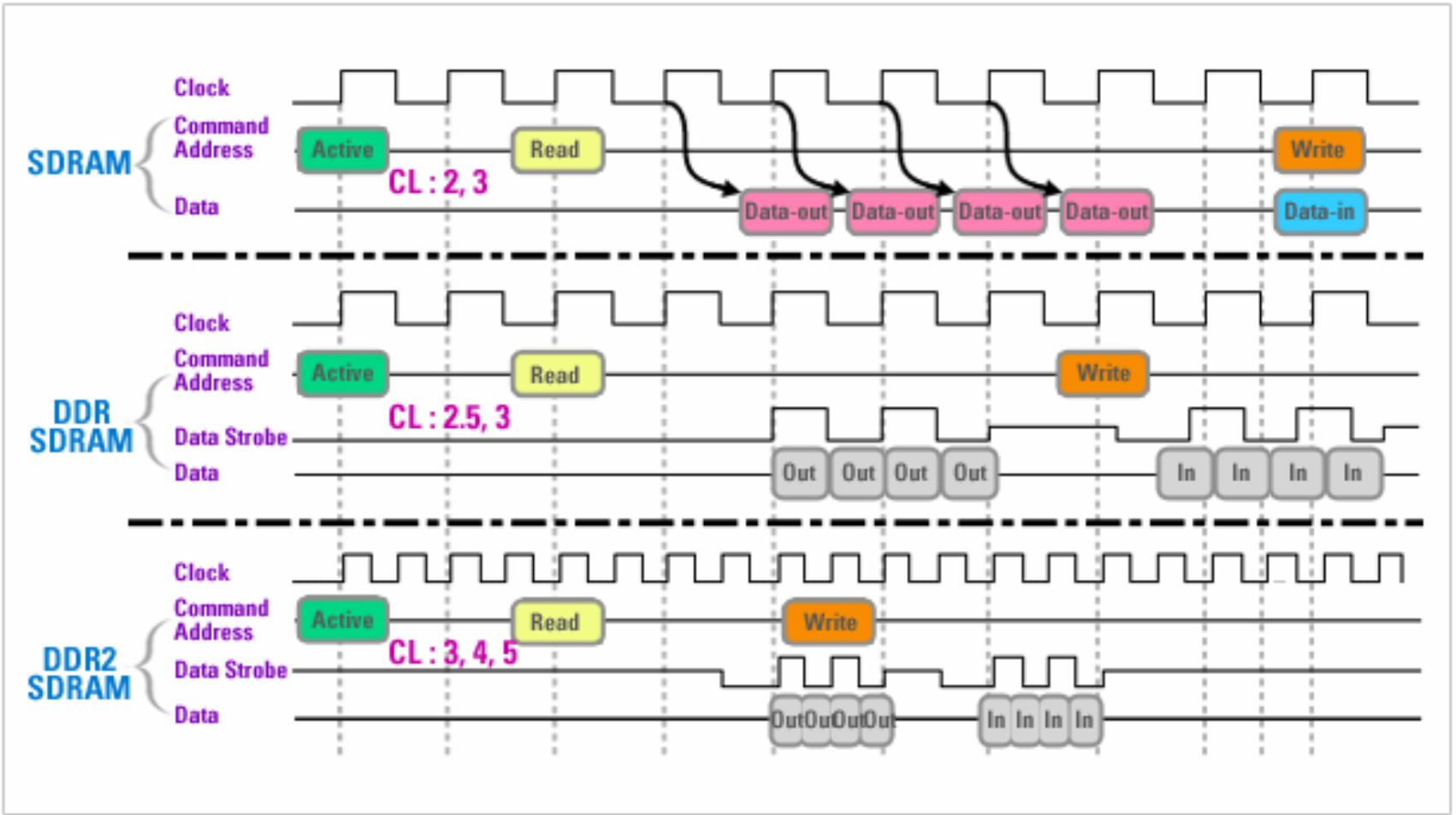
- **First we have to compare key feature of DDR-SDRAM and SDR-SDRAM**

Key Feature

	SDRAM	DDR	DDR2
Vdd/Vddq	3.3V	2.5V	1.8V
Package	54 TSOP-II	66 TSOP-II 60 BGA	60/84 BGA
Bit Org.	x4, x8, x16		
Clock Freq	~167 Mhz	100~200 Mhz	200~400 Mhz
Data rate	~167 Mtps	200~400 Mtps	400~800 Mtps
Interface	LVTTL	SSTL_2	SSTL_18
Prefetch	N/A	2	4
Burst Length	1, 2, 4, 8, F/P	2, 4, 8	4, 8
Strobe	No	Yes	Yes
Minimum clock Freq	No	~77MHz	~125MHz

Timing comparison SDR / DDR / DDR2

Timing Diagram



DDR-SDRAM Project

Based on French coordination in the frame of Multi-partnership it is assumed that we **have to** characterize DDR. But :

- In the time being, DRAM's are no longer the nominal way to build SSR. Flash NAND are considered.
- In a first time, DDR2 are not considered because of higher min clock frequency and only available package is FBGA => the step is to high !

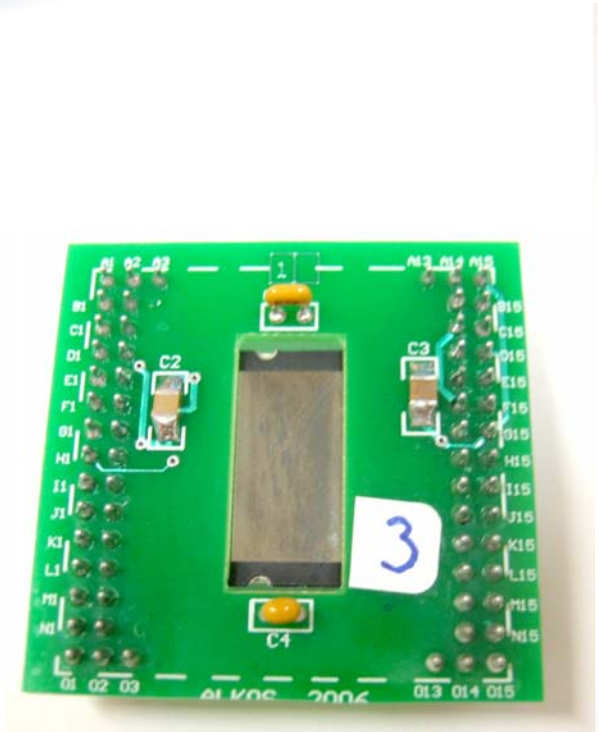
After Market Study selected devices are :

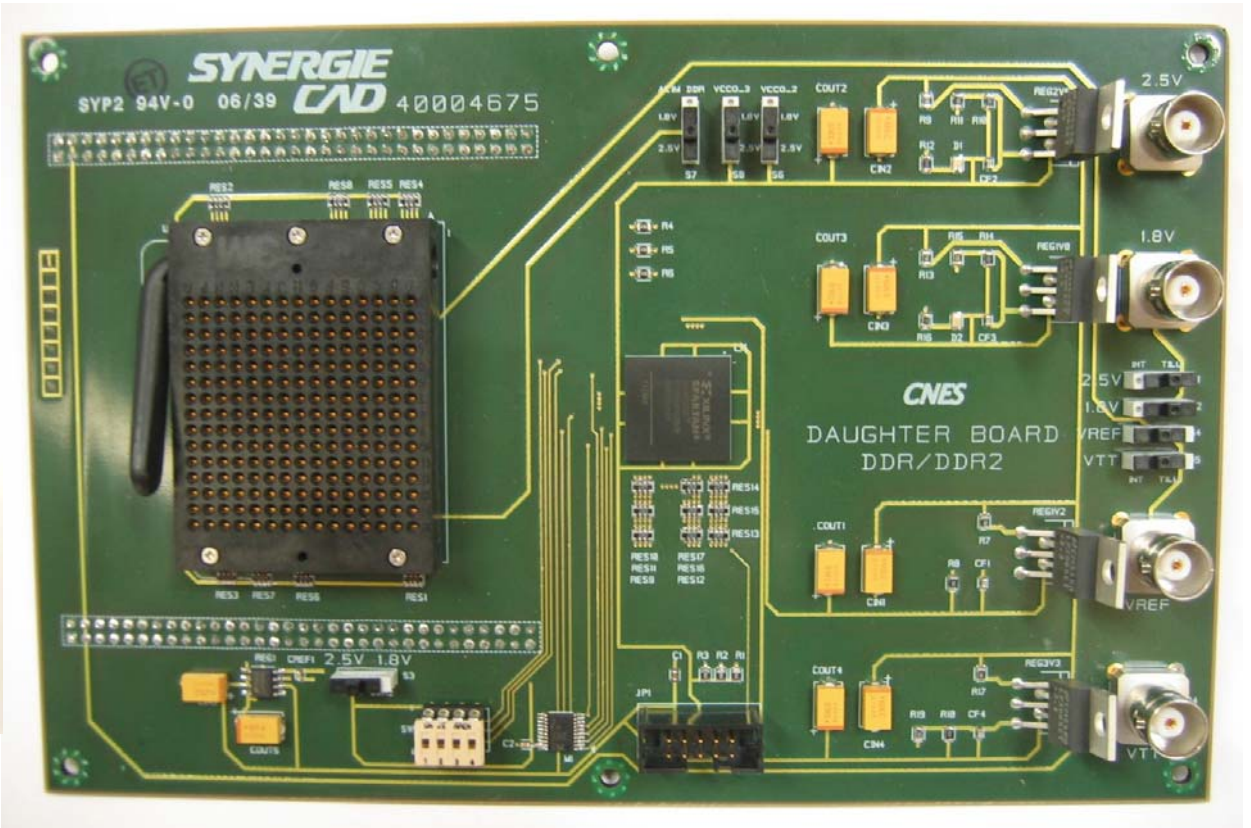
- Samsung K4H1G0838M : Purchase problem because minimum buy is 1000# and unit price ~200€ => cancelled !!!
- Micron MT46V128M8 : A trainee make the adaptation of interface between the device and the memory tester (TIMES).

Daughter Board for DDR testing with the TIMES

- Very complex board due to :
  - TIMES deliver only LVTTL, DDR interface is SSTL2 => we must use a Xilinx Spartan 3 FPGA as level shifter !
  - Test have to be performed at more than 77MHz when Tester have only 48MHz clock => Spartan 3 'DCM' allow to multiply clock in order to reach 96MHz.
  - DDR require routing with adapted impedance => 64x 22Ω matching resistor !
  - DDR require accurate voltage reference for V_{ref} and V_{TT} (1,25V +/- 0,015V) => use of dedicated component 'DDR Termination' (LP2996 from NS)
  - On the other hand, this 'super' daughter board will be able to test DDR2 without any hardware modification, just VHDL and a few switches to change.

Daughter Board for DDR testing with the TIMES





- In the time being, the daughter board has not been debugged due to trainee lack of time.

DDR-SDRAM Project : Phase 2

- By 2007, if budget is available, it is planned to make a new DDR stack in a 3D-Plus package (Hybrid assembly qualified by ESA and CNES). The main objective are :
  - 4 to 8 devices stacked, 1Gb DDR1 in TSOP66 and FBGA.
  - Electrical and thermal characterization of elementary devices outside manufacturer specification (mil. temp. ; lower clock frequency)
  - Radiation complement if necessary.
  - Stack manufacturing and electro-thermal characterization of the stack.
  - Feasibility study for ‘added value’ into the cube in order to be more ‘user friendly’. For example : level shifter LVTTL⇔SSTL2 ; load resistors ; voltage reference.

Overview of NVRAM radiation study (1/3)

Study performed by ONERA-DESP (T. NUNS) under CNES contract.

Objective is to investigate radiation (TID and SEE) behavior of Non-Volatile RAM in order to find the more promising one's.

First, a market study have been conduce. Almost all the major memory manufacturer have an NVRAM project. But only a few of them have a credible offer in term of maturity.

Technology	Manufacturer	Targeted capacity
Magnetorestive (MRAM)	Freescale, NEC/Toshiba, Cypress, Infineon, IBM	4Mb ➔ 16Mb
Ferro-electric (FRAM)	Ramtron, Toshiba, Matsushita, Fujitsu	1Mb ➔ 64Mb
Chalcogenide (OUM)	Ovonyx, BAE System, Samsung, ST Micro.	4Mb ➔ 512Mb
Nanotubes	Nantero	10Gb

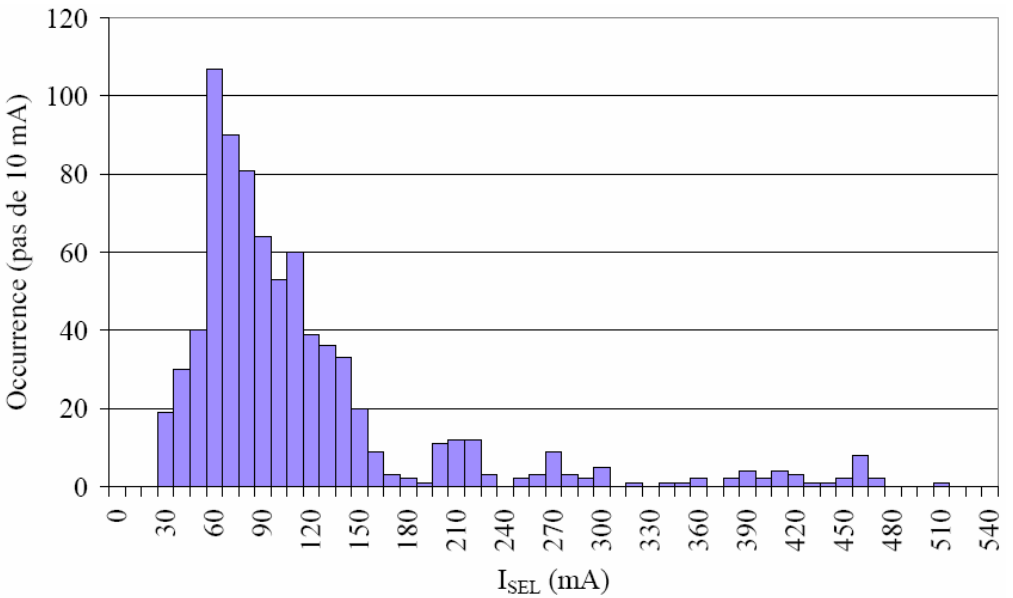
Overview of NVRAM radiation study (2/3)

- **Two technology have been selected : MRAM from Freescale and FRAM from Ramtron.**
- Ramtron - 1Mb FRAM - FM20L08 :
  - SEL LETth ≈ 23MeV(mg/cm²) ; $Sigma_{sat}$ ≈ 8E-4cm²/dev. (true SEL only)
  - Memory array is immune to SEU when device is OFF. Very few errors at LET>45 when device is irradiated in static mode. This sensitivity is probably due to SEU in periphery who activate the erase mechanism.
  - Irradiation in Dynamic mode show SEU LETth ≈ 6MeV(mg/cm²) ; $Sigma_{sat}$ ≈ 1.5E-3cm²/dev.
  - MBU are very often in cluster, it confirm that most of the sensitivity come from periphery.
  - TID performance : > 31kRad(Si) for device ON ; all devices remain functional after annealing (24h@25°C+168h@100°C) ; No failure at 35kRad(Si) when devices are OFF.

Overview of NVRAM radiation study (3/3)

- MRAM 4Mb Freescale MR2A16A :
  - SEL LET_{th} ≈ 5MeV(mg/cm²)
    Sigmasat ≈ 1E-3cm²/dev.
  - True SEL and cumulative μSEL have been detected

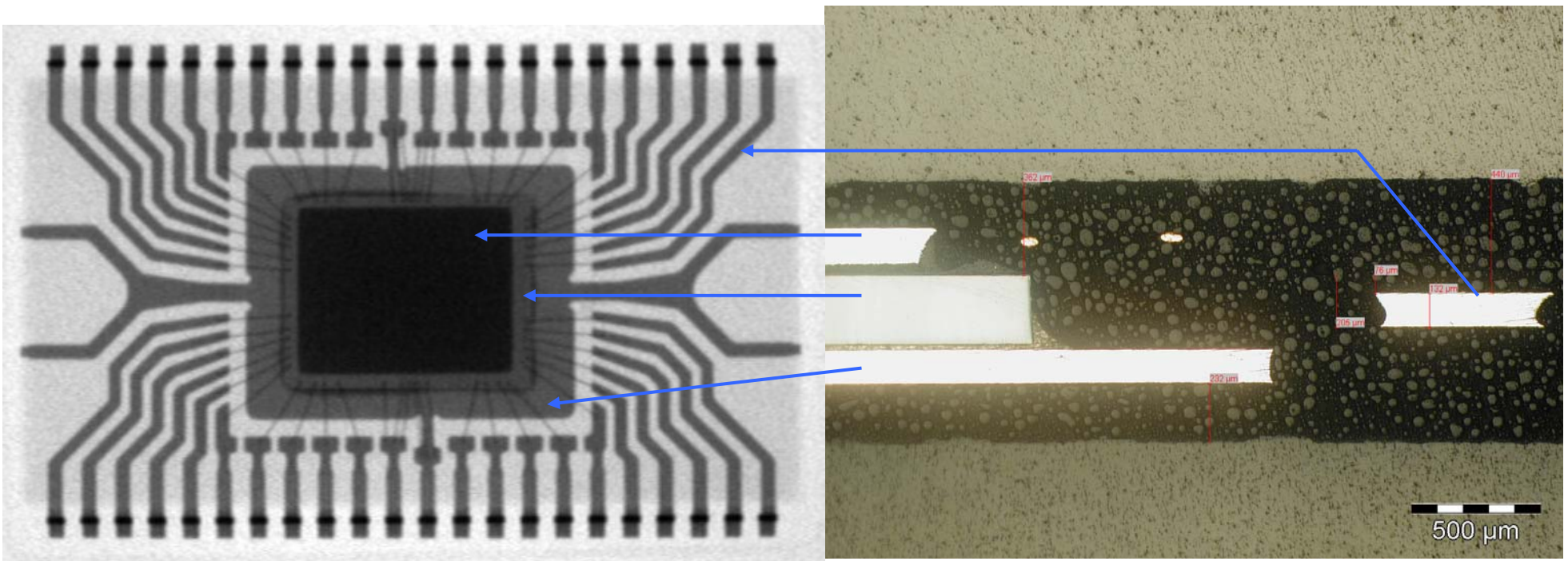
Histogram of SEL Amplitude :



  - Memory array is immune to SEU when device is static.
  - Tests in dynamic mode have been perturbed by SEL. This is probably due to bad synchronisation between SEU tester (TIMES) and SEL tester (TILU)
  - TID performance : > 52kRad(Si) for device ON ; all devices remain functional after annealing (24h@25°C+168h@100°C) ; No failure at 110kRad(Si) when devices are OFF.

Problematic sample preparation of Freescale device

- Die is covered by a metallic protection (Magnetic shielding?) :
  - Chemical etching is impossible. Thinning cannot be performed by ‘sander’ because pins are coplanar with die.
  - It require machine tool in order to drill base-plate and thin only the die. This method have a lower yield (2 fail on 6 devices thinned)



The new integrated SEE tester for memory : TIMES.

- **Key features of the TIMES (Testeur Intégré de Mémoire en Evènements Singuliers) :**
  - Fully autonomous in term of test algorithm and error recognition (SEU, MBU, SHE).
  - Synchronisation with TILU for Latch-up detection.
  - Internal capacity of 300 000 error vectors (time / type / address / mask).
  - 100 programmable LVTTL I/O (Xilinx Spartan 2)
  - Remote controlled by GUI on PC. (Ethernet 10Mb/s).
  - GUI provide real time cartography of error.

The new integrated SEE tester for memory : TIMES.