Further Heavy Ion and Proton SEE Evaluation of High Capacity NAND-FLASH Memory Devices for Safeguard Data Recorder

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Introduction

ESA Study: SafeGuard Data Recorder (SGDR)

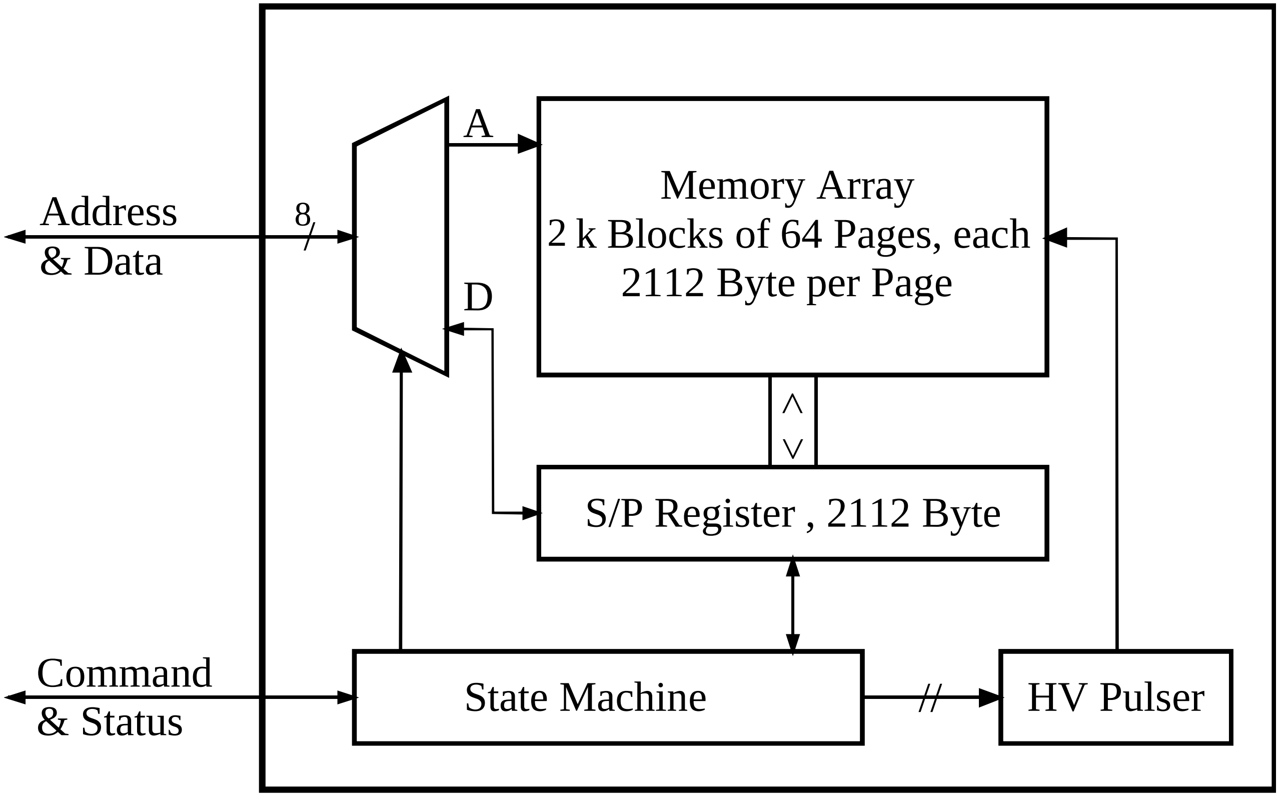
Requirements:
(a) Nonvolatility
(b) Highest Integrity of stored data after 10 years
(c) ....

Selected Technology: NAND-Flash Memory Devices

Storage Cell: Dual Gate MOS Transistor
Data represented by electron charge on Floating Gate

Electron Transport: Channel $\leftrightarrow$ Floating Gate by Fowler-Nordheim Tunneling

Principal Organization of 2 Gbit NAND Flash Devices



Basic FLASH Memory Operations

Write: Pagewise
Serial Byte Transfer User $\rightarrow$ 2112 Byte Data Register DR,
Parallel Programming of "0"s by pulsed electron tunneling,
Page Write Time: 2112 Byte · 30 ns/Byte + 700 µs ≈ 800 µs

Read: Pagewise
Status of 2112 · 8 selected Transistors $\rightarrow$ DR,
Serial Byte Transfer DR $\rightarrow$ User,
Page Read Time: 2112 Byte · 30 ns/Byte + 25 µs ≈ 100 µs

Erase: Blockwise $\rightarrow$ "1"
Parallel Decharging of 2112 · 8 · 64 Storage Cells
by pulsed electron tunneling,
Block Erase Time: ≈ 3 ms

Complexity of Flash Memory Operations

Device internal voltage generator delivers "high voltage" of 20 V to achieve sufficient electrical field strength across the thin oxide between channel and floating gate for write / erase tunneling.

Flash operation requires many clock cycles and command executions like the operation of internal state machines, data and command registers, high voltage generators, a.s.o.

⇒ Numerous potential error types besides the corruption of the content of storage cells.

⇒ Classification of observed errors

Classification of Distributed Data Errors

Class A Errors $\Rightarrow$ σ_A

Distributed Data Errors

- **Static Errors = Memory Cell Errors** $\Rightarrow$ σ_{Static}
  Error reproduced by subsequent read out

- **Dynamic Errors = Register Upsets** $\Rightarrow$ σ_{Dyn}
  Error disappears at subsequent read out

  - **Random SEUs** $\Rightarrow$ $\sigma_{Dyn,\ SEU}$

  - **Cluster Events, CLEs** $\Rightarrow$ **Events:** σ_{CLE}**, Bytes:** σ_{CLB}
    Chain of erroneous, but not immediately adjacent Bytes,
    Typically "0" $\rightarrow$ "1" Errors at the same bit position,

    CLEs are prone to impair error correction,
    calling for code interleaving

Classification of SEFIs

Class B Errors, caused by $\Rightarrow$ σ_B

Transient SEFIs

- **Page Errors, PEs**
- **Vertical Errors, VEs**
  Subsequent pages are spoiled at the same byte and bit position
- **Block Errors, BEs**
  most likely caused by failed erase

Class C Errors, caused by $\Rightarrow$ σ_C

Persistent SEFIs, resolvable by reset command or power cycling

- Accompanied by current surge (e.g. SELs), supports detection
- Not accompanied by current surge

Class D Errors, caused by

Destructive Device Failures, **DFs**

Example Test Modes

- Write Background pattern to each block
- While exposure perform for every block:
  - Verify background of the block
- Continue

Read Mode M2

- Write Background pattern to each block
- Expose the device
- Verify background of every block

Storage Mode M3

- Write Background pattern to **each** block
- While exposure perform for **every** block:
  - Verify background of the block **(R_1)**
  - PC
  - Verify background of the block **(R_2)**
  - Erase Block **(E)**
  - PC
  - Perform for each page of the block:
    - Verify the erased page **(r)**
    - Programm the page with the inverse background **(W)**
    - Verify the inverse background of the page **(r)**
- Continue with inverted background pattern

Marching Mode M5

Purpose of the Performed Heavy Ion Tests

Five Test campaigns:
3 Tests at HIF, UCL Louvain-la-Neuve, Belgium
2 Tests at RADEF, Jyväskylä, Finland

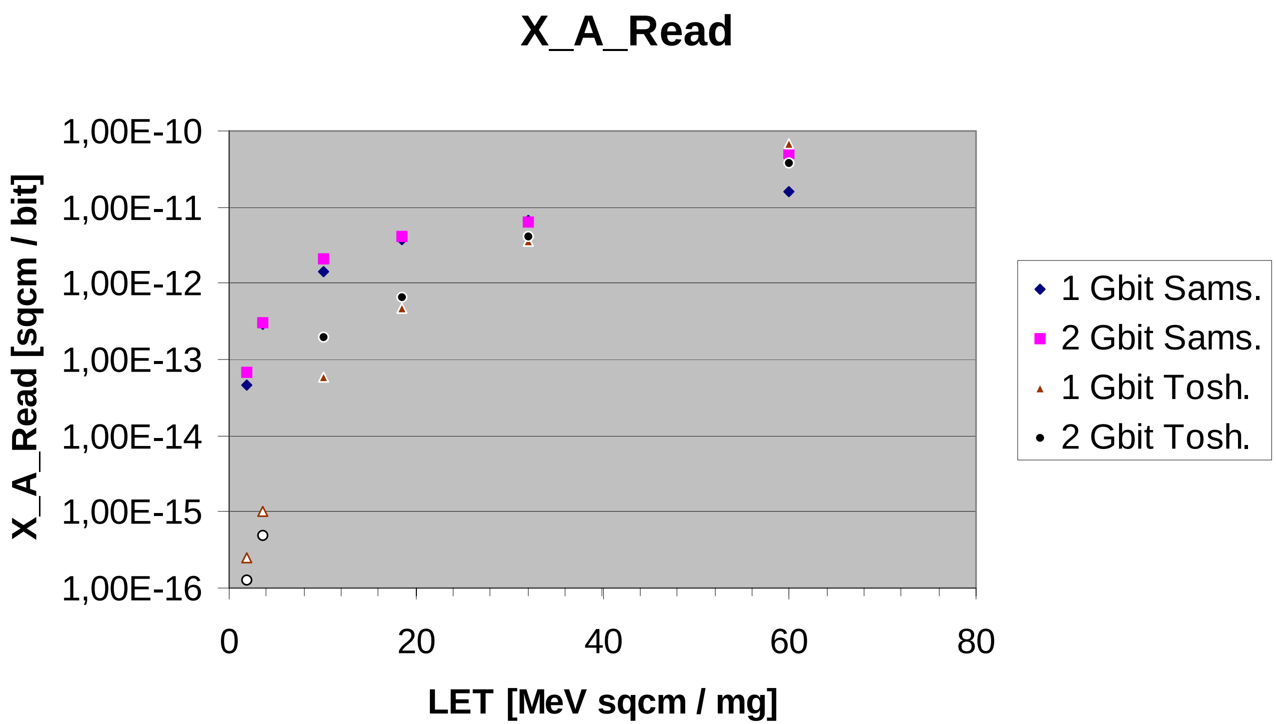
These tests were aimed

- to get an overview of the error types,
- to identify, to characterize and to describe the statistic properties of those error types, which endanger the SGDR data integrity,
- to validate the effectiveness of countermeasures

The outcome of these tests enforced two substantial refinements of the conceptual SGDR design:

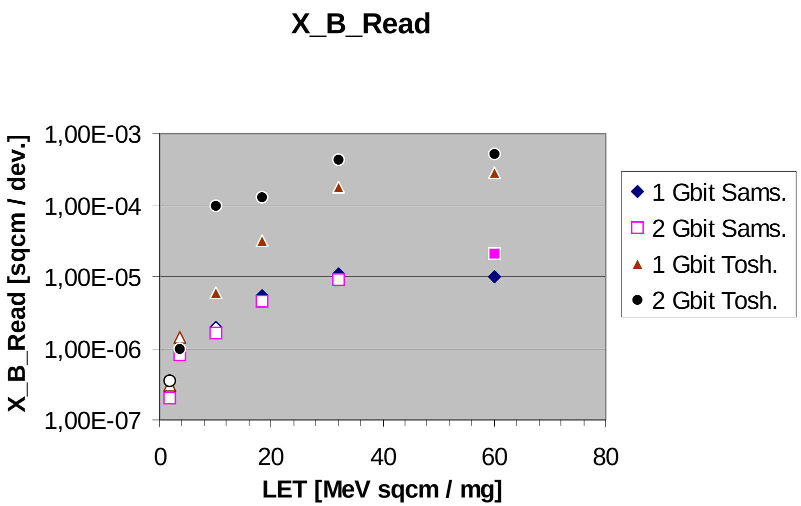
- Interleaving of the error correction code against clustered errors,
- Insertion of Power Cycles after each Block Erase

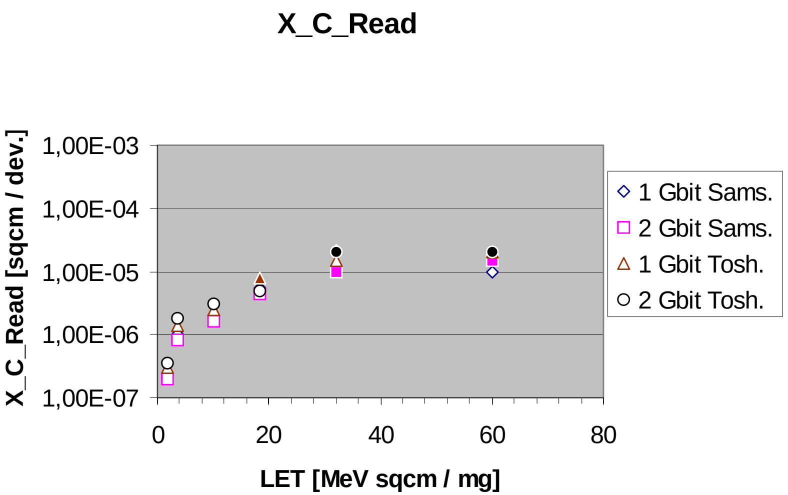
Single Byte Error Cross Sections σ_A, of 1 / 2 Gbit NAND Flash's



Open Symbols indicate: "No errors, σ less than"

Cross Sections σ_B and σ_C of 1 Gbit / 2 Gbit NAND Flash Devices in Read Mode





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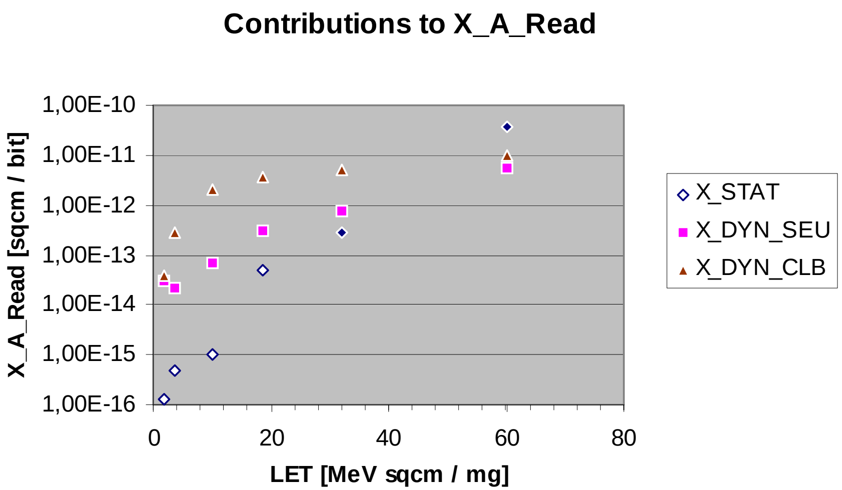
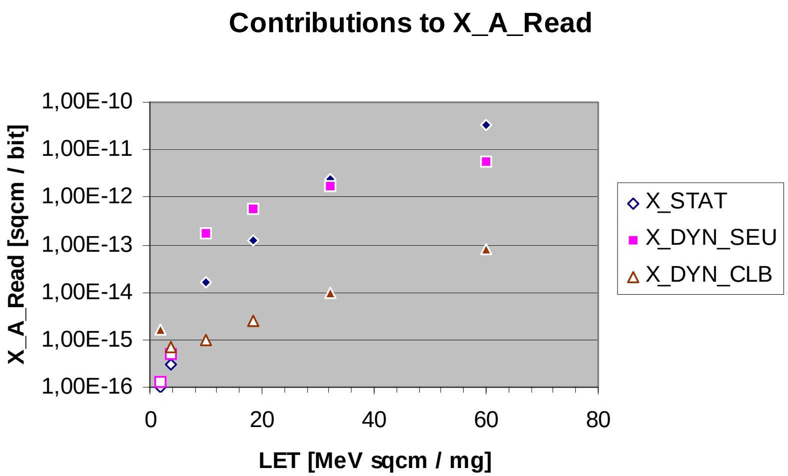
Transient SEFI Cross Sections $\sigma_{B, Read}$ of 1 Gbit / 2 Gbit NAND Flash's

Persistent SEFI Cross Sections $\sigma_{C, Read}$ of 1 GBit / 2 Gbit NAND Flash's

Cross Sections σ_{Stat}, $\sigma_{Dyn,SEU}$ and $\sigma_{Dyn,CLB}$ of 1 / 2 Gbit Nand Flash Devices





Open Symbols indicate: "No errors, σ less than"

2 Gbit Samsung,

Single Byte Error X-Sections σ_{Stat}, $\sigma_{Dyn,SEU}$ and $\sigma_{Dyn,CLB}$

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2 Gbit Toshiba,

Single Byte Error X-Sections σ_{Stat}, $\sigma_{Dyn,SEU}$ and $\sigma_{Dyn,CLB}$

Samsung: No Static Errors at LET < 20 MeV cm2 mg-1

Toshiba: Substantially smaller share of clustered error bytes.

All Static Errors and most Cluster Errors disturb "0" $\rightarrow$ "1"

Statistical Properties of Cluster Errors

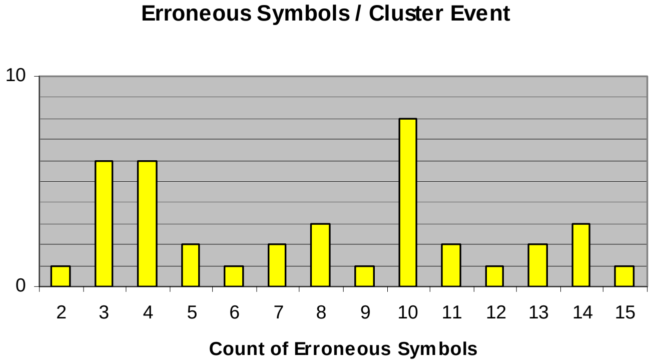


Fig. 1:
Spectrum of the Count of Erroneous Cluster Symbols,
LET= 10.1 MeV cm^{2} mg^{-1}

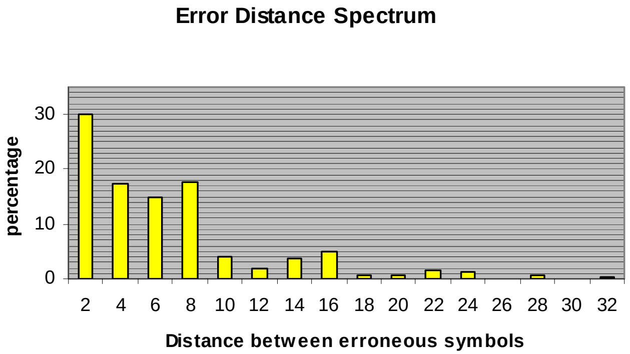


Fig. 2:
Spectrum of Distance between Erroneous Symbols

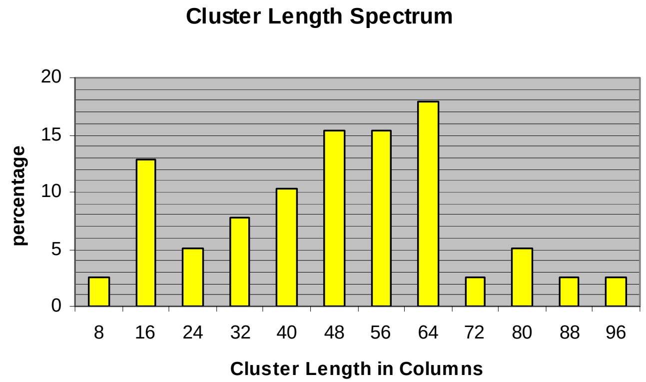
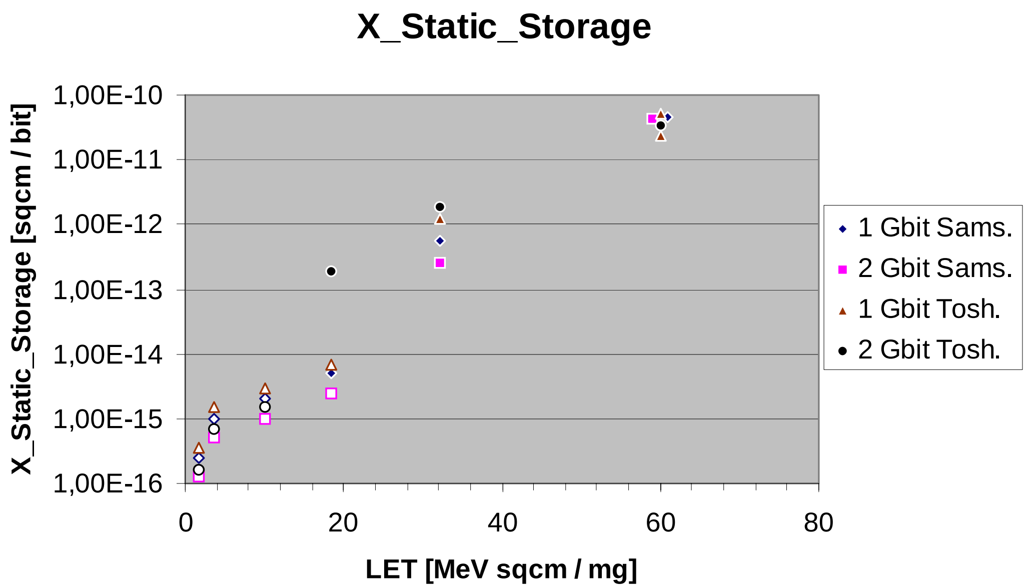


Fig.3: Spectrum of Cluster Length

Cross Sections σ_A, of 1 / 2 Gbit NAND Flash Devices in Storage Mode



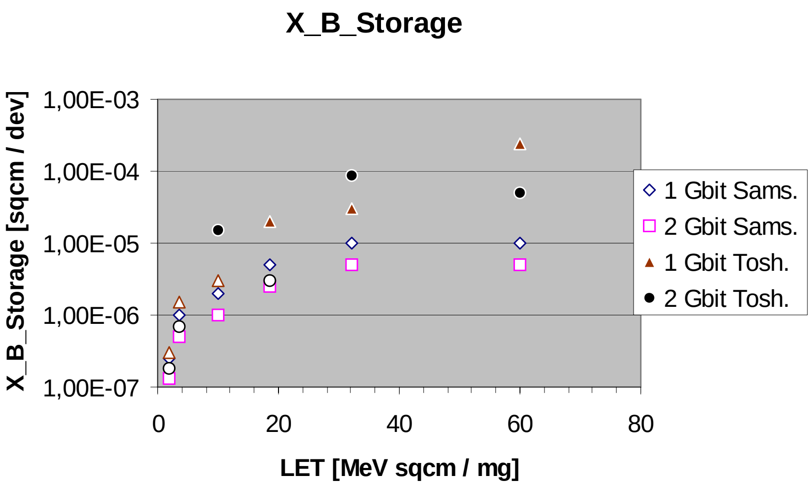
Single Byte Error Cross Sections σStatic of 1 Gbit / 2 Gbit NAND Flash's, RADEF Spring 06

Open Symbols indicate: "no errors, σ less than"

All Static Errors disturb "0"→ "1"

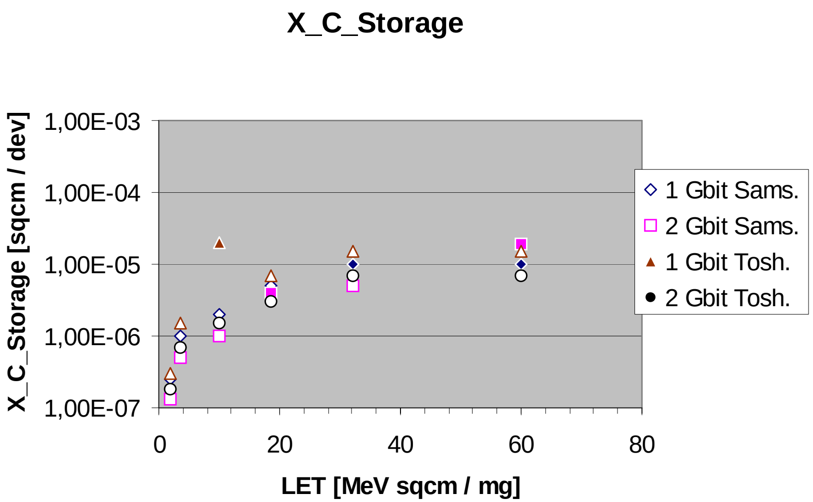
No Static Errors below LET ≈ 15 MeV cm^2 mg^{-1}, above steep increase

Cross Sections σ_B and σ_C of 1 / 2 Gbit NAND Flash Devices in Read Mode



Transient SEFI Cross Sections $\sigma_{B,Storage}$ of 1 Gbit / 2 Gbit NAND Flash's in Storage Mode RADEF Spring 06

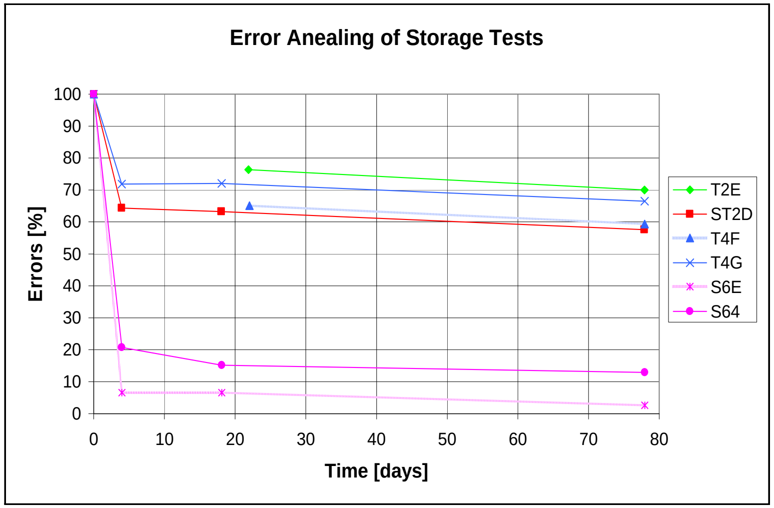
Open Symbols indicate: "no errors, σ less than"



Persistent SEFI Cross Sections $\sigma_{C,Storage}$ of 1 Gbit / 2 Gbit NAND Flash's in Storage Mode RADEF Spring 06

Open Symbols indicate: "no errors, σ less than"

Annealing of Static Errors



Annealing of Static Errors after Test in Storage Mode (erroneous "1" → correct "0")

Investigation of the Read Mode error files unveiled also annealing of Static Errors during the test run, typically ranging over six to seven complete read outs

Example: Total 96 Static Errors,
24 of them annealed already during the test run

Question: Do all Static Errors disappear with time?

60 MeV Proton Test

Only 60 MeV Protons available

3 x 1 Gbit Samsung, 3 x 1Gbit Toshiba, 3 x 2 Gbit Samsung, 3 x 2 Gbit Toshiba

Storage Mode, biased and unbiased:

- No Single Byte Errors
- One Page Error @ 2 GBIT Toshiba, biased

Marching Mode, combines:

(i) Erase under exposure
(ii) Write under exposure
(iii) Multiple Read under exposure

for rapid survey

60 MeV Proton Cross Sections in Marching Mode

Device	Fluence [cm^{-2}]	$\sigma_{Stat + SEU}$ [cm^2/bit]	σ_{CLB} [cm^2/bit]	σ_A [cm^2/bit]	σ_B [cm^2/dev]	σ_C [cm^2/dev]
Samsung 1 Gbit	**3.3 E+10**	**4.5 E-19**	**1.8 E-19**	**6.3 E-19**	*< 3.0 E-11*	*< 3.0 E-11*
	3.2 E+10	**5.2 E-19**	**3.3 E-19**	**9.0 E-19**	*< 3.1 E-11*	*< 3.1 E-11*
	2.9 E+10	**6.1 E-19**	**2.1 E-19**	**8.2 E-19**	*< 3.4 E-11*	*< 3.4 E-11*
Toshiba 1 Gbit	**2.9 E+10**	*< 3.4 E-20*	*< 3.0 E-20*	*< 3.0 E-20*	*< 3.0 E-11*	*< 3.0 E-11*
	2.8 E+10	*< 3.6 E-20*	*< 3.1 E-20*	*< 3.1 E-20*	*< 3.1 E-11*	*< 3.1 E-11*
	2.8 E+10	*< 3.6 E-20*	*< 3.4 E-20*	*< 3.4 E-20*	**3.4 E-11**	*< 3.4 E-11*
Samsung 2 Gbit	**3.6 E+10**	**4.1 E-19**	**3.2 E-19**	**7.3 E-19**	*< 2.8 E-11*	*< 2.8 E-11*
	4.1 E+10	**3.6 E-19**	**1.8 E-19**	**5.4 E-19**	*< 2.4 E-11*	*< 2.4 E-11*
	2.9 E+10	**9.5 E-20**	**2.0 E-19**	**3.0 E-19**	*< 3.4 E-11*	*< 3.4 E-11*
Toshiba 2 Gbit	**3.0 E+10**	**1.6 E-19**	< 2.4 E-20	**1.6 E-19**	**3.3 E-11**	*< 3.3 E-11*
	3.0 E+10	**1.6 E-19**	< 2.5 E-20	**1.6 E-19**	**3.3 E-11**	*< 3.3 E-11*
	3.1 E+10	**2.4 E-19**	< 1.6 E-20	**2.4 E-19**	**3.2 E-11**	*< 3.2 E-11*

Figures in italics: “No errors, less than”

Summary

- Previous heavy ion tests occasionally showed destructive device failures even at LETs < 20 MeV cm^2 mg^{-1} without accompanying current surge.
  After the insertion of a power cycle behind each block erase only one more destructive device failure occurred at LET = 60 MeV cm^2 mg^{-1}.

- Static and Dynamic Data Error Cross Sections and
  Transient and Persistent SEFI cross sections
  of 1 Gbit and 2 Gbit NAND Flash devices of two leading suppliers have been gained.

- Some device types showed significant error clustering under exposure to heavy ions, and also to protons. This property is prone to impair the efficiency of error correcting codes.
  Typically same single bit of several chained bytes is "0" $\rightarrow$ "1"falsified.
  Related cross sections and statistical cluster properties have been determined.

- Significant annealing of Static Errors (erroneous "1" $\rightarrow$ correct "0") has been observed.
  This questions the Static Error Cross Sections gained by the usual high flux exposure.
  Possibly all Static Errors disappear with time.

Acknowledgement

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