Practical Interpretation of LET Requirements

Saab Space

Stanley Mattsson

LLN, January 25th, 2007

SEE Requirements from Alcatel Alenia Space

- Pragmatic and "in principal" easy to comply to.

- Destructive SEE:
  - LET ≥ 60 MeV /cm2/mg & 10^7 ions/cm2: No Events Observed
    - ✓ LET ≥ 60 approximated with Xe ⇒ Frequently available beams, No tilting required
    - ✓ 10^7 ions/cm2: @ Xe ⇒ Usually no problem with use of high ion FLUX
      - ✓ 1000 - 3000 ions/sec ⇒ 3h – 1h beam time

- Non-Destructive SEE:
  - Ions & Energies shall be selected in order to make sure that
    - ✓ Saturated device cross section is obtained
    - ✓ Ion range greater than EPI layer thickness (valid for destructive & non-destructive)
      - ✓ Opens up for use of test data from IPN / Orsay or BNL / Brookhaven

- Heavy ion testing in accordance with ESA 25100 or JEDEC #57

ESA/SCC 25100

- Test & Bias Conditions ⇒ Shall be given by the test report
  - Alcatel Alenia Space: ⇒ Refers to ESA/SCC 25100
  - Astrium requirement: ⇒ "Typical conditions of use for application"

- Ion Range ⇒ Typically 30µm

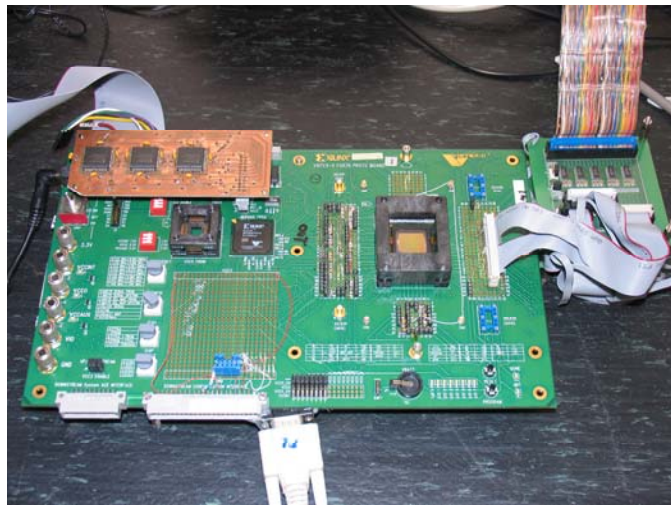
- Ion Flux ⇒ Meaningful number of upsets in 1 to 20 minutes
  - "No Dose Rate Effects in SEE testing"

- Max Fluence ⇒ 10^7 ions/cm2

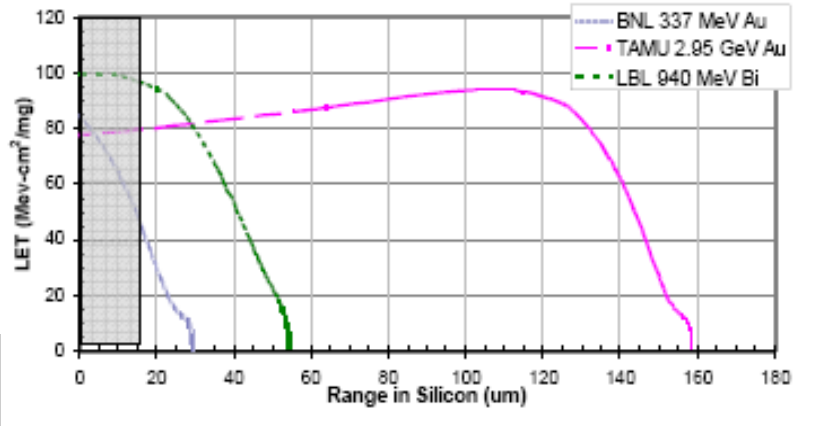
- 8 out of 13 of pages ⇒ How to write Documentations

SEL Requirements General Documents

- No Events Observed for LET > 70 – 110 MeV/mg/cm2
  - Tilt Needed for European Ion Beams
  - Tilt may be difficult due to shadowing by the socket

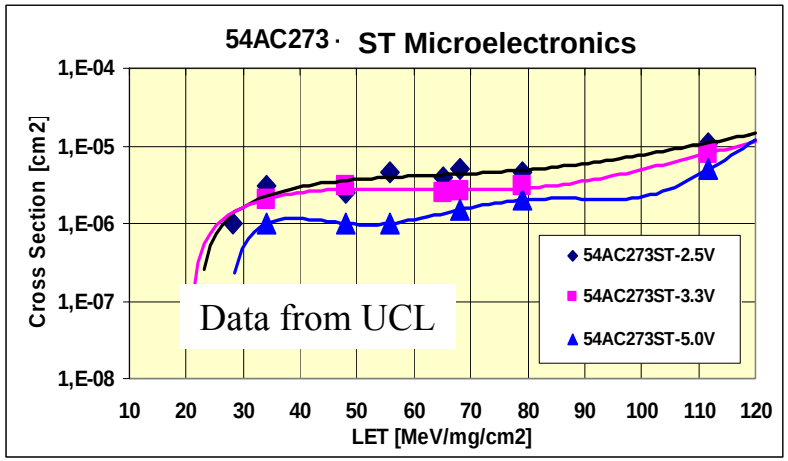


- Ion Range Requirement ⇒ 30µm
  - For Galileo, Au ions at BNL would be acceptable
    - ✓ ^{197}Au ; LET 80 Mev/mg/cm2, range in Si ~ 28µm
    - ✓ With 15 µm dead layer, equivalent LET ≈ 40 MeV/mg/cm2 available

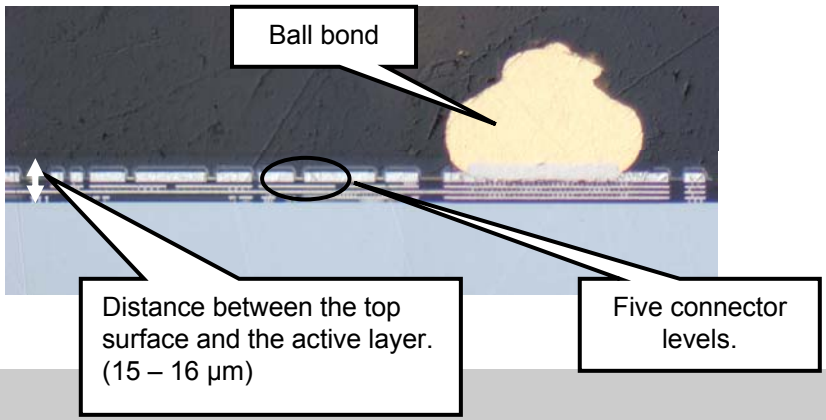


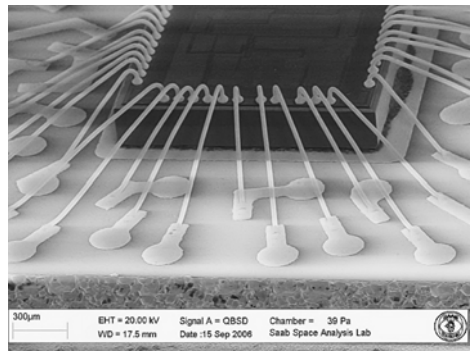
Low Ion Range

- Test of FF in 54AC374 from ST @ IPN
  - SEU free LET ≤ 93 MeV/mg/cm2 ;
    - ✓ Ion ^{127}I, range 30µm, tilt 48º, Fluence 1E+6
    - ✓ (10^7 ions/cm2 forgotten for CNES / ESA reports)
- Test of FF in 54AC273 from ST @ UCL
  - This could be due to range or test set-up



- Ions of short range require detailed information about DUT

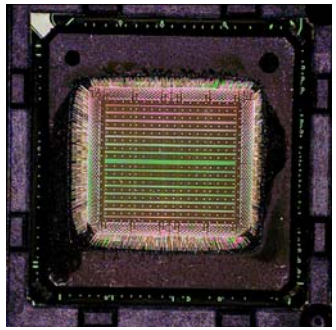




SEM picture of small ASIC

Problems with High Ion Flux @ High LET Values

- Evaluation of "Commercial" Parts Not Seldom Etched Plastic Parts Tested in "Special Evaluation Campaigns"
- Device preparation delicate work
- Complex Devices Normally Requires Complex Test Boards
  - Test induced effects frequently observed
    - ✓ Problems related to charging of the device
    - ✓ "Spurious Events" due to conflict on "test board " level / high error rate
    - ✓ Flux related double bit errors (TMR designs)
  - Hick-ups may require restart of test run



- Low flux @ high LET required
  - 10^7 ions/cm2 @ 100 ions/sec $\Rightarrow$ 24h beam time
  - Solution for Latch-up: Dedicated test and test board

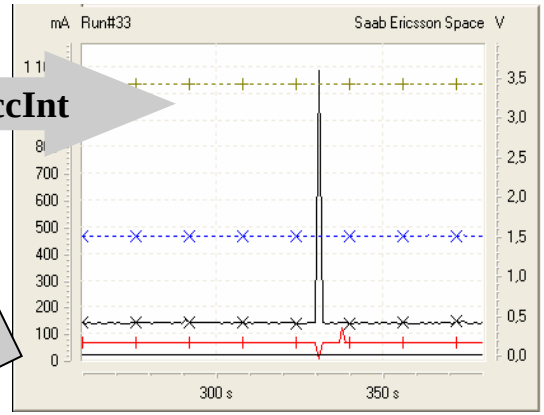
SAAB TECHNOLOGIES SAAB

LESSONS LEARNED from Xilinx

”Dead lock” events

Heavy Ions at RADEF, Finland

>1 Amp spike on IccInt



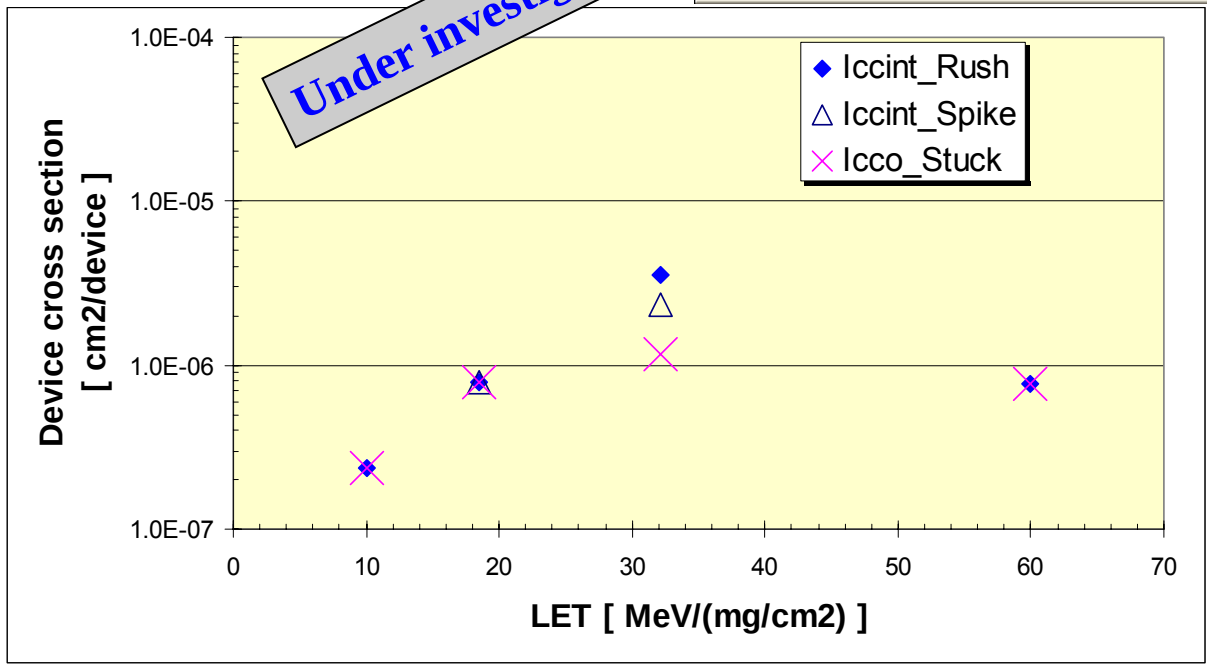
Latch-up Like Events

- Required Power Cycling to recover test system

Etched plastic samples, ~ 200 out of ~700 bonds used

Test system or circuit problems?

Under investigation!



Example of Complex Device

- AT697E Sparc Processor from Atmel
  - TMR design of Std FF in 0.18µ technology
  - Latch-up performed in separate tests to 1E+7
- Users are referred to Atmels data
  - Heavy Ion Flux ~ 1000 ions/cm2/sec
    - ✓ Xe 5E+5 ions, errors > 10,
    - ✓ Ar, 5E+5 ions, No error
- Reliability aspects
  - Unacceptable fluence at LET 14 (Ar)
  - Flux issue; Comparing data @ lower flux needed

SEU/SET dynamic test data @100 MHz for AT697E

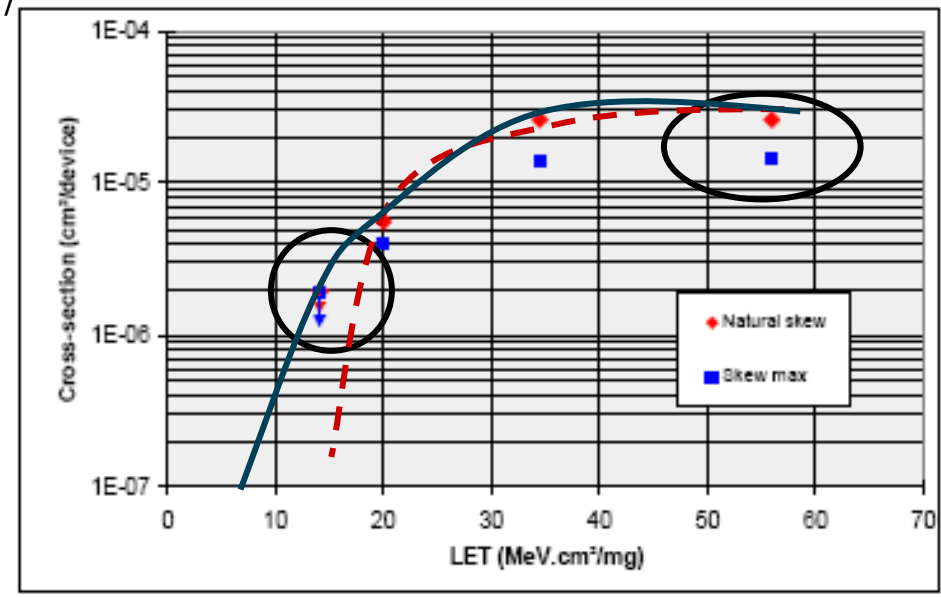


Fig. 7 : Uncorrectable errors cross sections (in cm^2/ device) at 100 MHz, for natural and maximum skews

Conclusions & Topics for the Round Table

- Are we rejecting / destroying useful devices by over testing ?
- For radiation analysis we have a “blunt” tool in CREME96
  - What is a realistic ratio between sensitive depth and sensitive area (Z=X/?)
  - Likely, we have observed test induced problems in Mosfet, SRAM, DRAM, E2prom, FlashProm, FPGA,…
  - Is high fluence testing at Xe really necessary?
  - Reliability aspects require this, but are the numbers realistic
- SEL special test @ high flux to 1E+7
- SEU/SET tests to lower fluence


www.space.se
Thank You for Your Attention