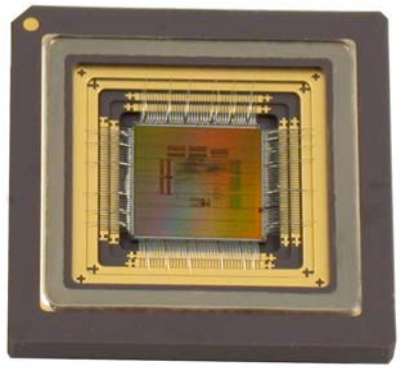
LET requirements impact from a manufacturer perspective



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Overview

- LET requirements
- Design implications
- Technological consequences
- Testing issues
- Conclusion

LET requirements

- **Most of the space products developed by ATMEL are partly funded by ESA or CNES**
- **LET requirements based on agencies input**
- **Up to now :**
  - **SEL requirements : no SEL below 70 MeV/mg/cm2 at room temp**
  - **SEU requirements : no SEU below 25 MeV/mg/cm2**
  - **Error rate for a complex product (processor, SRAM based FPGA…) : on a case by case basis**
- **Since 2005, growing concern for temperature tests (SEL related)**
  - **Some test results are requested for most recent products**
  - **Can result in strong constraints if high LET / max temperature / max voltage is requested**

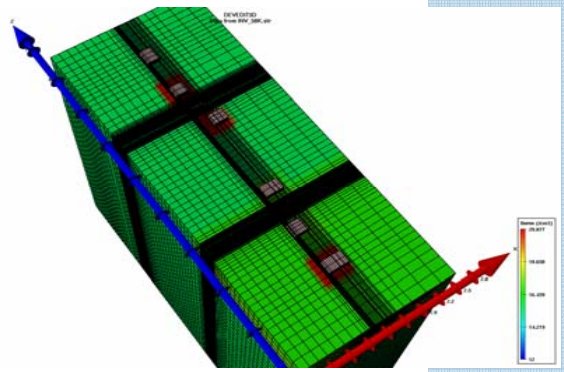
Design implications

- **The collected charge has a strong impact on the mitigation techniques to be used for space products**

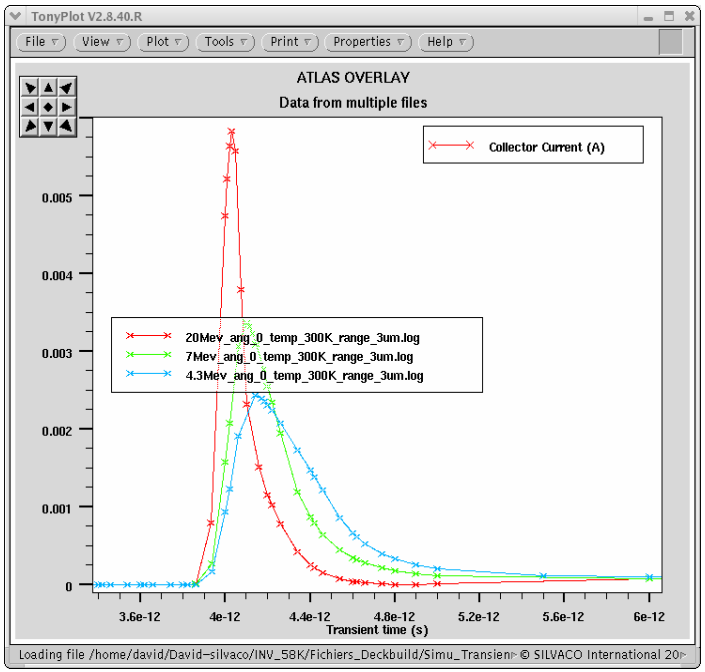
- **SEU/SET**
  - **The heavy ion induced pulse width is linked to the LET and to the location of the impact.**
  - **Multiple collection aspects**

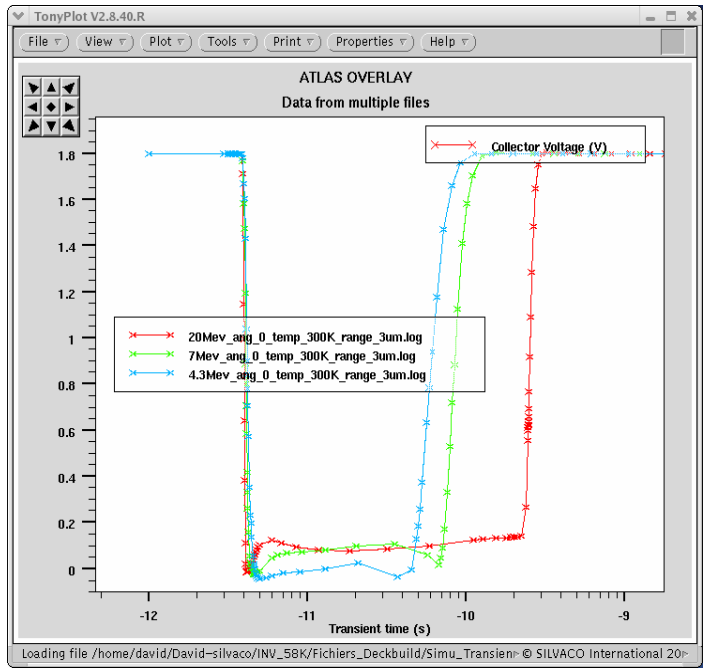
- **SEL**
  - **Body tie density**
  - **Guard bands**

SET pulse width



- **3D simulation of an inverter of the ATC18RHA CMOS 0.18µm technology**

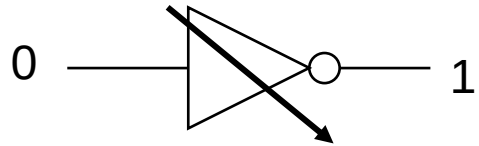


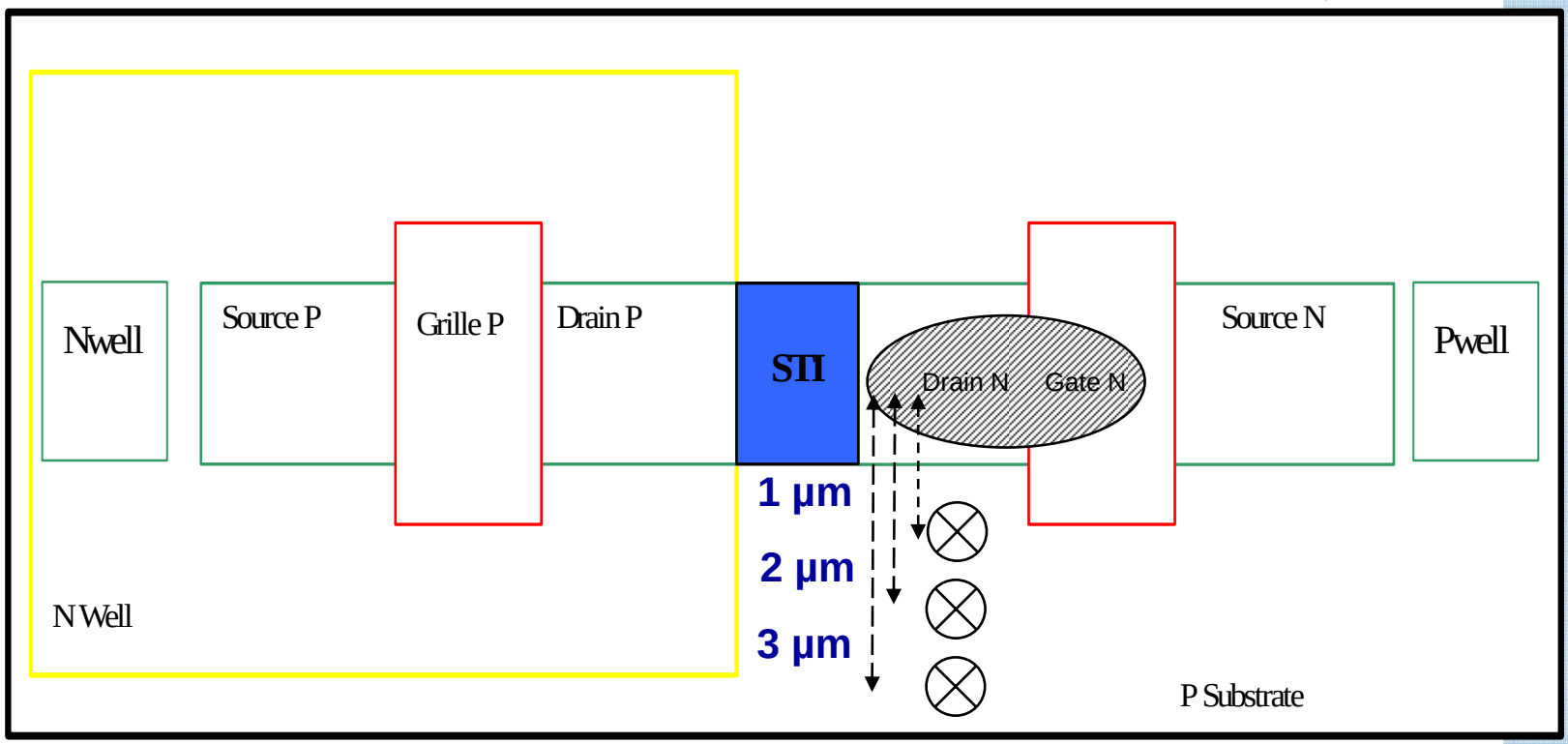


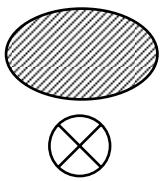
The duration of diffusion increases with LET.
The Voltage duration increases with LET.

Influence of heavy ion impact location

- **Inverter**



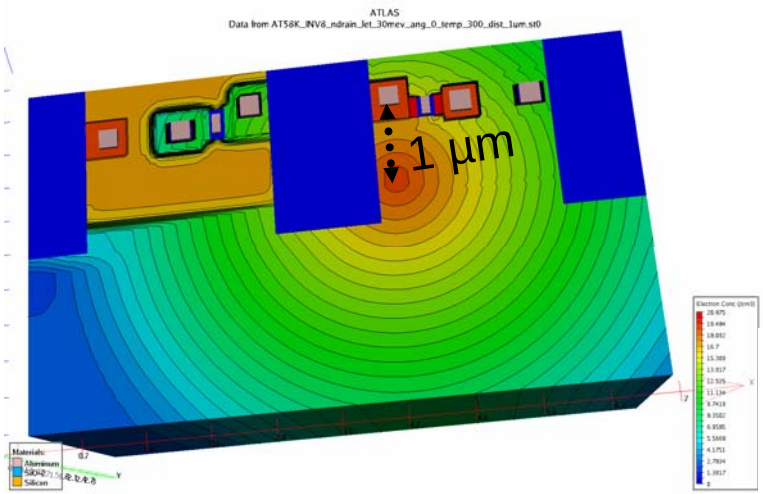


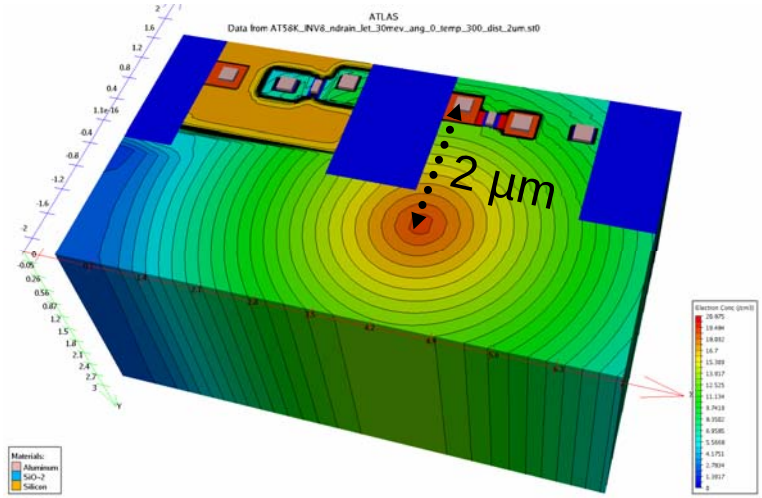


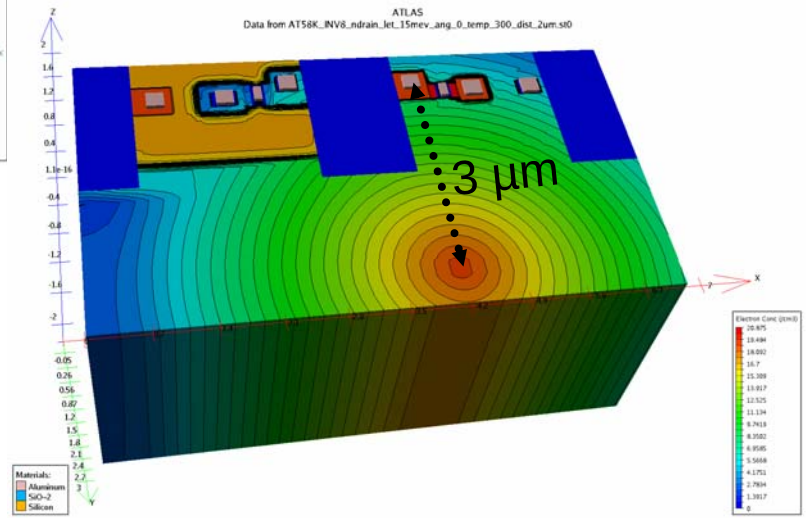
: The most sensitive area

: Heavy-ion impact

Heavy ion impact

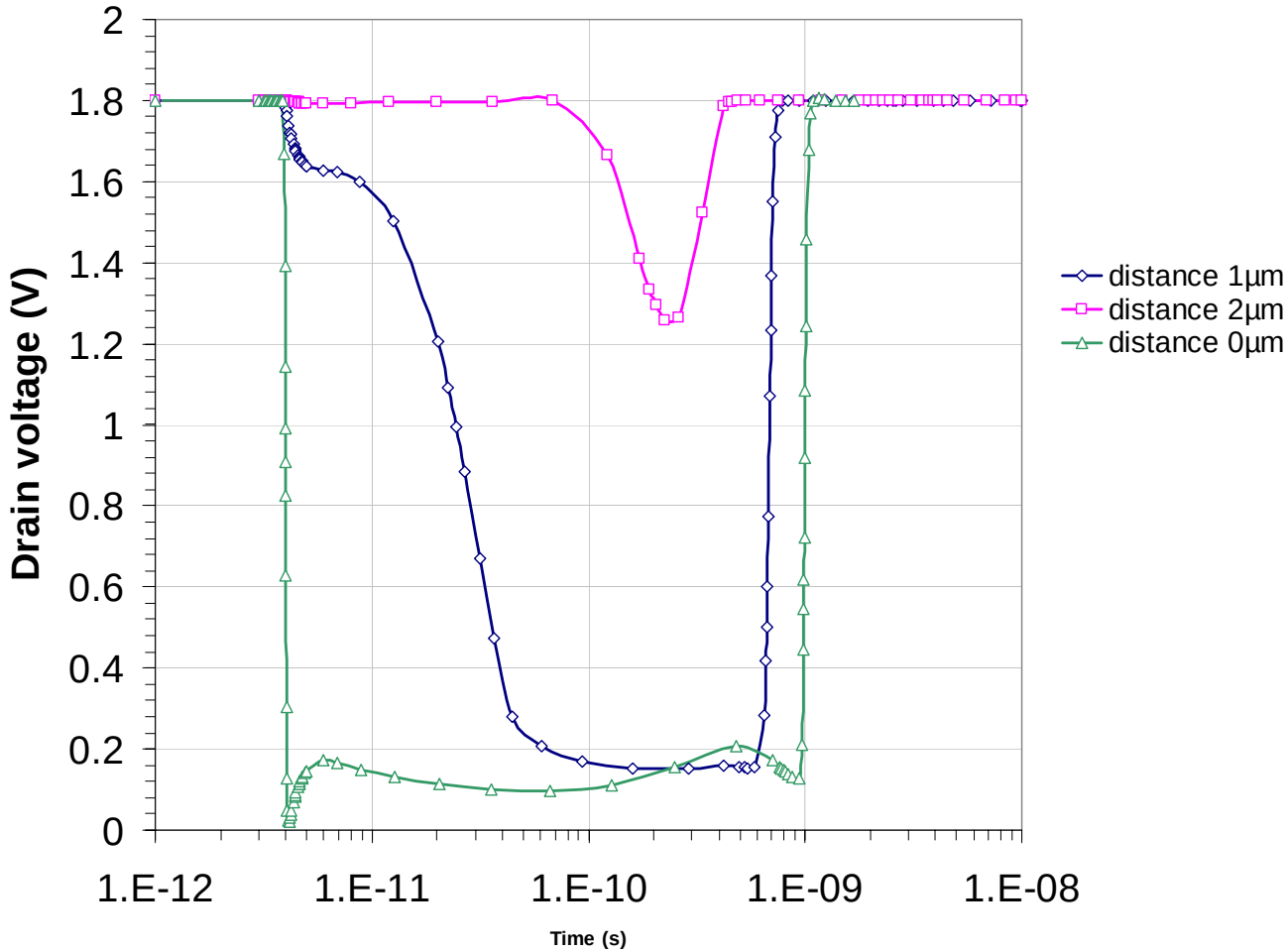






Example of location impact influence

- **LET = 30 MeV/mg/cm2**



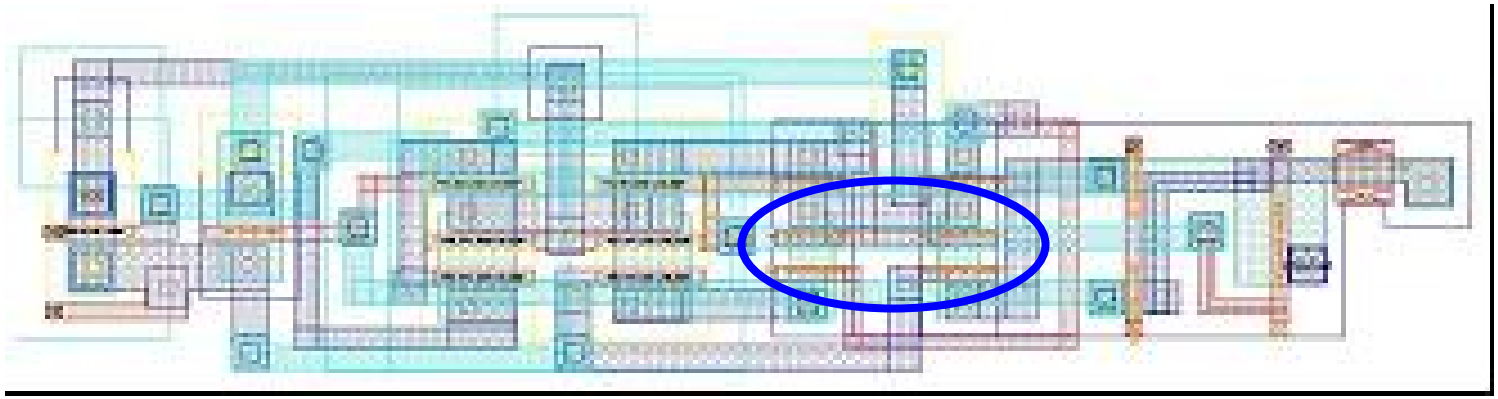
LET influence on pulse shape

- **For a given LET value, when the distance increases:**
  - **The current magnitude and duration decrease**
  - **The voltage magnitude and duration decrease**
  - **Moreover, both current and voltage pulse are delayed.**

- **No trivial law to assess V and I variation with the LET and the ion location**

Multiple collection

- **Layout influence**
  - **Example of AT40K FPGA HDFF SEU sensitivity**



Design mitigation techniques

- **Design mitigation techniques efficient up to a certain quantity of collected charge**

- **Impact on :**
  - **Cells size : ASIC density**
  - **Cells speed : max frequency**
  - **Cells power consumption**
  - **Complexity of the design implementation (e.g. the use of Triple Modular Redundancy techniques)**

Technological aspects

- **The technogical and process methods to be used to be protected against SEE are impacted by LET**
- **Particular case of SEL**
  - **Epi layer characteristics, well dose implants, SOI …**
  - **Trade-off with other phenomena such as ESD**
- **Qualification**
- **Process monitoring**

Testing issues

- **High LET and penetration depth**
  - **Number of metal layers increases with advanced technologies**
- **High LET (> 70 MeV/mg/cm2) with normal incidence not available at UCL or JYFL**
- **Use of GANIL to reach 95 MeV/mg/cm2 when requested by some customers**
- **Complex ASICs : SEL test at high LET is disturbed by SEU/SET/SEFI effects**

Conclusion

- **Targetting a certain (high) LET value has an impact on :**
  - **Design**
    - **Number of gates**
    - **Maximum speed**
    - **Power consumption**
  - **Technology / Process**
    - **Process or technology improvements have to be qualified and often imply a trade-off with other features**
  - **Testing**
    - **Limited places**
    - **Complexity**
- **Existing max LET definition : “As High As Achievable”**
- **Is it Reasonable?**

The end

Thank you for your attention !