Summary of LET Requirements/Testing

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Natural Space Environment Radiation Regimes*

- High (~10% of mix)
  - > 100 krads (Si)
  - May have
    - long mission duration
    - intense SEE environment
    - intense displacement damage environment
- Moderate (~65% of mix)
  - 10-100 krads (Si)
  - May have
    - medium mission duration
    - intense SEE environment
    - moderate displacement damage environment
- Low (~25% of mix)
  - < 10 krads (Si)
  - May have
    - short mission duration
    - moderate SEE environment
    - low displacement damage environment

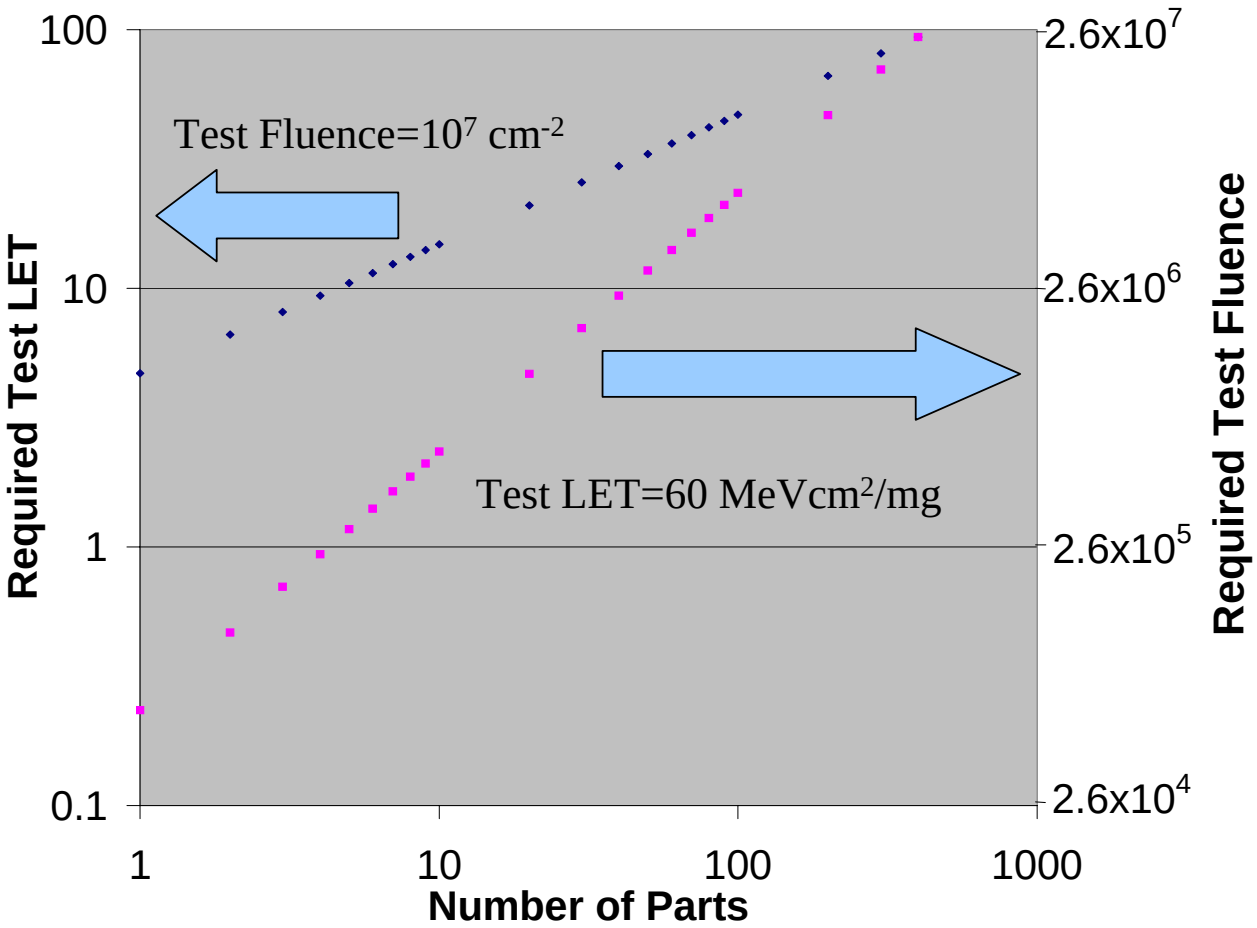
Examples: Europa, GTO, MEO Type of device: Rad hard (RH)	Examples: EOS, highLEO, L1, L2, ISSA Type of device needed: Rad tolerant (RT)	Examples: HST, Shuttle, XTE, Orion Type of device needed: SOTA commercial with SEE mitigation
Use Rad Hard Parts Radiation test needs: Low SEU: LET>37 MeVcm^2/mg SEL: LET>70-80 MeVcm^2/mg	Use Rad Tolerant Parts Radiation test needs: Moderate to High SEL: LET>70 MeVcm^2/mg	May Use COTS Parts Radiation test needs: High SEL: LET>37 MeVcm^2/mg

*Shamelessly lifted from Ken LaBel's "NASA Radiation Technology Needs"

Effect of System Complexity

Test Fluence/LET to achieve a 1% failure probability @95% CL given a null result.

Assumes FOM error rate and 95% WC Poisson downward fluctuation @ highest LET.



The Problem: It's No Longer Just LET

Some testing needs are difficult to meet at low-energy facilities.

Test Fidelity

1) Single-Event Latchup (SEL)
2) Single-Event Gate Rupture/ Burnout (SEGR/SEB)
3) Multi-Cell/Multi-Bit Upset (MCU/MBU)
4) Nuclear Scattering with high-Z recoils

Summary: Some SEE risks inherently depend on ion energy as well as LET

Testability

1) Novel Packaging (e.g. flip-chip, BGA)
2) Increased Integration (System on a chip—SOC—and System in a Package—SIP)
3) Novel Test Conditions (e.g. cryogenic testing)

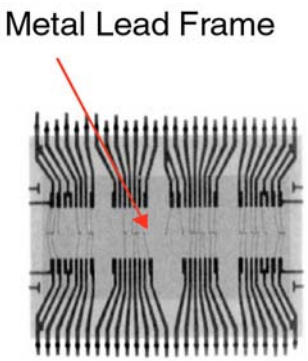
Summary: What matters is LET at the sensitive volume.

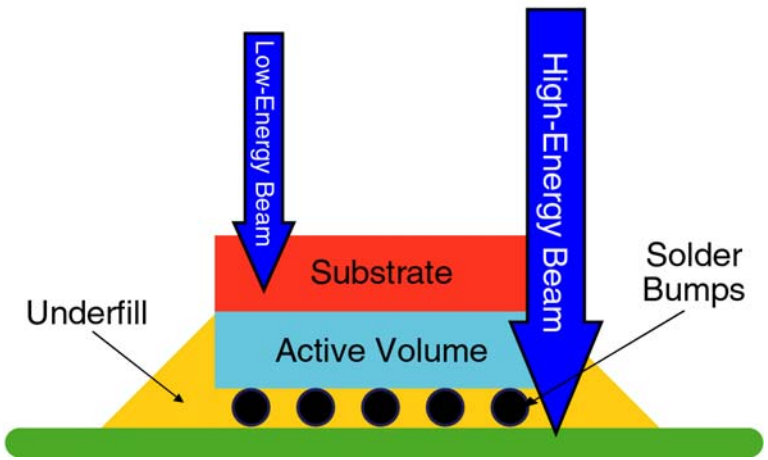
What matters is charge collected in the sensitive volume!

Challenge: Develop qualification methods that effectively reduce risk while not making the cost of qualification prohibitive.

Testability Issues

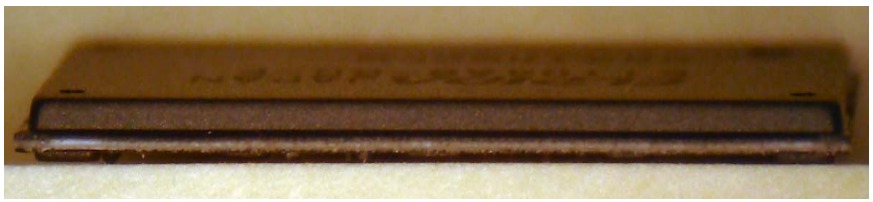
Packaging poses significant issues for testing state-of-the-art microcircuits. Metal lead frames, flip-chip/BGA/CGA pose significant barriers to reaching die active area and to knowing the LET when you do. Die are also becoming thinner—and so more fragile—but still not thin enough to test at low-energy facilities.

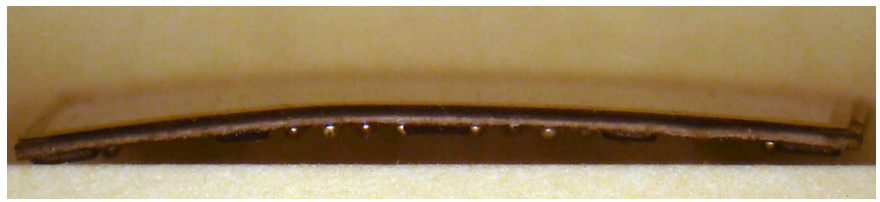




Testability Issues (Continued)

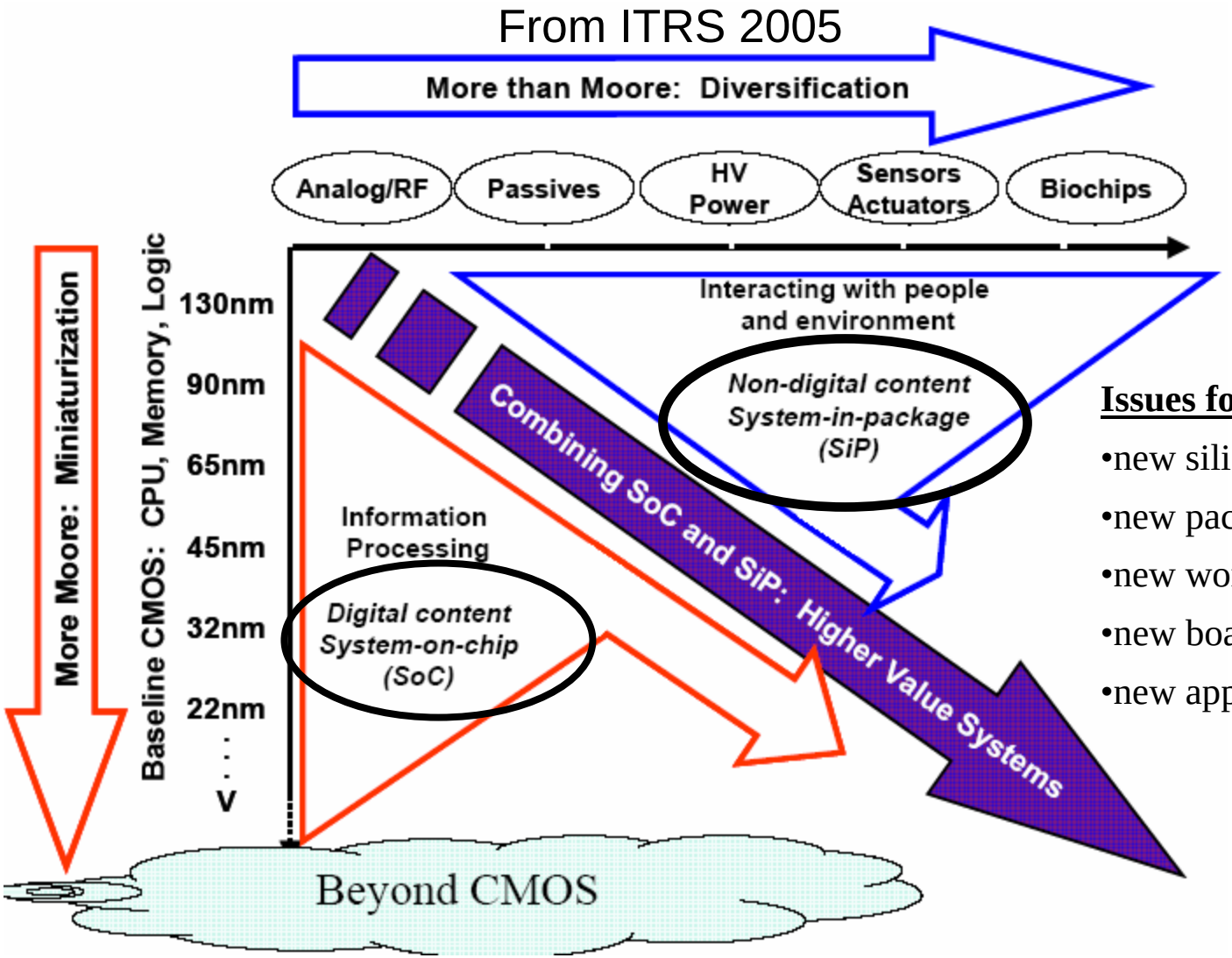
Preparing die for testing is becoming more difficult. DDR2 SDRAM from Samsung had initial thickness of ~250 microns. After thinning to ~150 μm, the cracks on the preceding slide were noted. Edge-on photos show the likely cause was buckling of the die when it became too thin to support the strain on it.





Note that the bowing in the middle has pulled up solder balls off of the carrier. Where does this stress come from? Will it be a general feature in deep submicron feature size CMOS?
Parts are 90nm feature size 1 Gbit DDR SDRAMs in 68 pin FBGA

Integration Poses Testability Challenges



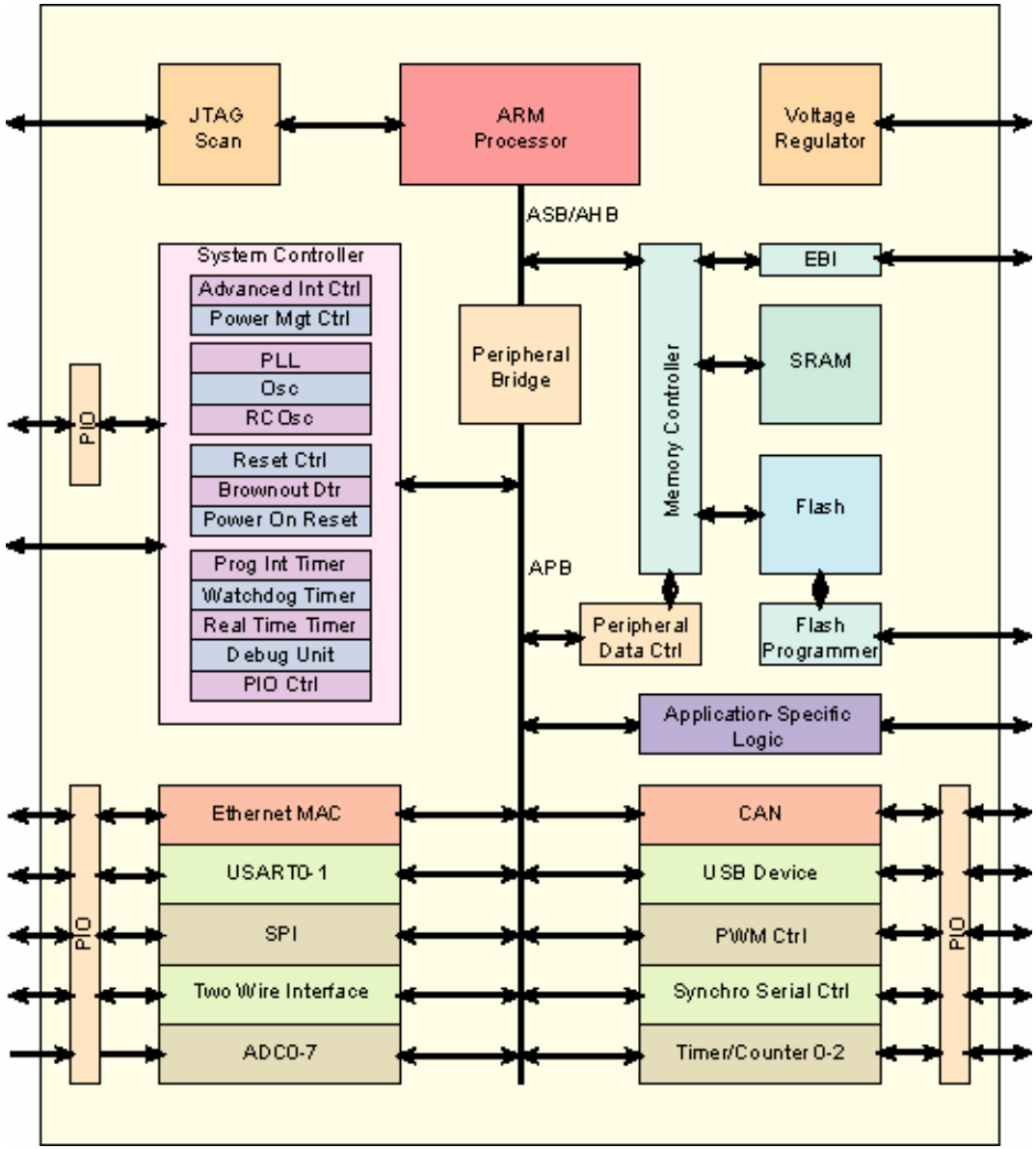
Issues for New Technologies

- new silicon
- new packaging
- new workmanship
- new board/carrier material
- new application/programming

*lifted shamelessly from ITRS-2005, Executive Summary

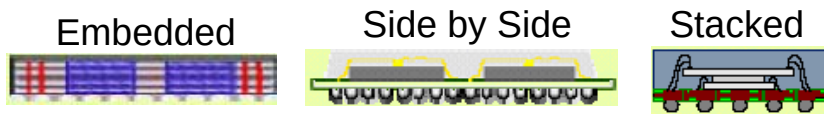
Challenges on a Chip

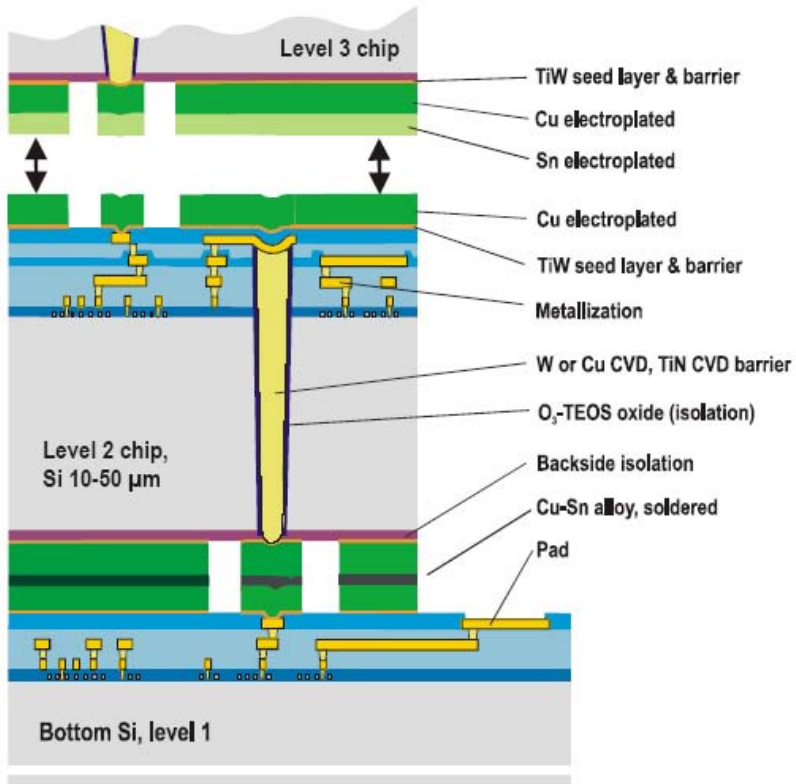
- SOC poses challenges for several reasons
  - Complex control logic means complicated SEE data especially for broad-beam irradiation
  - Many functions means many complex processing steps
  - High integration level means SOTA processing, new structures, materials and failure modes
  - “High-value” means samples are expensive



Challenges in a Package

- Reasons for SiP
  - Resolves timing issues
  - Allows integration of dissimilar technologies
  - More economical for small-scale manufacture
- System-in a Package also poses challenges
  - Die are often thinned and rely on packaging for support
  - Repackaging may damage parts or alter SEE response
  - Even if repackaging succeeds, signal-integrity and fidelity pose significant challenges
  - Thinning/laser testing won't work

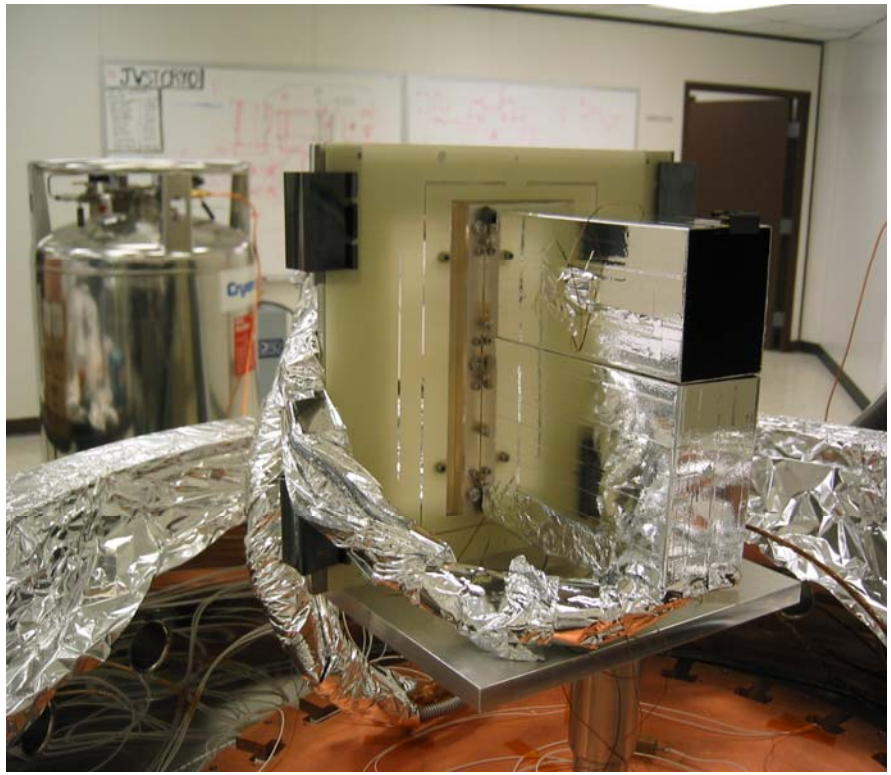




*adapted from ITRS-2005, Assembly and Packaging

Novel Test Conditions

- Space missions are also changing
  - New environmental conditions
    - Cryogenic Operation for IR detectors
    - Extreme Temperature Fluctuations
  - The Low-Energy Frontier
    - Material degradation studies
      - JWST sunshield required protons with energy <100 eV
    - Displacement Damage
      - Low-energy protons important to map out Coulomb dependence of damage.



Apparatus used by BATC to test MOSFETs for enhanced Gate Rupture susceptibility at cryogenic Temperature.

High-Energy Facilities: An Answer?

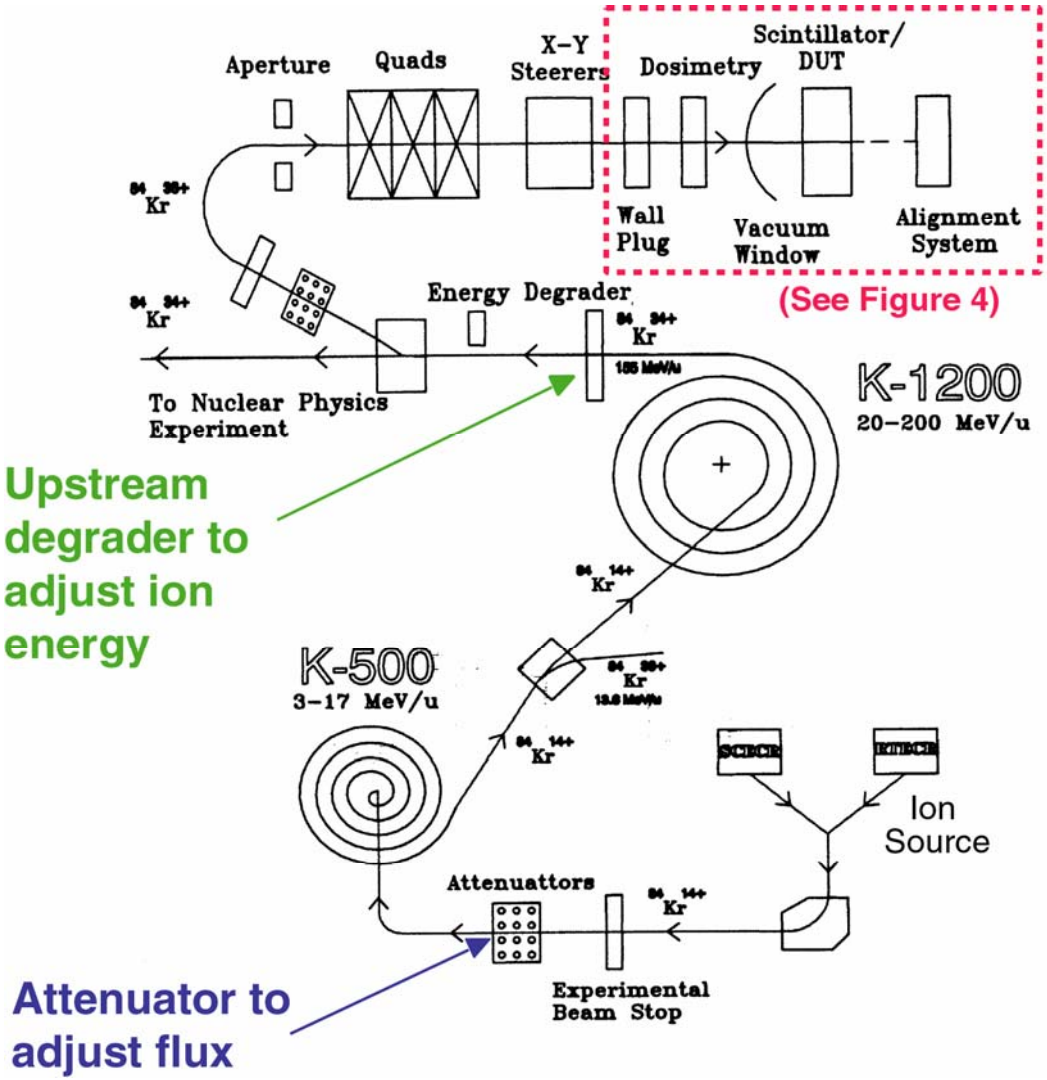
Michigan State delivers ions with energies up to 120 MeV/amu and ranges in mm, rather than microns

Ion	Maximum Energy (MeV/amu)	Incident LET in Si ($MeVcm^2/mg$)	Range in Si (microns)	Bragg Peak LET in Si ($MeVcm^2/mg$)
Ar-36	143	1.5	8860	18
Kr-78	121	6.1	4440	40
Xe-136	131	14.1	3070	69
Bi-209	72	42	1100	100

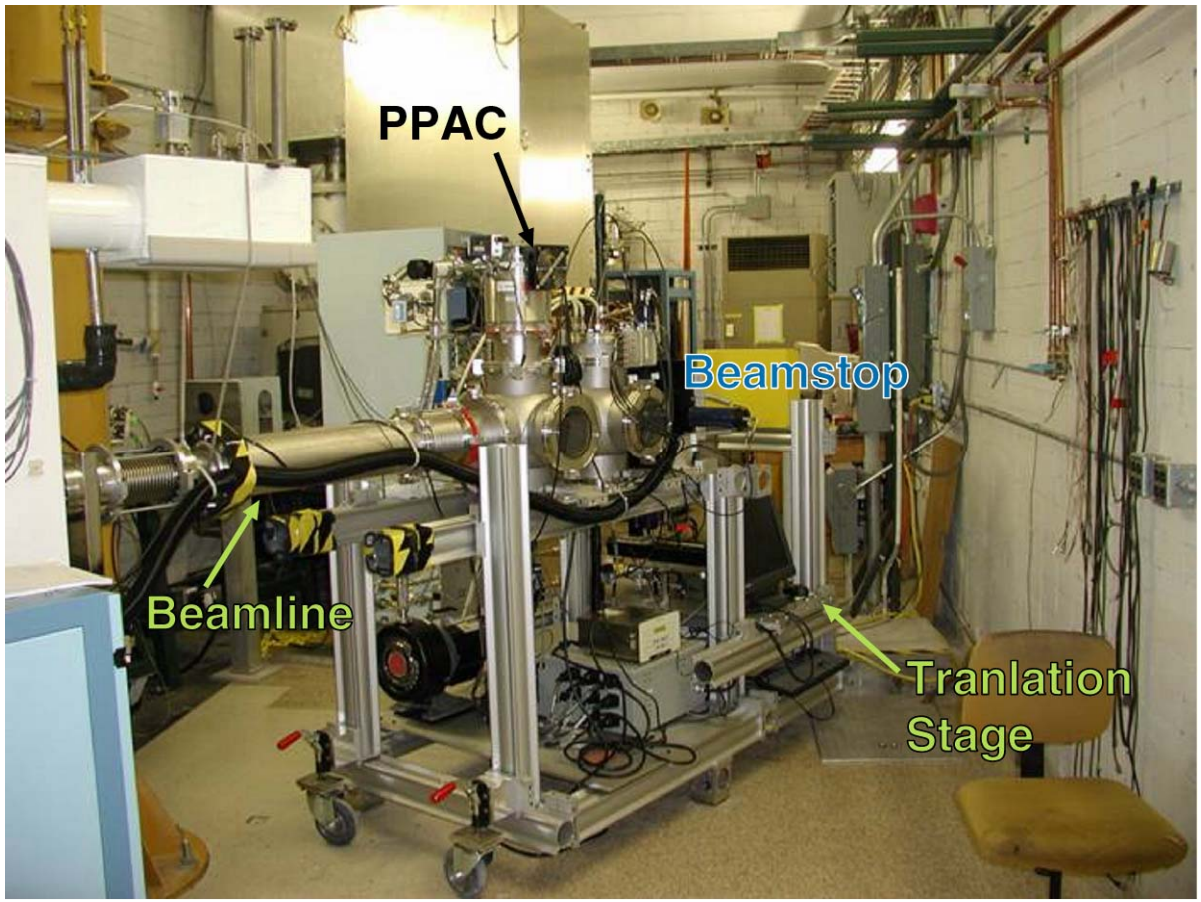
Unfortunately

- Cost is ~$2600/hr with a minimum 24 hour commitment
- Tuning to a new ion takes ~24 hours at the above rate
- High-LET beams are relatively rare (1-2 times per year).
- Initial incident LET is low (e.g. 14.1 $MeVcm^2/mg$ for Xe)

High-Energy Facilities Are Complicated

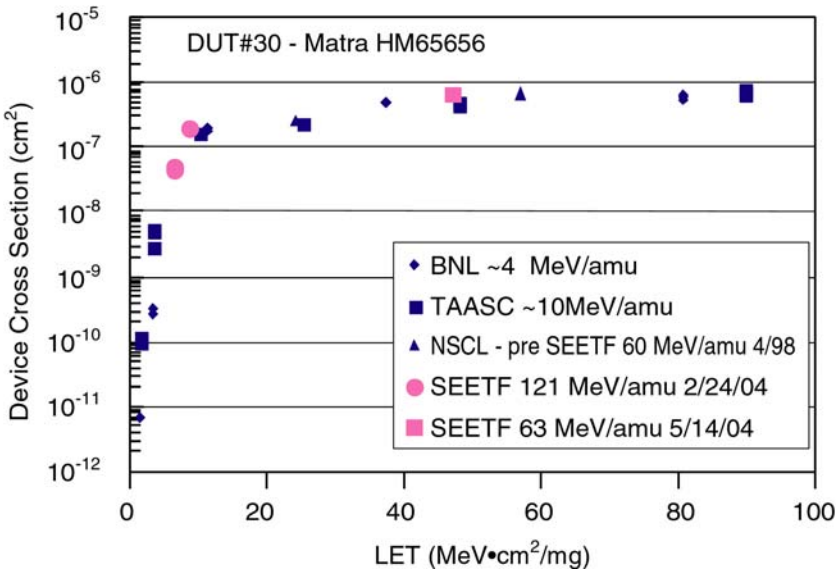


Adapting Existing Nuclear Science Facilities is Expensive

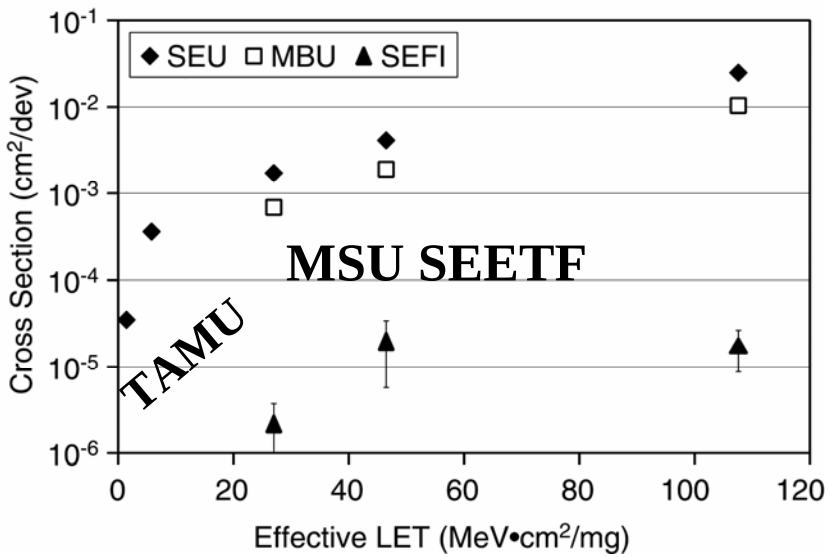


High-Energy Facilities: An Answer?

- Results at MSU's SEETF agree well with other facilities



256 K SRAM



1 Gbit DDR SDRAM

High-Energy Facilities: Caveats

- For high-energy facilities, knowing ion LET means knowing overburden in detail—plastics and other "light" materials often contain impurities.

Part	Packaging	Incident Energy (MeV)	LET @ die surface (MeV•cm^2/mg)	Average Cross Section (cm^2)
IDT71256	Lidded Plastic	9574	N/A	2.01×10^{-3}
IDT71256	Delidded	9574	6.3	1.08×10^{-3}
IDT71256	Lidded Plastic	5953	N/A	6.92×10^{-5}
IDT71256	Delidded	5953	8.7	5.15×10^{-3}
M65656	Lidded Plastic	9574	6.3	4.89×10^{-2}
M65656	Delidded	9574	7.1	1.35×10^{-1}
M65656	Lidded Hermetic	5953	11.7	1.61×10^{-2}
M65656	Delidded	5953	6.3	1.25×10^{-2}

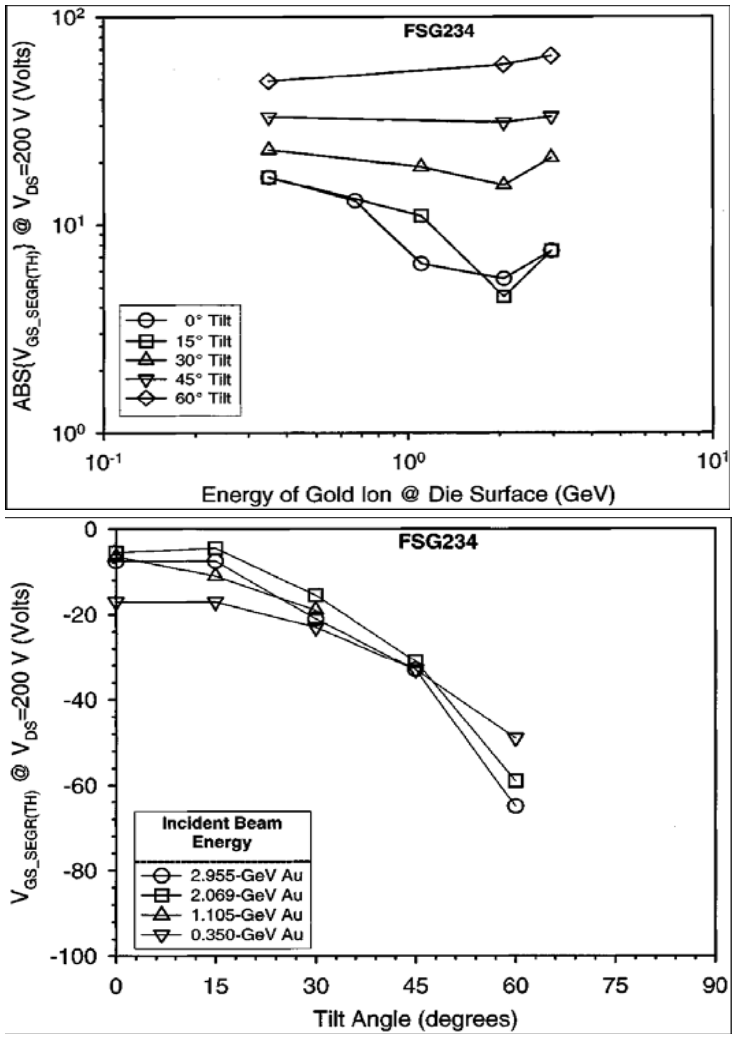
- Range-out of ion beam
- Straggling and beam spreading can alter LET and flux
- Achieving high LET done by degrading primary beam and can be time consuming
- Not a panacea

BUT! When you need it, the facility is invaluable.

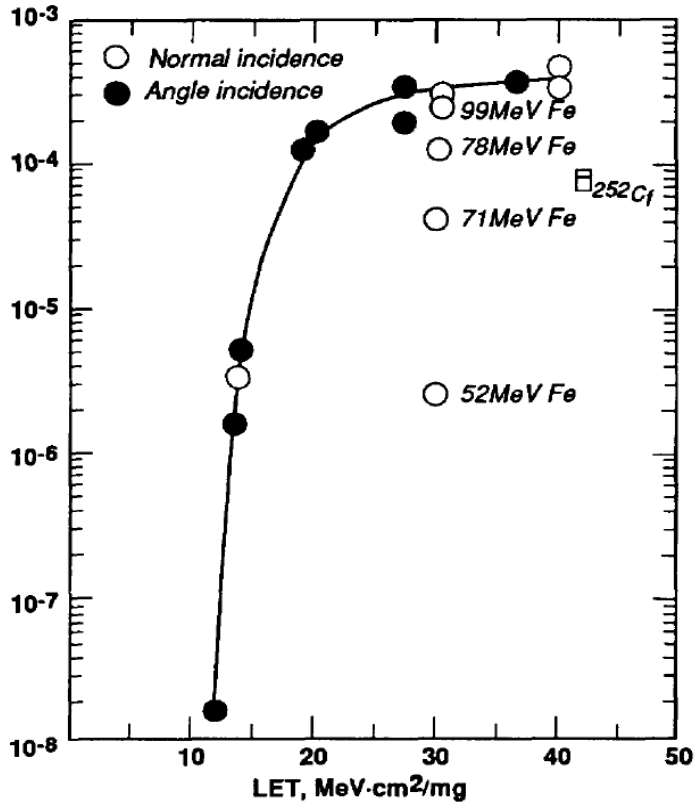
Testability: Summary

- Scaling makes devices more difficult to test
  - Greater integration means more complicated SEFIs and increasing importance of SETs
    - May be very difficult to characterize fully with broad-beam radiation
    - Current microbeams may not have sufficient range
    - Laser testing is much more difficult due to metallization—even from the back side
  - New Packaging makes it more difficult to prepare parts for testing without damaging them or altering their performance
    - BGA, SIP and SOC all pose challenges
  - New materials and structures *may* introduce new failure modes.
- High-energy facilities offer greater penetration, but are more difficult to work at and more expensive.
- Ability to do micro—or at least “mini” beam testing could be very useful for figuring out vulnerabilities for SOC.
  - Metallization may preclude or at least complicate laser testing.

Test Fidelity: Range and Destructive Failure



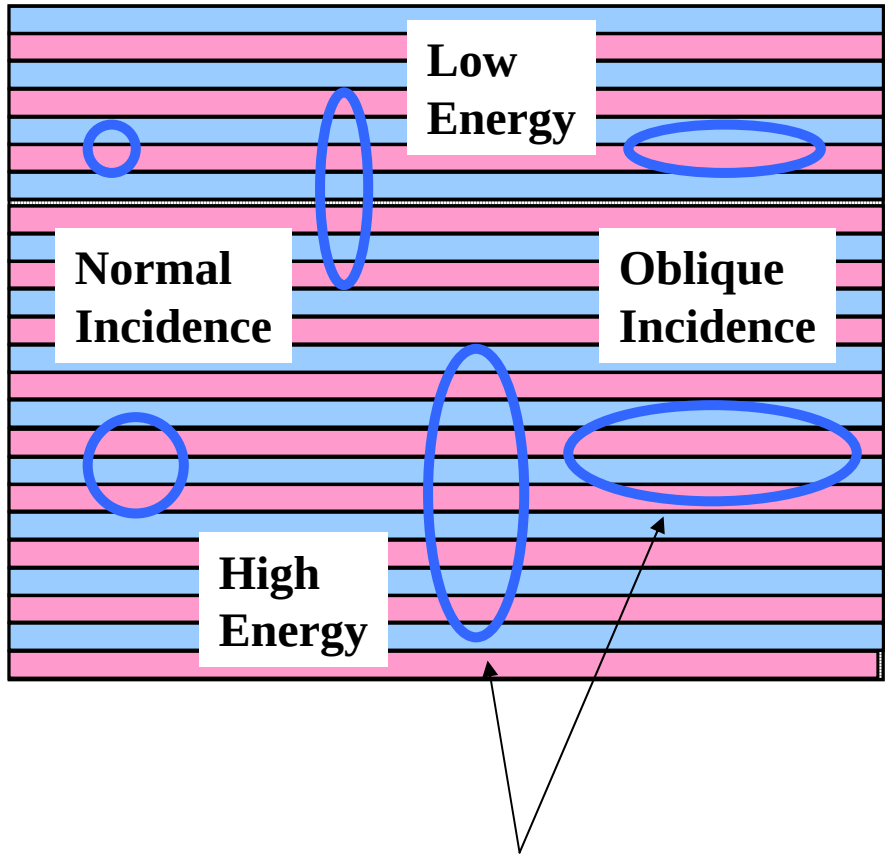
Titus et al. showed SEGR susceptibility depends on ion energy.



- Levinson showed that ion range influenced SEL cross section [Single Event Latchup (SEL) in IDT 7187 SRAMs-dependence on ion penetration depth," RADECS 93 (1993)]
- But how much range is enough?
  - Current best guesses >60-100 microns

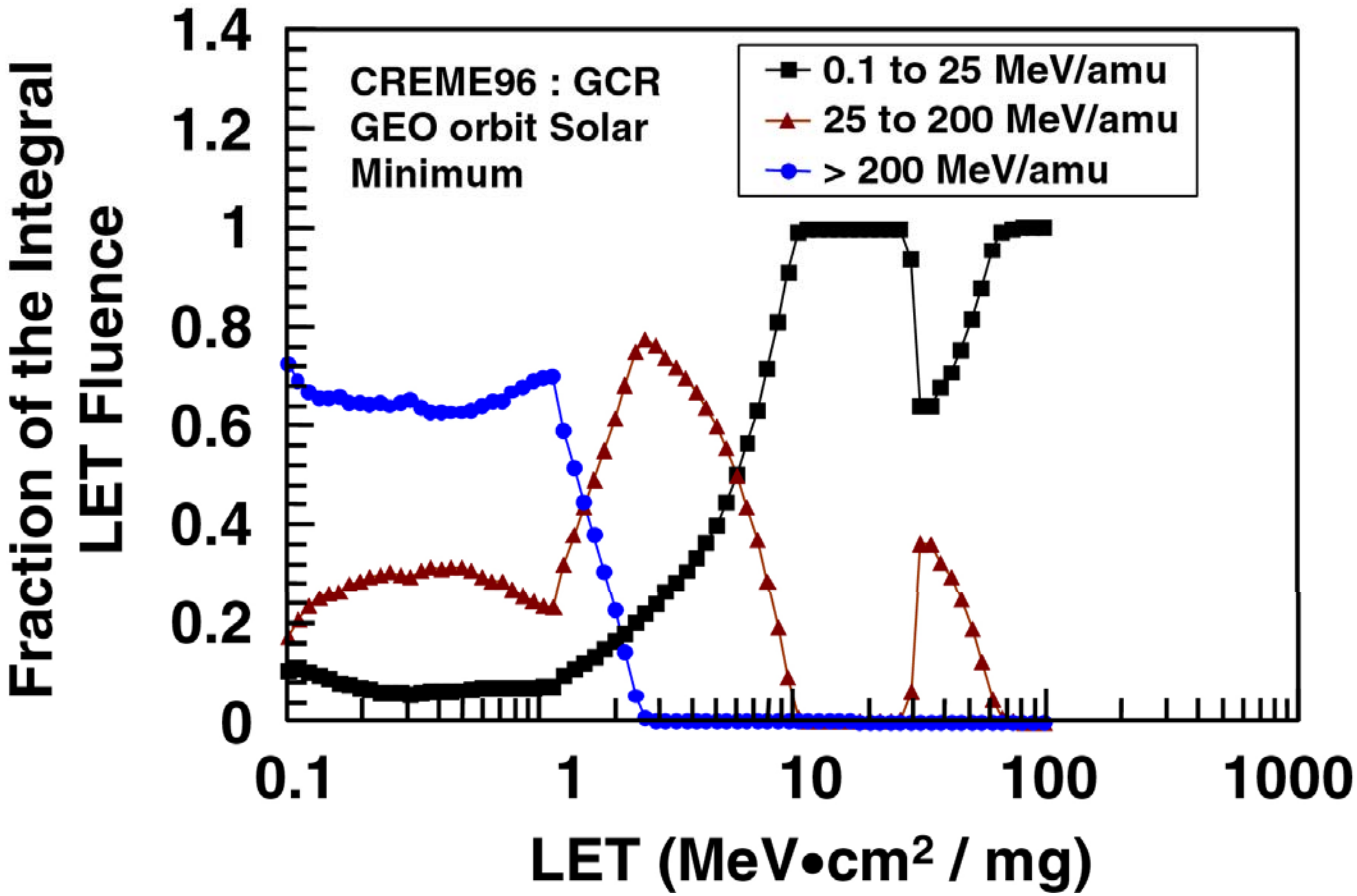
Test Fidelity: Multi-Cell and Multi-Bit Upsets

- Shrinking technologies mean more bits upset per ion, but not always more MBUs
  - Many memories separate logically related bits by interleaving them with unrelated bits—but there's a limit
  - High-energy ions produce broader ionization tracks even at normal incidence and longer tracks at oblique incidence.
- Will increasing cell densities reach a point where GCR ions defeat interleaving?
  - How will we know without testing with high-energy ions?



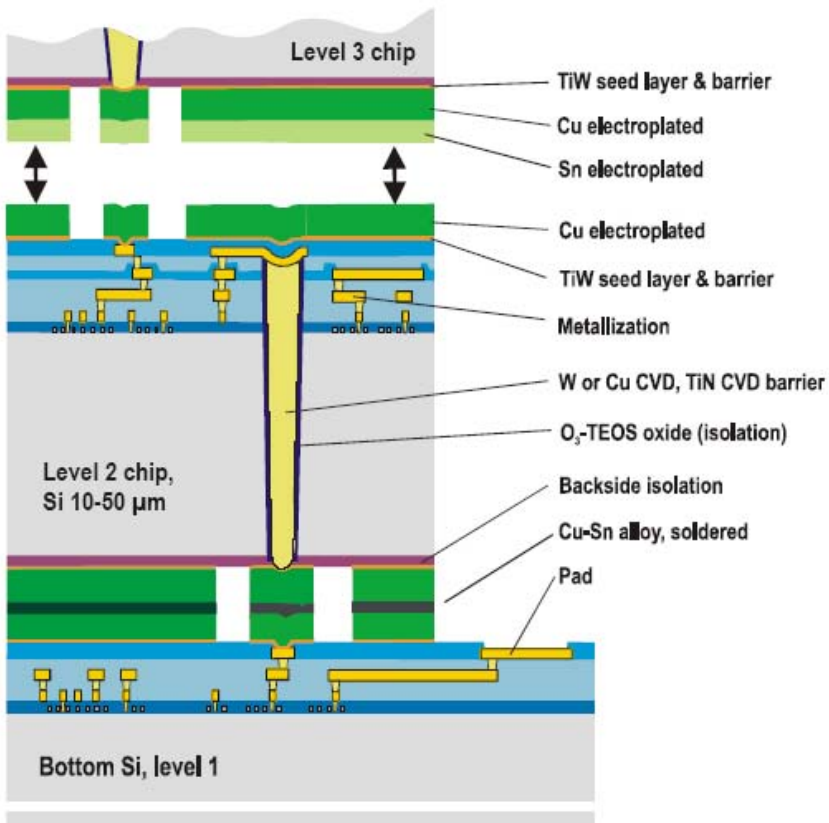
Fidelity to the Space Environment

MSU allows us to reproduce 99% of the space radiation spectrum in Linear Energy Transfer (LET) and energy for LET > 3 MeV·cm2/mg.



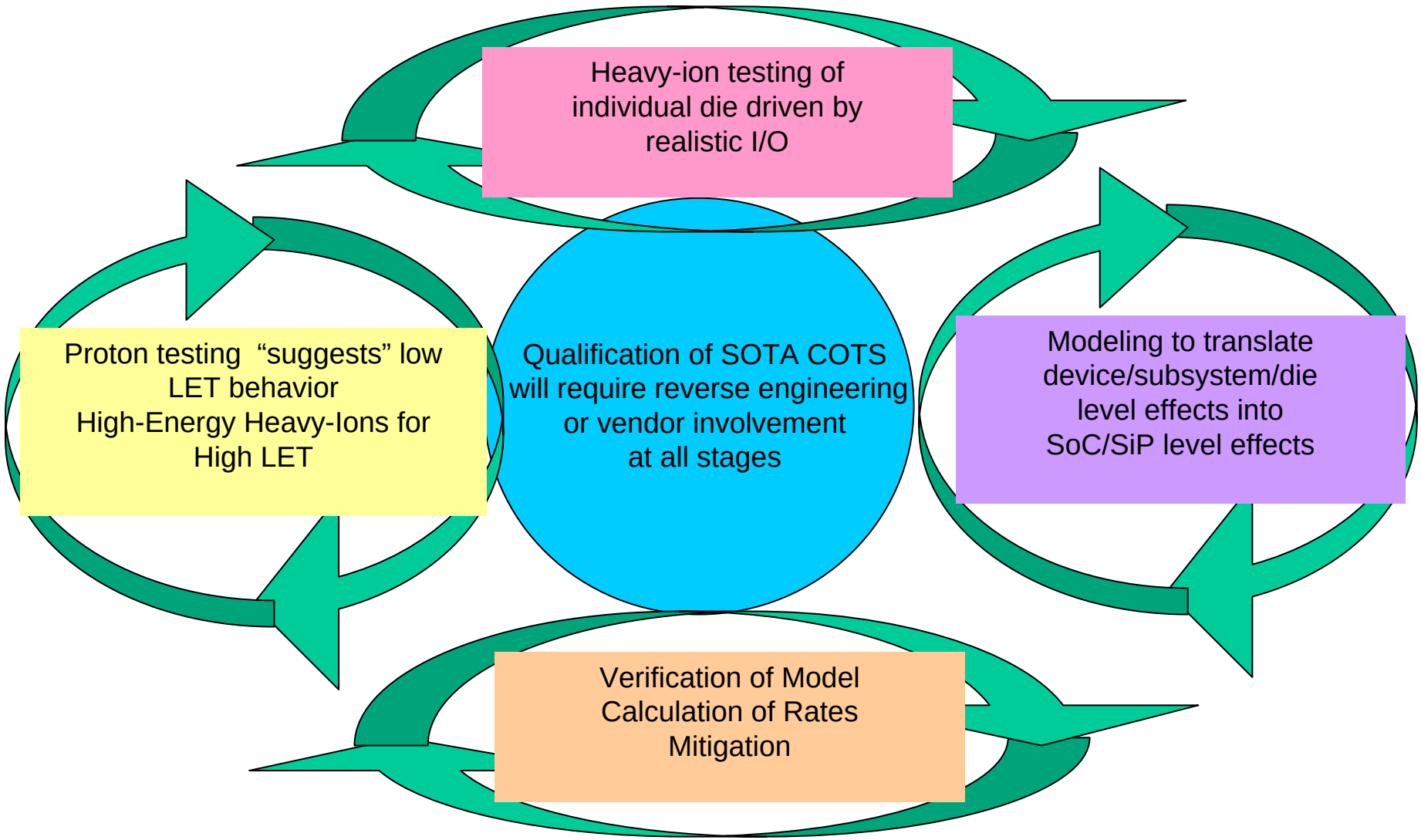
But There Is More to SEE Than LET

- LET is the right parameter for SEL, but energy/range important
- For SEGR, both LET and ion energy are important.
- Energy could become critically important for MBUs
  - Possibly important for **configuration memory** as well as bulk memory
- Also nuclear scattering by light ions
  - Warren et al. showed that recoils from nuclear scattering in metallization by light ions can cause upsets in rad-hard SRAMs



New Technologies have lots of metal in close contact with semiconductor

MY Qualification Suggestions



Conclusions

- Economics drive commercial semiconductors toward greater integration and complexity—and hence higher value
  - The drive toward SiP shows this trend will continue even if scaling fails
- Increased capability at lower weight/power drive spacecraft designers to use COTS
- Challenge: Find economical methods to qualify new technologies
  - Test facilities need to further that goal
    - High-LET and high-energy are essential for both testability and fidelity.
    - High cost per hour must be justified by higher productivity.
    - High-energy is essential to address some risks—SEL, SEGR, and MBUs
    - High-Z recoils from nuclear collisions will be range limited at accelerators, but probably not so in space
      - We still fall an order of magnitude short of energy/amu relative to GCR peak.
- If the cost of qualification becomes too high, programs must choose:
  - Increased cost (meaning we'll be overworked)
  - Increased risk (meaning we'll be working as consultants when they fail)
  - Overly conservative design (meaning we're out of a job)

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