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EEE COMPONENT DERATING (ESA TAILORING OF ECSS-Q-60-11A)

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Addition of : "Repetitive transients, e.g. in a switching DC/DC converter operation, clock transmission lines, etc. shall not exceed the specified steady state parameter load ratio or limits. Radiation sensitive components are identified, but the user shall consult the appropriate standard to ensure that appropriate derating is applied".	2	Para 2.1

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1 INTRODUCTION

This document applies in conjunction with ECSS-Q60-11A. It details the mandatory tailoring of EEE component derating specified in ECSS-Q60-11A applicable without exception to all ESA programmes. The tailored paragraphs listed in this document replace the equivalent paragraphs of ECSS-Q60-11A entirely. All other paragraphs of ECSS-Q-60-11A apply without tailoring.

2 DERATING

The following sections show the tailored derating requirements for ESA programmes. The relevant ECSS-Q-60-11A paragraph number has been maintained in the heading for each section for ease of reference.

2.1 5.4 Derating parameters

Derating requirements are provided in first part of clause 7.xx for each component family.

For each category, the parameters to be derated are identified. The main parameters to be derated are:

- junction or case temperature at maximum operating conditions;
- power (rating, dissipation);
- voltage;
- current.

The parameters to be derated depend on component type.

When available, load ratios or limits are given for different mission durations or different temperatures. A stress balancing concept offers flexibility between one stress versus another (voltage and temperature). In some cases, e.g. resistors, derating has a direct impact on component performance.

When the procurement specification includes parameter values for transients or surge conditions, the same load ratios or limits as for steady-state parameters shall be used.

When transient or surge conditions are present in the application, but no transient or surge rating values are specified in the procurement specification, the design transients or surges shall not exceed the maximum steady state rating given in procurement specifications.

Repetitive transients, e.g. in a switching DC/DC converter operation, clock transmission lines, etc. shall not exceed the specified steady state parameter load ratio or limits.

Radiation sensitive components are identified, but the user shall consult the appropriate standard to ensure that appropriate derating is applied.

Where components are required to operate in protection mode or in fail-safe mode in order to prevent failure propagation (e.g. short circuit protection), the components concerned shall meet the derating requirements and application rules when performing the protection or fail-safe function under the worst failure case (i.e. highest stress applied to the components).

The worst case analysis shall include:

- drift from initial tolerances, temperature effects, ageing effects:
- any operational modes that may induce excess stress and any failure mode which must be contained and controlled: additional margins/derating/parameter degradation other than those in the relevant clause, shall be considered as necessary.

Several effects may be additive, e.g. the drift values given in the relevant clause have to be added to the initial tolerance and to the temperature coefficient effect. Radiation effects may be similarly additive.

2.2 7.2 Capacitors: ceramic , family group code: 01-01 and 01-02

7.2.1 General

a. The capacitor stress sum value of steady state voltage, AC voltage and transients shall not exceed the load ratios specified hereunder.

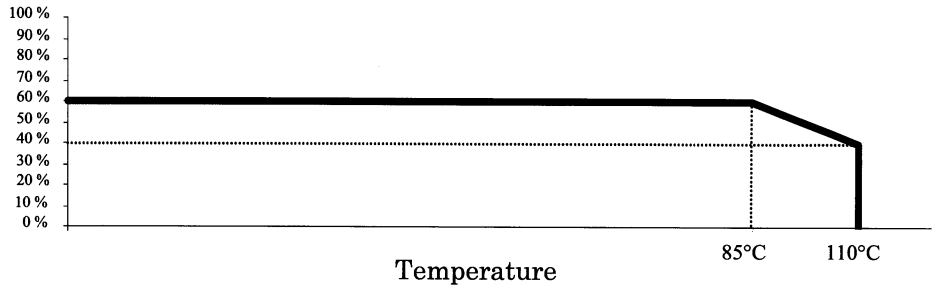
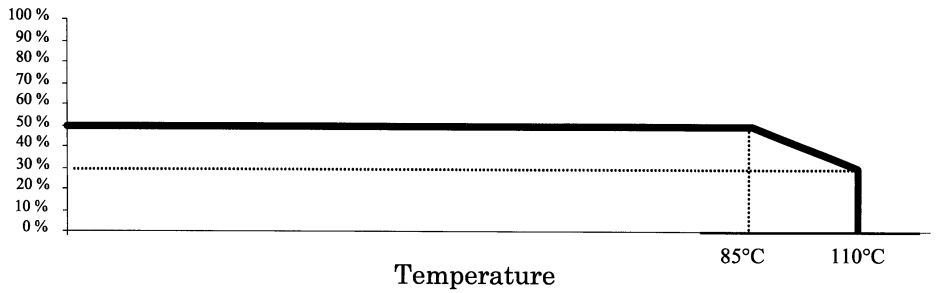
b. Ceramic capacitors are sensitive to high surge currents. Manufacturer's surge current ratings shall never be exceeded. When no surge current rating is specified, the issue shall be recorded in the design file and the component's selection shall be reviewed and approved as described in ECSS-Q-60.

c. Multilayer capacitors with a voltage rating less than 100 V may be used in low voltage (less then 10 V) continuous applications provided they have been submitted to a low voltage (1,5 V) 85 % humidity at 85 °C screening test.

d. Physical limitation for type II: maximum surge dV/dt: 100 V/ms.

e. Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.2.2 Derating

Parameters	Load ratio or limit
Voltage: rated voltage ≤ 500 V	
Voltage: rated voltage > 500 V	

2.3 7.3 Capacitors: solid tantalum, family group code: 01-03

7.3.1 General

a. The capacitor stress sum value of steady state voltage, AC voltage and transients shall not exceed the load ratios specified hereunder.

b. 100% surge current screening is required for ***all*** low series impedance applications such as power supply filters etc or when configured in parallel banks. The potential for surge current in application shall never exceed 40% of the tested surge current value reached during capacitor screening. Surge current screening shall be performed in accordance with either MIL-55365 option B, or the relevant ESCC specification. If the latter is used, then it shall be immediately preceded by the Rapid Change of Temperature test.

c. For low series impedance application or where configured in parallel banks, the capacitors used must be low ESR, high surge rated types.

d. Part date code shall differ not more than 12 months from the PCB assembly date to minimise the risk of moisture ingression (adequate storage conditions are mandatory) and to benefit from process improvements.

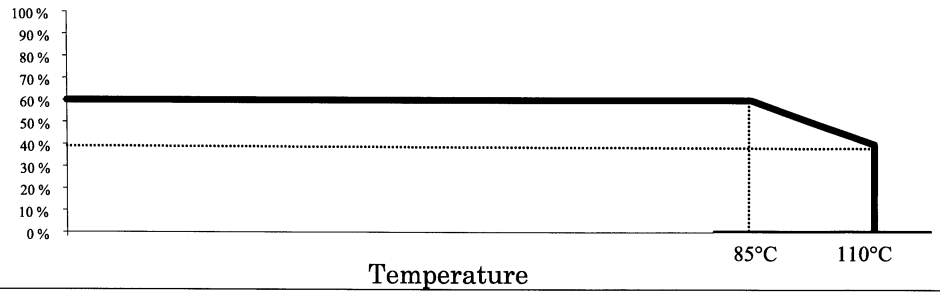
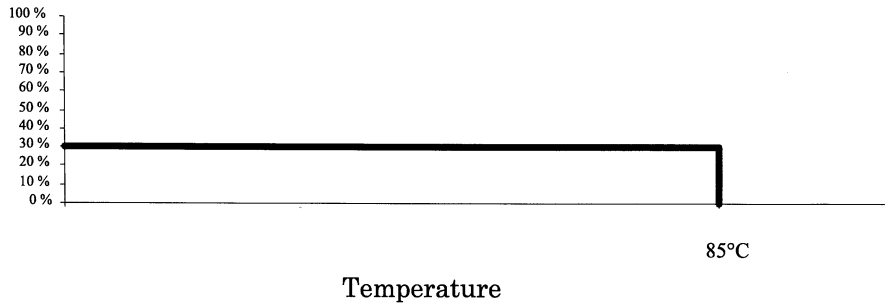
e. The manufacturer recommended soldering parameter limits may not be exceeded and additional margins must be applied subject to soldering process conditions.

f. No reverse voltage shall be applied to these capacitors.

g. Ripple power or ripple current shall never exceeded 50% of the manufacturers specified maximum value.

h. Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.3.2 Derating

Parameters	Load ratio or limit
Voltage: steady state and dynamic applications where I < 10 Amps.	
Voltage: dynamic applications where I > 10 Amps.	

2.4 7.4 Capacitors: non–solid tantalum, family group code: 01-04

7.4.1 General

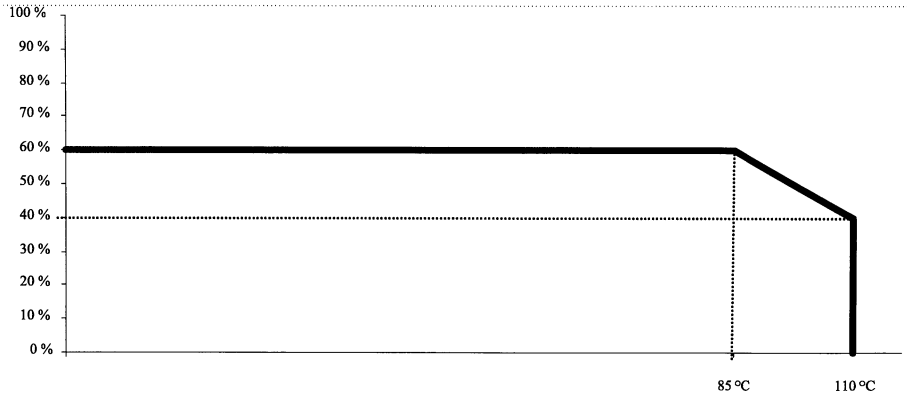
a. No reverse voltage shall be applied to these capacitors.

b. Manufacturer's ratings for ripple power or current shall never be exceeded.

c. Surge voltage shall never exceed 50 % of the specified value.

d. Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.4.2 Derating

Parameters	Load ratio or limit
Voltage: voltage includes DC voltage and superimposed AC peak voltage.	

2.5 7.5 Capacitors: film, family group code: 01-05

7.5.1 General

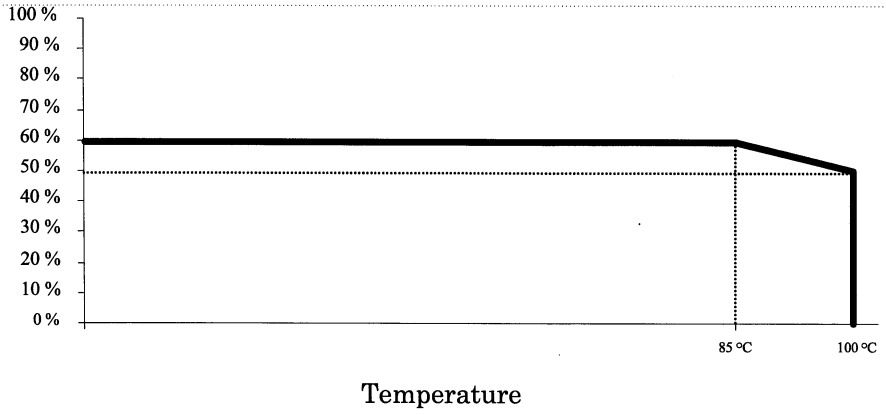
a. Self healing requirements for polyethylene terepthalate (PET, polyester) film:
   1. To have a clearing process in any case, the minimum energy available shall be > 5 mJ.
   2. To prevent any risk of destruction during self healing, capacitor banks shall not provide energy greater than 15 J.

b. For other films, clearing recommendations from manufacturers shall be followed.

c. Surge voltage shall never exceed 50 % of the specified value.

d. Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.5.2 Derating

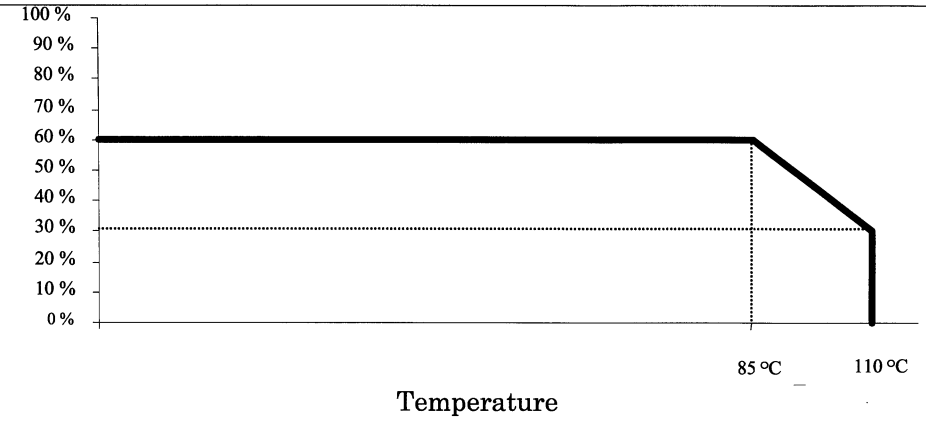
Parameters	Load ratio or limit
Voltage: voltage includes DC voltage and superimposed AC peak voltage.	

2.6 7.6 Capacitors: glass and porcelain, family group code: 01-06

7.6.1 General

Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.6.2 Derating

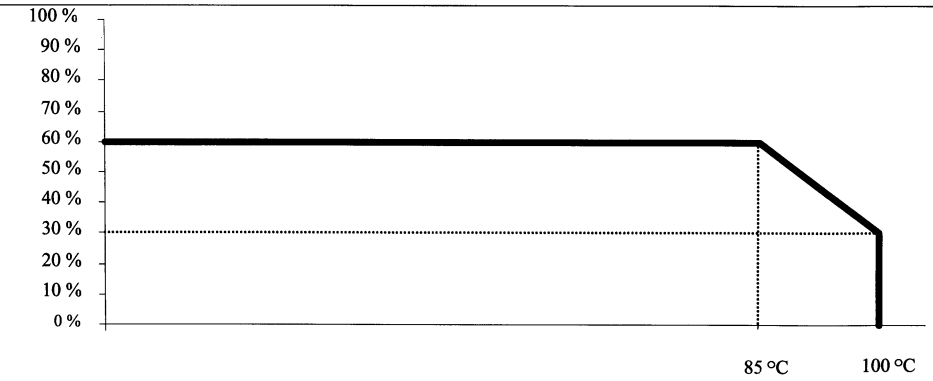
Parameters	Load ratio or limit
Voltage: voltage includes DC voltage and superimposed AC peak voltage.	

2.7 7.7 Capacitors: mica and reconstituted mica, family group code: 01-07

7.7.1 General

Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.7.2 Derating

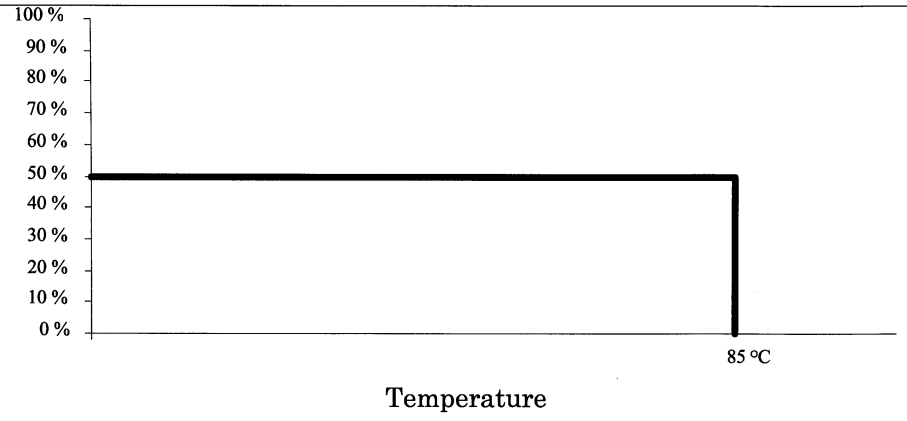
Parameters	Load ratio or limit
Voltage	

2.8 7.8 Capacitors: aluminium solid, family group code: 01-09

7.8.1 General

Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.8.2 Derating

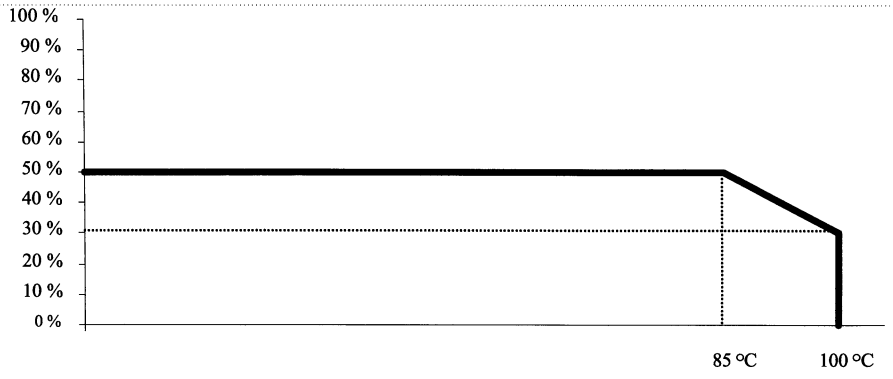
Parameters	Load ratio or limit
Voltage	

2.9 7.9 Capacitors: feedthrough, family group code: 01-10

7.9.1 General

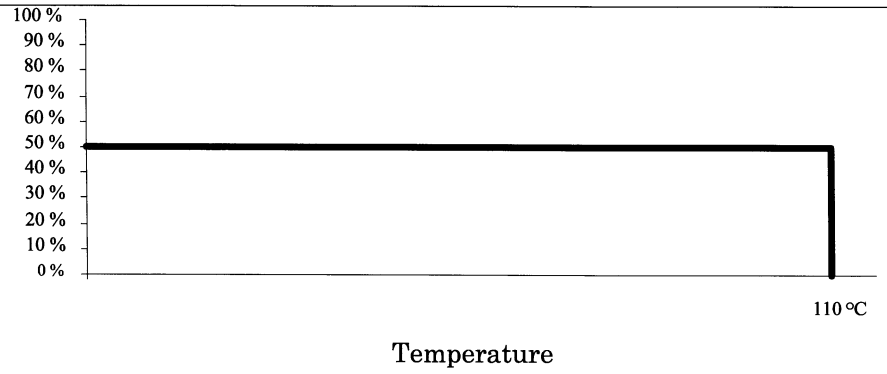
Internal heating due to ESR can increase ageing and shall be taken into account for derating purposes. Where the ESR is not known at the frequency of ripple current, an extrapolation of the ESR value at resonance (from manufacturer's data) shall be made. Where this is not possible, suitable margins on temperature shall be taken and justified.

7.9.2 Derating

Parameters	Load ratio or limit
Voltage	

2.10 7.10 Capacitors: semiconductor technology (MOS type), family group code: 01-11

7.10.1 Derating

Parameters	Load ratio or limit
Voltage	

2.11 7.14 Diodes, family group codes: 04-01, 04-02, 04-03, 04-04, 04–05, 04–08, 04–10 to 04–13, 04-14 and 04–15

7.14.1 General

Some diodes can be radiation sensitive: the issue shall be recorded in the design file and the components selection shall be reviewed and approved as described in ECSS-Q-60

7.14.2 Derating

Parameters	**Load ratio or limit**		
	Signal, switching, rectifier, transient suppression and varactor diodes	**Schottky, step recovery diodes**	**Zener, reference diodes**
Forward surge current (I_{FSM}): non–repetitive operation	80 %	80 %	--
Forward current (I_F): repetitive and continuous operation	60%	60%	--
Zener surge current (I_{ZSM}): non–repetitive operation	--	--	80 %
Zener current (I_Z): repetitive and continuous operation	--	--	60 %
Reverse voltage (V_R)	75 %		--
Dissipated power (P_D)	50 %		65 %
Junction temperature (T_j)	110 °C or $T_{j\,max}$ - 40 °C (whichever is lower).		

2.12 7.15 Diodes: RF, family group code: 04-05, 04-06, 04-15, 04-16 and 04-17

7.15.1 General

Some diodes can be radiation sensitive: the issue shall be recorded in the design file and the components selection shall be reviewed and approved as described in ECSS-Q-60

7.15.2 Derating

Parameters	**Load ratio or limit**
Reverse voltage (V_R)	75 %
Forward surge current	50 %
Dissipated power (P_D)	65 % or maximum derated junction temperature as below
Junction temperature (T_j)	110 °C or $T_{j\,max}$ - 40 °C (whichever is lower)

2.13 7.18 Inductors and transformers, family group codes: 07-01 – 07-03

7.18.1 General

For custom–made inductors and transformers, the maximum rated temperature shall be evaluated taking into consideration the temperature characteristics of the materials used.

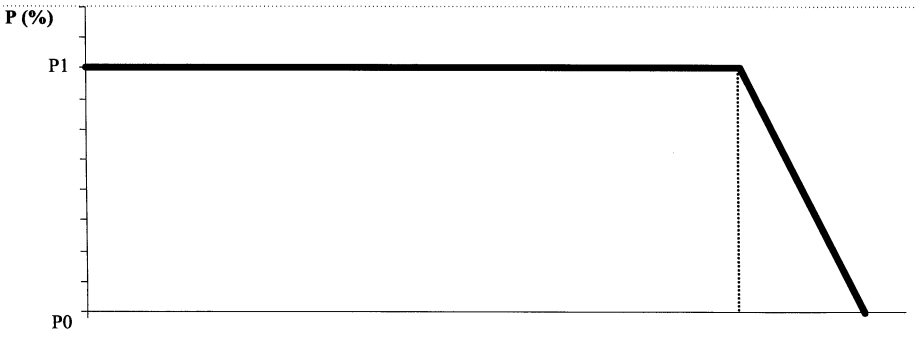
7.18.2 Derating

Parameters	Load ratio or limit
Maximum operating voltage (1)	50 % of the applied insulation test voltage (2)
Hot spot temperature	20 °C below maximum rated temperature

(1) Between winding-winding and between windings-case. The maximum operating voltage shall include DC, AC peak or combined.
(2) Minimum insulation test voltage applied shall be 500 V. For operating voltages greater than 200V the insulation test voltage is equal to the partial discharge voltage (VPD), defined as the component qualification test level, where the partial discharge activity is detected, and with a test equipment sensitivity of no less than 1 pC.

2.14 7.26 Resistors, family group codes: 10-01 to 10-11

7.26.1 Derating (all resistors except heaters)

<table>
<tr><th>Parameters</th><th>Load ratio or limit</th></tr>
<tr><td>Voltage</td><td>80 %</td></tr>
<tr><td>Power</td><td>


<table>
<tr><th rowspan="2">Type</th><th colspan="2">P_1 @ T_1</th><th colspan="2">P_0 @ T_2</th></tr>
<tr><th>(%)</th><th>(°C)</th><th>(%)</th><th>(°C)</th></tr>
<tr><td>Metal film precision (type RNC except RNC90)</td><td>50</td><td>125</td><td>0</td><td>150</td></tr>
<tr><td>Metal film semi–precision (type RLR)</td><td>50</td><td>70</td><td>0</td><td>125</td></tr>
<tr><td>Foil (type RNC90)</td><td>50</td><td>70</td><td>0</td><td>125</td></tr>
<tr><td>Wire–wound high precision (type RBR 56), tolerance 1%</td><td>50</td><td>115</td><td>0</td><td>130</td></tr>
<tr><td>Wire–wound high precision (type RBR 56), tolerance 0,5%</td><td>35</td><td>115</td><td>0</td><td>130</td></tr>
<tr><td>Wire–wound high precision (type RBR 56), tolerance 0,1%</td><td>25</td><td>115</td><td>0</td><td>130</td></tr>
<tr><td>Wire–wound power (types RWR, RER)</td><td>50</td><td>25</td><td>0</td><td>175</td></tr>
<tr><td>Film or foil chips</td><td>50</td><td>70</td><td>0</td><td>112,5</td></tr>
<tr><td>Film network</td><td>50</td><td>70</td><td>0</td><td>112,5</td></tr>
</table>
P_1 and P_0 relative to P_{max};
</td></tr>
<tr><td>Pulse power rating — repetitive/periodic pulses</td><td>$$P_{average} = \frac{V_p^2}{R} \cdot \frac{t_p}{T}$$
Where: V_p: pulse amplitude; R: resistance; t_p: pulse width; T: cycle duration
Average power < 50 % of rating at corresponding temperature</td></tr>
</table>

7.26.1 Derating (all resistors except heaters) (Continued)

Pulse power rating — single pulses	Single pulse power derating is strongly dependant on the resistor type, its power rating, pulse duration and temperature. Single pulse power derating shall be applied as defined in the component detail specification. If the component detail specification does not contain this derating information the pulse power rating provided in the manufacturer's data sheet shall be derated by 50%. Otherwise steady state derating shall apply or alternatively the user shall evaluate the device in accordance with the specific application to determine the appropriate rating.

7.26.2 Derating for heaters

Parameters	**Load ratio or limit**
Power density with respect to heating area (W/cm^2)	50 %

2.15 7.27 Thermistors, family group codes: 11-01 to 11-03

7.27.1 Derating

Parameters	Load ratio or limit
Power	50 % of the maximum power (1)
Voltage	The voltage drop between the thermistor and its base plate shall not exceed 50% of the dielectric withstanding voltage for the device.
(1) For positive temperature coefficient (PTC) and negative temperature coefficient (NTC) thermistors.	

2.16 7.28 Transistors: bipolar, family group codes: 12-01 to 12-04 and 12–09

7.28.1 General

Some transistors can be radiation sensitive: the issue shall be recorded in the design file and the components selection shall be reviewed and approved as described in ECSS-Q-60

7.28.2 Derating

Parameters	**Load ratio or limit**
Collector–emitter voltage (V_{CE0})	75 %
Collector–base voltage (V_{CB0})	75 %
Emitter–base voltage (V_{EB0})	75 %
Collector current (I_C max)	75 %
Base current (I_B max)	75 %
Safe Operating Area (1) D $I_{C\ max}$ DC D $I_{C\ max}$ pulsed	 65 % of manufacturer's SOA curve. 65 % of manufacturer's SOA curve.
Junction temperature (T_j)	110 °C or $T_{j\ max}$ - 40 °C (whichever is lower).
(1) For power cycling application: • $DT_j < 50$ °C • D $T_j < 30$ °C	 50 000 cycles. 100 000 cycles.

2.17 7.29 Transistors: FET, family group codes: 12-05 and 12-06

7.29.2 Derating

Parameters	Load ratio or limit
V_{DS}	40 % (2)
V_{GS}	75 % (1)
I_{DS}	75 %
P_{diss} (max)	60 %
Junction temperature	110 °C (3)
Worst case analysis (Drift to be considered)	
Leakage currents	5 times the specified maximum.
Breakdown voltages	5 % decrease of the specified minimum.
Currents and voltages shall be maintained at levels compatible with the safe operating area.	

(1) Heavy Ion induced Single Event Gate Rupture (SEGR) probability is increased if transistors are operated in blocked mode : V_{GS}(off) < 0V for N-channel types and V_{GS} (off) > 0V for P-channel types. Blocked mode shall not be used unless relevant type specific radiation test data show that the device in insensitive for a given mission environment, V_{GS} and V_{DS} value. This SEGR safe V_{DS} test value shall be derated to 80%.

(2) Applicable for devices not tested for their susceptibility to heavy ion induced "burn–out" . For device types with relevant test data for a given mission environment the SEBO safe V_{DS} test voltage level shall be derated to 80 % in consideration of the mission environment.

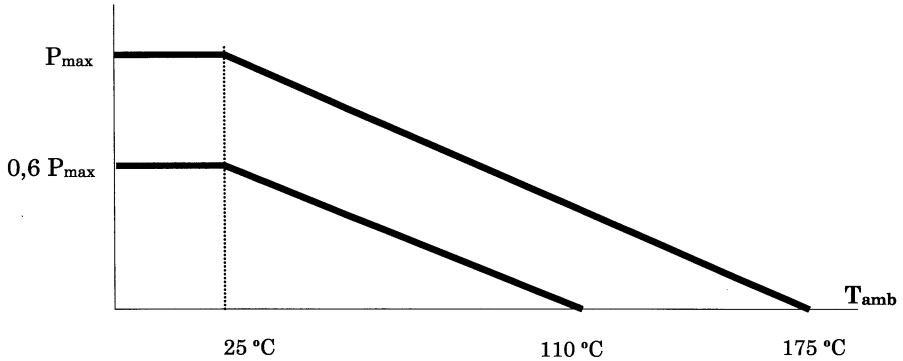
(3) Detailed calculations permitting compliance with these two requirements are given below.

The power derating curves and formula below are based on a maximum T_j capability of 175 °C demonstrated during qualification and lot acceptance testing. For types where testing is conducted at lover T_j, the power allowed shall be reduced accordingly to preserve the same 65 °C margin between T_j operating and T_j qualification.

For small signal transistor operating without heat sink (measurement of $T_{case\ is}$ impractical), the following rule of thumb is applicable, where T_{amb} is the temperature of the mounting board:

where: $T_{amb} > 25$ °C $\quad P_{derated}=0.6 \times \frac{110-T_{amb}}{85} \times P_{max}$

where: T_{amb} @ 25 °C $\quad P_{derated}=0.6P_{max}$



Without heat sink

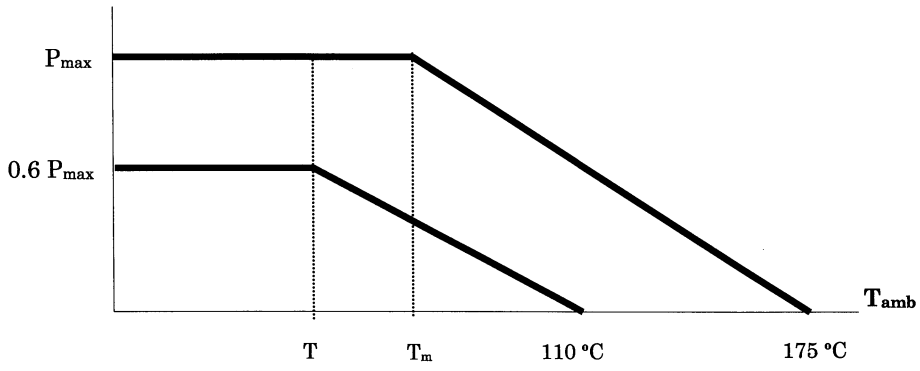
7.29.2 Derating (Cont.)

For transistors operating with heat sink:

If T_{case} @ 110 °C – 0.6 × (175 - T_m) °C $\quad P_{derated}=0.6P_{max}$

If T_{case} > 110 °C – 0.6 × (175 - T_m) °C $\quad P_{derated}=\frac{110-T_{case}}{175-T_m}$

Where Tm = max. specified case temperature at rated power



With heat sink: T= 110 °C – 0.6 (175 - T_m) °C

2.17 7.33 Opto–electronics, family group codes: 18-01 to 18-05

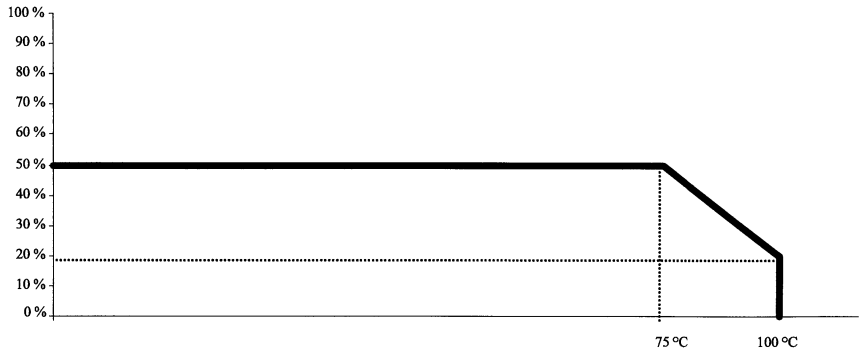
7.33.1 General

a. Light emitting diodes can be radiation sensitive, in particular, there is a high sensitivity to displacement damage: this issue shall be recorded in the design file and the components selection shall be reviewed and approved as described in ECSS-Q-60.

b. Opto–couplers can be radiation sensitive, in particular, operation at low diode currents increases radiation sensitivity: this issue shall be recorded in the design file and the components selection shall be reviewed and approved as described in ECSS-Q-60.

c. Photo–transistors can be radiation sensitive: the issue shall be recorded in the design file and the components selection shall be reviewed and approved as described in ECSS-Q-60.

7.33.2 Derating

Parameters	Load ratio or limit
Light emitting diodes and opto–couplers Power	
Photo–transistors and opto–couplers	
• V_{ceo}	75 %
• $V_{R\ (Diode)}$	75 %
• $I_{c\ max}$	80 %
• Junction temperature	110 °C or $T_{j\ max}$ – 40 °C (whichever is lower).

7.33.3 End–of–life drifts

End-of-Life drifts provided in ECSS-Q-60-11A shall not be used. Mission specific aging and drift effects shall be evaluated on the basis of the mission environment / application conditions and manufacturer data.