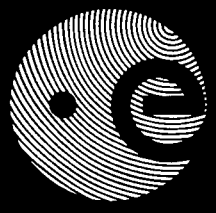
ESA PSS-01-608 Issue 2
April 1987



european space agency
agence spatiale européenne

Generic specification for hybrid microcircuits

Prepared by:
Product Assurance & Safety Department
European Space Research and Technology Centre
Noordwijk, The Netherlands

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ABSTRACT

This specification defines the general requirements for circuit-type approval, procurement, lot-acceptance testing and delivery of thick- and thin-film hybrid microcircuits suitable for space application. It shall be used in conjunction with the detail specification applicable to the actual circuit type and is valid only for procurement from manufacturers whose capability has been approved by ESA in accordance with specifications ESA PSS-01-605 or ESA PSS-01-606.

Status	Document Change Summary
Issue 1 July 1983	First release
Issue 2 April 1987	Completely revised issue: - to revise added-on component testing - to change lot acceptance procedure - to change related documents into applicable documents and therefore reduce the number of documents quoted. - to change circuit type approval procedure.

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1. SCOPE

This specification defines the general requirements for circuit-type approval, procurement, lot-acceptance testing and delivery of thick- and thin-film hybrid microcircuits suitable for space application. It shall be used in conjunction with the detail specification applicable to the actual circuit type and is valid only for procurement from manufacturers whose capability has been approved by ESA in accordance with specification ESA PSS-01-606 for thick-film and ESA PSS-01-605 for thin-film hybrids.

2. GENERAL

2.1 INTRODUCTION

2.1.1 Quality/Reliability Programme

The manufacturer shall have and implement a quality/reliability programme compatible with this specification and any of its related specifications listed in the purchase order or contract. The review of this programme by ESA is part of the capability approval.

2.1.2 Responsibility

The manufacturer shall be responsible for the performance of tests and inspections required by this specification. All these tests and inspections shall be performed at the plant of the manufacturer. The use of external facilities or services has to be approved by the orderer/ESA prior to the event.

2.1.3 Monitoring

The orderer/ESA reserves the right to participate in or execute reviews, source inspection, test observation etc., or have resident or itinerant personnel at the plant(s) of the manufacturer.

The participation of the orderer/ESA shall not in any way replace or relieve the manufacturer of his responsibility.

The manufacturer shall make arrangements to permit designated orderer and/or ESA personnel free access to that documentation/hardware and to those areas indicated in the Product Identification Document (PID) as inspection items and mentioned in the contract.

2.1.4 Pre-cap Visual Inspection

The manufacturer shall notify the orderer/ESA at least two working weeks before the date planned for the pre-encapsulation inspection for self-assembled added-on and hybrid components.

The orderer/ESA shall respond to the notification within one week.

2.2 APPLICABLE DOCUMENTS

The following documents are applicable to the extent specified herein:

ESA PSS-01-20	Quality Assurance of ESA Spacecraft and Associated Equipment
ESA PSS-01-30	Reliability Assurance of ESA Spacecraft and Associated Equipment
ESA PSS-01-60	Components Selection, Procurement and Control for ESA Spacecraft and Associated Equipment
ESA PSS-01-301	Derating Requirements and Application Rules for Electronic Components
ESA PSS-01-605	The Capability Approval Programme for Thin Film Hybrid Microcircuits
ESA PSS-01-606	The Capability Approval Programme for Hermetic Thick Film Hybrid Microcircuit
ESA PSS-01-722	The Control of Limited-Life Materials
ESA-SCC	Specification System
ESA-SCC No. 21400	SEM Inspection
ESA-SCC No. 22800	ESA/SCC Non-Conformance Control System
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-750	Test Methods for Semiconductor Devices

2.3 DEFINITIONS

The Definitions listed in Annex A shall apply.

3. REQUIREMENTS

3.1 GENERAL

Hybrids are components and their selection requirements are called up in document ESA PSS-01-60. Before hybrids are procured, the manufacturer's production line capability shall be approved in accordance with ESA PSS-01-606 or ESA PSS-01-605. The same documents define the rules for maintenance, suspension and withdrawal of capability approval status.

The requirements for the approval of a particular circuit type are specified in Section 3.2 of this specification.

The test requirement for procurement of hybrid circuits so approved shall comprise **Final Production Tests** (Chart II), **Burn-in** and **Electrical Measurements** to testing level 'B' or 'C', as required (Chart III), and **Lot Acceptance Tests** .

Chart I represents schematically the procurement of hybrid microcircuits.

3.2 CIRCUIT TYPE APPROVAL

3.2.1 Definition

A hybrid circuit is considered type approved when all of the following requirements are successfully fulfilled:

(a) The sequence of activities as specified in Para 3.2.3 herein is performed.

(b) It is produced on a manufacturing line with a valid capability approval status.

(c) It is manufactured with the processes and materials listed in the PID that have been extensively tested by means of test structures or other means. In the case of a circuit type already approved, any change made to the PID after initial circuit type approval has been assessed and is considered not to affect the actual circuit design.

(d) The added-on components of the circuit meet the requirements of specification ESA PSS-01-60 and of Para 3.3.4 herein.

3.2.2 QPL Listing

A hybrid circuit type shall be listed in a QPL when the approval activities described hereafter are carried out by ESA and the relevant Detail Specification, written according the Annex B of this specification, is approved by ESA. If the circuit type is project specific and no QPL listing is envisaged, the writing of detail specifications and other activities are to be monitored and approved by the orderer.

3.2.3 Sequence of Activities

(a) **Design Activities**

- Selection of added-on components according to ESA PSS-01-60
- Application of Derating Requirements of ESA PSS-01-301
- Worst case analysis
- Implementation of design rules in the lay-out
- Implementation of thermal management criteria, as applicable
- Verification of radiation resistance on component parts, as applicable
- Performance of reliability calculations

(b) **Fabrication of Hybrid Circuit Prototypes**

The purpose of these prototypes is equivalent to that of an Engineering Model of Electronic Space Hardware. The technology of the circuit shall be the same as listed in the PID and the quality of the component parts and manufacturing shall be consistent with the testing performed hereafter. Chip components on these prototypes are not required to be HiRel.

(c) **Testing of Prototypes**

The testing to be performed on the prototypes shall be tailored to verify potential circuit-related problems and include:

- Verification of worst case electrical and extreme temperature conditions.

  The extreme temperatures shall be those at which electrical measurements are performed during screening, i.e. -55°C and +125°C.

- Thermographic test as applicable

- Verification of radiation resistance on hybrid, as applicable

- Any other test related to the particular application

(d) **Fabrication of Hi-Rel Lot according to PID**

The lot of hybrid microcircuits of the actual circuit type shall be manufactured according to the PID and screened to the highest level (Level B) of this specification. See Charts II and III of this specification.

(e) **Lot Acceptance Testing**

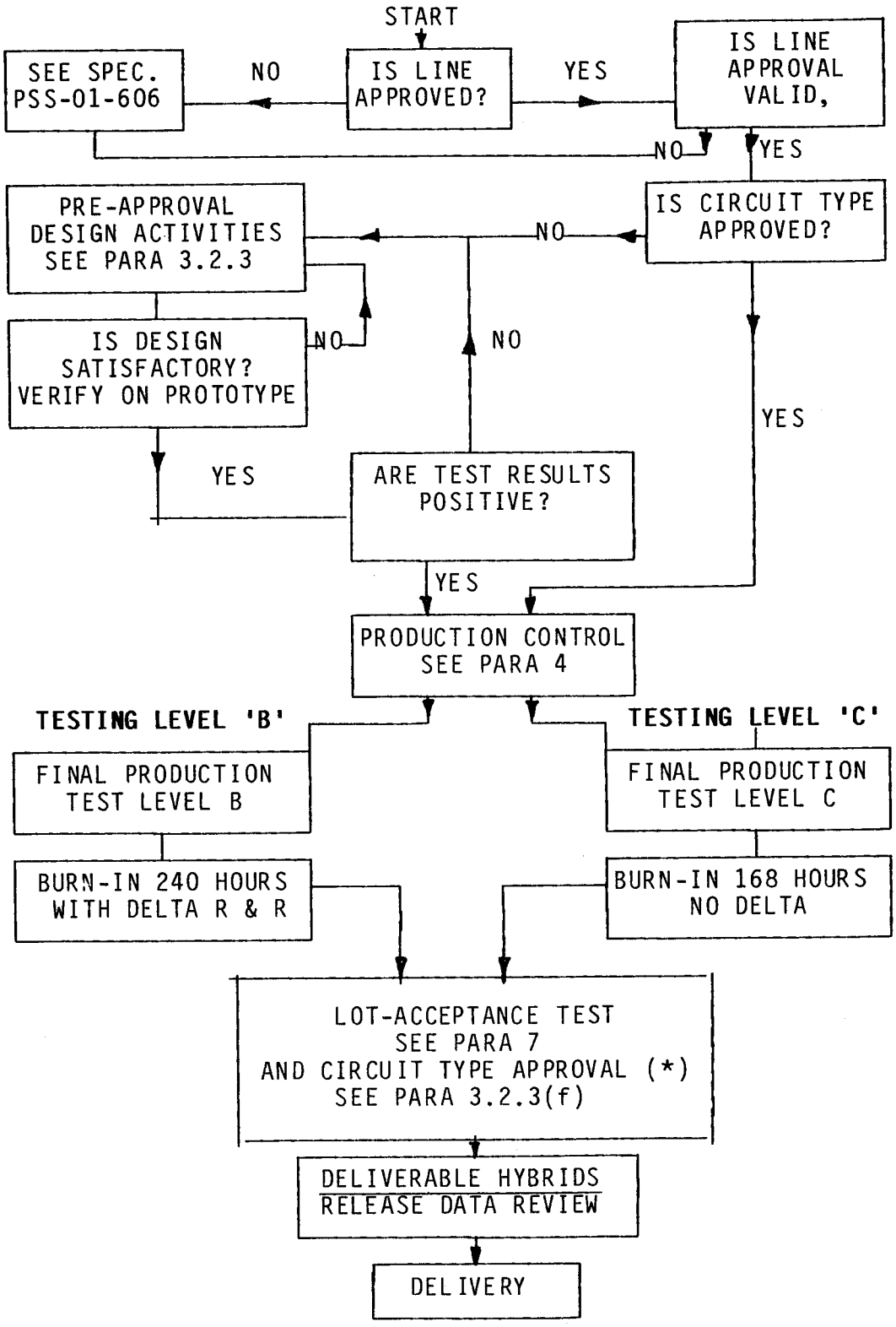
Lot Acceptance Testing has, in this case, also the function of circuit type acceptance and consists of Operational Life Test and DPA as described in Para 7 of this specification except that the time duration of the Operational Life Test shall be 2000 hours and the sample size for this test shall be as a minimum 4 pieces.

(f) **Circuit Type Approval**

Upon successful completion of the Lot Acceptance Testing as described above, the orderer (in the case of no QPL listing) or ESA (in the case of QPL Listing) will grant Circuit Type Approval. This approval shall be valid as long as Line Approval is valid and shall be invoked for subsequent procurements.

CHART I

HYBRID CIRCUIT APPROVAL AND PROCUREMENT SCHEMATIC



(*) **NOTE** : Circuit Type Approval is performed together with Lot Acceptance Testing in the case the circuit type was not previously approved.

3.3 HYBRID PROCUREMENT

3.3.1 General

Hybrids delivered to this specification shall be processed and inspected in accordance with the relevant Process Identification Document (PID).

Each delivered hybrid shall be traceable to its production lot.

Components delivered to this specification shall have completed satisfactorily all tests to the testing level required in the purchase order and shall have passed the lot acceptance procedure. (See Para. 3.3.3).

3.3.2 Lot Failure

Lot failure may occur during final production tests (Chart II), burn-in and electrical measurements (Chart III), or lot-acceptance testing (Chart IV).

Should such failure occur, the manufacturer shall notify the orderer by telex within two working days, giving details of the number and mode of failure and the suspected cause.

In the case of circuit-type approval or if circuit-type has previously been granted to the hybrid-type, the manufacturer shall, at the same time and by the same means, inform the Agency for consideration of its implications. No further testing shall be performed on the failed components except on instructions from the orderer. The orderer will inform the manufacturer and the Agency what action is to be taken.

3.3.3 Testing and Lot-Acceptance

This specification defines two levels of testing severity designated by the letters "B" and "C" (see Chart I) and the lot-acceptance testing (see Chart IV). The required testing level

shall be specified in the purchase order. Each delivery lot shall have passed the lot-acceptance procedure.

3.3.4 Added-On Components

3.3.4.1 **General.** All add-on components shall be selected, procured and controlled in compliance with ESA PSS-01-60 and the complementary requirements for chip acceptance as outlined herein.

Each type of add-on component shall be controlled via an individual procurement specification, which in the case of an encapsulated device shall be an ESA/SCC detail specification, and in the case of a chip, a user specification based on the ESA/SCC detail specification for the packaged version. The testing level (B or C) of encapsulated devices shall be the same as the testing level of the hybrid concerned.

3.3.4.2. **Active Components**

3.3.4.2.1 **General.** Active components to be added on to a film conductor/resistor network may belong to one of the three following main categories:

(a) **Hermetically encapsulated.** These components can be fully characterised and tested before being mounted on the film network. Screening and burn-in can be accomplished. These hermetically encapsulated components to be used on hybrids shall be procured in accordance with ESA PSS-01-60, or assembled by the hybrid manufacturer with provisions for full testability and screened according to a procedure to be agreed with ESA during capability approval and described in the PID.

(b) **Not hermetically encapsulated,** i.e. naked chips, mounted on open carriers. These components permit limited electrical testing beforehand. The risk of handling damage is, however, incurred. Screening and burn-in are possible, but difficult.

Not hermetically encapsulated components mounted on open carriers shall be procured and tested according to a procedure to be agreed with ESA during the capability approval of the hybrid line. This procedure shall be described in the PID.

(c) **Naked semiconductor chips** that are attached directly to the substrate permit only very limited testing before assembly. Electrical characterisation at temperature extremes, dynamic measurements and burn-in may not be possible on 100% basis before assembly.

3.3.4.2.2 **Chip-lot-acceptance programme - Active components.** Naked semiconductor chips of type (c) above, which do not allow 100% testing, shall be submitted to a chip-lot-acceptance procedure which shall contain as a minimum the following elements :

- Wafer acceptance tests including radiation resistivity (when applicable)
- Electrical and life tests on an assembled and packaged sample
- Bondability test on sample basis.
- Radiation resistance tests as applicable.

(a) The **wafer acceptance tests** consist of:

1. **Lot Identification.** The lot shall be composed of wafers diffused and metallised at the same time.

2. **Optional, wafer-lot acceptance.** Depending on chip type and technology, the wafers shall be submitted to MIL-STD-883 Method 5007 or MIL-STD-750 Method 5001 test.

The necessity of performing this test shall be determined, case by case, by the orderer.

3. **SEM Inspection** (if not already performed in ref. 2 above). Each wafer lot of monolithic integrated circuits shall be subjected to SEM inspection in accordance with ESA/SCC specification No. 21400.

4. **Stabilisation Bake.** To be carried out on a 100% basis according to MIL-STD-883 Method 1008, Condition D - 24 hours.

5. **Wafer Probe.** To be carried out on a 100% basis testing DC and functional parameters at ambient temperature.

6. **Visual Inspection.** After scribing, the chips shall be submitted to 100% visual inspection according to Method 2010 of MIL-STD-883 or Method 2072 of MIL-STD-750, test conditions A, as applicable.

(b) The **electrical and life tests** on an assembled and packaged sample from the chip lot shall be carried out either at the semiconductor chip manufacturer's premises or at the hybrid manufacturer's facilities.
For a unique lot of less than 100 chips a sample of 32 chips shall be assembled in a suitable hermetic package for further testing. For a unique lot of more than 100 chips a sample of 38 chips shall be used. The testing on the sample shall be as follows :

1. **Serialisation of all pieces**

2. **Electrical measurement** at ambient temperature and temperature extremes (-55°C, +125°C) with limits as per ESA SCC detail specifications (Tables 2 and 3) of the applicable device type. Requirement: 1 reject maximum allowed.

3. **Read and record** of burn-in parameters as per ESA SCC Table 4 of device type detail specification.

4. **Burn-in** for 240 hours as per conditions of device type detail specification.

5. **Electrical Measurements** at ambient temperature and parameter drift calculation, (ESA SCC Tables 2 and 4). Requirement: 2 rejects maximum allowed.

6. **Life test** on remaining pieces, conditions as per ESA SCC detail specification. Duration 1000 hours. Followed by electrical measurements as per Table 6 of ESA/SCC detail specification. Requirement : 1 reject maximum allowed.

(c) **Bondability Test.** If the samples are mounted and electrical tests are performed by the semiconductor chip manufacturer, the following additional tests shall be carried out by the hybrid manufacturer.
The processes, materials and machine settings used for mounting the chips shall be as defined in the PID. The sample shall simulate the same environment as the actual hybrid.
The sample shall be of 20 pieces and shall be submitted to the following tests:

1. **Electrical measurements** as per Table 2 of ESA SCC detail specification

2. **Life test,** 1000 hours at 125°C

3. **Electrical measurements** as per Table 6 of ESA/SCC detail specification. One failure allowed on the 20 pieces.

4. **Wire Bond Pull** according to MIL-STD-883, Method 2011. on a minimum of 22 wires (or all the wires if less).
No failures allowed.

5. **Shear Test** according to MIL-STD-883, Method 2019. on a minimum of 4 chips. No failures allowed.

If the electrical and life tests listed in (b) above are performed at the hybrid manufacturuer premises, the sample shall be mounted and wired with the same processes, materials and machine settings as defined in the PID. This sample shall simulate the same environment as the actual hybrid.
The following bondability test shall be carried out on the samples which have passed the life test:

1.Wire Bond Pull according to MIL-STD-883 Method 2011 on a minimum of 40 wires (or all the wires if less)

2.Shear Test according to MIL-STD-883 Method 2019 on a minimum of 4 chips.

No failures on any of the above-mentioned tests are allowed.

(d) The **radiation resistance tests** shall be carried out if the application envisaged requires it. The tests, sample size, and accept/reject criteria shall be agreed on between the hybrid manufacturer and the orderer.

3.3.4.3 **Passive Components**

3.3.4.3.1 **General.** Passive Components shall be selected, whenever possible, in a way that permits the full screening sequence as outlined in the ESA/SCC specification system. For all passive add-on components, where only reduced individual screening (burn-in, ageing) can be performed, the minimum chip testing and chip lot-acceptance programme as described below shall be conducted.

3.3.4.3.2 **Chip-lot-acceptance programme - Passive components.** This programme may be performed at either the hybrid manufacturer's plant or the chip manufacturer's facilities. The programme consists of:

(a) **100% chip testing** Each chip shall be visually inspected and electrically tested (25°C) as specified in the detail specification.

(b) **Chip lot acceptance** From each lot of passive chips having passed the 100% chip testing of (a) above, a randomly selected sample of 20 devices shall be assembled into suitable packages that simulates the assembly methods and functional conditions of the chip within the intended application.
The assembled devices shall be submitted to the following tests :

(1) Stabilisation bake according to MIL-STD-883 Method 1008 Cond. C
(2) Temperature cycling according to MIL-STD-883 Method 1010 Cond. C
(3) Voltage conditioning (or ageing) for 1000 hrs. at 125°C (condition to be specified in the detail specification)
(4) Electrical measurements as outlined in the detail specification
(5) Visual inspection
(6) Shear test and bond strength test (in the case of wire bonding). This test shall be performed by the hybrid manufacturer. Minimum sample 4 passive chips for shear test, 40 wires for bond strength test.

For lot acceptance one failure is allowed for the total sequence.

3.3.5 Marking

Marking shall be on the body of the hybrid. Apart from serialisation, all marking shall be clearly visible when normal mounting procedures are followed. If a hybrid is too small to accommodate all marking, the device shall show as a minimum the polarity or lead identification and as much as possible of the marking required in the prescribed order of precedence. Any marking that cannot be accommodated on the cases themselves shall be shown on the individual containers, excluding the serial numbers which shall be shown on a tag attached to one of the leads.

Marking shall remain legible after all tests specified herein have been performed and shall withstand all solvents used in accordance with MIL-STD-883 Method 2015.

Each hybrid shall be marked with the following information and in the order of precedence shown below:

(a) **Polarity or lead identification** according to the detail specification.

(b) **Part number** in accordance with the detail specification, followed by the suffix B or C, according to the testing level.

(c) **Manufacturing date code.** A 4-digit code shall be used, the first two digits of which shall be the last two digits of the calendar year. The last two digits of the code shall identify the number of the week in which the hybrid was encapsulated. If more than one production lot of hybrids are encapsulated in a week, a suffix letter shall be added to the date code for each lot, starting from the letter "A" for the first lot. This suffix will not be required if the lot number is included separately (see 'f').

(d) **Serial Number.** This number shall be required only for testing level B, and shall consist of a sequential number of two or more digits for each selected sublot. Serial numbers shall not be duplicated when more than one selected sublot has been taken from one production lot.

(e) **Manufacturer's name, symbol or trade mark.**

(f) **Production lot number.** This is optional.

IMPORTANT NOTE:

(a) If a hybrid microcircuit contains beryllium oxide substrate or carriers, it shall be marked with the notation: **"Contains BeO".** In the case of insufficient space on the package, indicate only **"BeO".**

(b) If a hybrid microcircuit is sensitive to electrostatic discharge, a warning shall be given on the package **"ESD sensitive".**

4. PRODUCTION CONTROL

Production shall follow the process identification document (PID), and production control/inspections shall be coordinated with the manufacturing operations/specification. The quality assurance requirements are defined in ESA PSS-01-20. However as a minimum the following requirements shall apply:

4.1 PROCESS IDENTIFICATION DOCUMENT (PID)

The PID prepared for the capability approval shall describe those steps and internal specifications/procedures which the manufacturer undertakes to employ in order to meet the requirements set forth in this and the detail procurement specification. The content of the PID as well as its use is described in ESA PSS-01-605 or ESA PSS-01-606, as applicable.

4.2 RAW MATERIAL AND SEMI-FINISHED PRODUCT CONTROL

Raw materials and semi-finished products shall be selected, inspected and tested (e.g. chemical and physical tests) in accordance with the PID. The manufacturer shall separate, and prevent the use of, raw materials and semi-finished products that are awaiting completion of test results.

4.3 TRACEABILITY

Traceability shall be maintained throughout the process from incoming inspection to final test as described in the PID.

The manufacturer's control system shall make it possible to determine, in respect of any production lot of hybrids, the history of all raw materials and semi-finished products listed in

the production flow chart and the individual process steps mentioned herein, and verify that the items originate from one production lot (see also definitions).

In the case of materials with limited shelf life, the manufacturer's control system shall provide for means to verify the validity of the relevant material for use. The verification and re-certification procedure shall be listed in the PID and be in compliance with ESA PSS-01-722.

4.4 SPECIAL IN-PROCESS CONTROLS

Where relevant, special in-process controls shall apply, as specified in the PID.

4.5 NONCONFORMANCE

Any nonconformance which is observed in respect of the process or test shall be dispositioned in accordance with the quality assurance requirements of ESA/SCC 22800.

4.6 CALIBRATION

Each standard and piece of measuring equipment shall be calibrated. Any suspected or actual equipment failure must be notified so that previous results may be examined to ascertain whether or not re-inspection/re-testing is needed (see also ESA PSS-01-20).

5. FINAL PRODUCTION TESTS

5.1 GENERAL

5.1.1 Hermetically Encapsulated Hybrids

Final production tests shall meet, as a minimum, the requirements of Chart II. The sequence of all tests shall be as shown, unless the manufacturer has formally requested and obtained permission from the orderer to deviate from this sequence. All components for delivery and all components used for environmental and endurance tests shall meet all of the relevant final production test requirements. Any component that does not meet those requirements shall be removed from the lot and at no time be resubmitted to the requirements of this specification.

5.1.2 Un-encapsulated Hybrids

Final production tests and procurement requirements for open substrates (ordered for assembly as part of a subsystem or for encapsulation at a location other than the hybrid circuit manufacturer's plant) will be defined case by case according to the provisions of the PID.

5.2 TEST METHODS AND CONDITIONS

The applicable test methods and conditions are specified in Chart II.

5.3 DOCUMENTATION

Documentation of **Final Production Test Data** shall be in accordance with the requirements of Chapter 8 of this specification.

CHART II - FINAL PRODUCTION TESTS

PRODUCTION AND CONTROLS IN ACCORDANCE WITH PARA 4 OF THIS SPECIFICATION

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FINAL PRODUCTION STEP EXCEPT ENCAPSULATION

↓

Test No.	Inspection and Screening Test	Specification & Test Method	Test Condition	Sample size	Testing Levels B	Testing Levels C
1	Thermographic Test	See Note 1		1piece	x	
2	Non-Destructive Bond Pull Optional	MIL-STD-883 Method 2023		100%	x	
3	Pre-seal Burn-in Optional	See Note 2	See Detail Specification	100%	x	
4	Electrical Test Optional	According to Manufacture Specification		100%	x	x
5	Photograph of Circuit	See Note 3		1piece	x	
6	Pre-cap Visual Inspection	MIL-STD-883 Method 2017 Class S		100%	x	x

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VACUUM BAKE-OUT: ACCORDING TO PID

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CONTINUED

CHART II - (CONT'D)

ENCAPSULATION: ACCORDING TO PID

Test No.	Inspection and Screening Test	Specification & Test Method	Test Condition	Sample size	Testing Levels B	Testing Levels C
7	Stabilisation Bake	MIL-STD-883 Method 1008	Cond. B - 72 hrs (see note 4)	100%	x	x
8	Thermal-Cycling	MIL-STD-883 Method 1010	Cond. B 10 cycles	100%	x	x
9	Mechanical Shock or Constant Acceleration	MIL-STD-883 Method 2002 or 2001	Y1 axis only. (see Note 8)	100%	x	x
10	Particle Impact Noise Detection (PIND)	MIL-STD-883 Method 2020 Specification	Cond. A or B (see Note 7)	100%	x	
11	Fine Leak	MIL-STD-883 Method 1014	Cond. A2 (see Note 5)	100%	x	x
12	Gross Leak	MIL-STD-883 Method 1014	Cond. C1 or C2 (see Note 5)	100%	x	x
13	Electrical Measurements	Detail Spec. Table 2	Ambient Temperature	100%	go / no-go	go / no-go
14	Physical Dimensions	MIL-STD-883 Method 2016		5 pieces	x	x

MARKING AND SERIALISATION: SEE PARA 3.4.5

NOTES:

1. **Thermographic Test** (only applicable to power circuits)
   The purpose of this test is to verify that the circuit is so designed that no hot spots are introduced when it is powered.
   During the test, the circuit shall be operated at rated power. If an infrared microscope is used, lacquer or a thick-film glass cover shall be applied to obtain a uniform emissivity factor from the metallisation surfaces. This test is destructive.

2. **Pre-seal Burn-in**
   Pre-seal burn-in is optional. If performed, the test procedure, the environment and duration shall be approved by the Agency as part of the line qualification activity.
   Pre-seal burn-in shall be performed in an inert atmosphere. The total burn-in time shall not be less than 240 hours and may be divided between pre-seal burn-in and post-seal burn-in, provided the latter lasts 96 hours or more.

3. **Photograph of Circuits**
   For reference purposes, a photograph shall be made of the surface of one open circuit. Magnification shall be such that the layout can be easily identified. The same circuit shall be photographed also at such a magnification that the chip-surface pattern is easily identifiable.

4. **Stabilisation Bake**
   Stabilisation bake may be omitted provided pre-seal burn-in has been performed or vacuum bake-out is extended to 72 hours.

5. **Leak Tests**
Pressurisation and time will depend on package sizes according to MIL-STD-883 Method 1014.
The performance of this test, at this point of the sequence, is left to the manufacturer's discretion.

6. **Radiographic Inspection** may be performed at any point during the test sequence. The performance of this test depends on the technology. In the case of aluminium wires and epoxy bonding of chips, this test can be omitted.

7. **Test Condition for PIND** to be defined by the orderer.

8. **Conditions for Constant Acceleration or Mechanical Shock** are a function of the hybrid package size as follows:

Hybrid Package Size	Constant Acceleration		Mechanical Shock
Up to 1" x 1"	10000 g (Condition B)	or	1500 g - 0.5 ms (Condition B)
From 1" x 1" up to 1" x 2"	5000 g (Condition A)	or	1500 g - 0.5 ms (Condition B)
Above 1" x 2"	Not applicable		1000 g - 0.5 ms

9. **Burn-in test** temperature shall be 125°C ambient. If other temperature is selected, test times shall be adjusted.

6. BURN-IN AND ELECTRICAL MEASUREMENTS

6.1 GENERAL

Burn-in and electrical measurements shall be performed only after final production tests. The applicable tests are shown in Chart III and shall be performed as specified in the PID.

Hybrids of **testing level B,** shall undergo a total burn-in period of 240 hours. The data points for parameter drift measurement shall be 0 hours (initial) and 240^{+24} hours (final).

Hybrid of **testing level C,** shall undergo a total burn-in period of 168 hours. The measurement point for post burn-in electrical measurements shall be 168^{+24} hours.

6.2 FAILURE CRITERIA

6.2.1 General

A hybrid shall be considered as having failed if it exhibits one or more of the failure modes listed in this section.

In the case of lot failure, the manufacturer shall act in accordance with the requirements of Paragraph 3.3.2 of this specification.

6.2.2 Parameter Drift Failure

The acceptable delta limit is shown in Table 4 of the detail specification. A parameter drift failure is a failure when the changes during the 0-hour and 240 hour readings of burn-in, based on the 0-hour reading, are larger than the delta value.

6.2.3 Parameter Limit Failure

A limit failure is a failure when one or more parameters exceed the limits shown in Table 2 or 3 of the detail specification. Any component which exhibits a limit failure prior to the burn-in sequence shall be rejected, but not counted when determining lot rejection.

6.2.4 Other Failures

A hybrid shall be considered as having failed if any of the following cases apply:

- catastrophic failure,
- mechanical failure,
- handling failure,
- lost component,

6.2.5 Lot Rejection

If the number of failed hybrids on the basis of the failure criteria described above (excluding handling failures and lost components) exceeds 20% (rounded upwards to the nearest whole number) of the number of hybrids submitted to burn-in and electrical measurements, the lot shall be considered as failed.

6.3 DOCUMENTATION

Data/documentation of burn-in and electrical measurements shall be in accordance with Chapter 8 of this specification.

CHART III: BURN-IN AND ELECTRICAL MEASUREMENTS

Test No.	Inspection and Screening Test	Specification & Test Method	Test Condition	Sample size	Testing Levels	
					B	C
15	Pre-Burn-in Electrical Measurements	Detail Specification Table 4		100%	Read and Record	
16	Burn-in	Detail Specification	Table 5 See Note 9 of Chart II	100%	240 hrs	168hrs
17	Parameter Drift Measurements	Detail Specification Table 4		100%	Read and Record	
18	Electrical Measurements Ambient Temp.	Detail Specification Table 2		100%	Read and Record	go / no-go
19	Electrical Measurements High and Low Temp.	Detail Specification Table 3		100%	Read and Record	go / no go
20	Radiographic Inspection	MIL-STD-883 Method 2012	See Note 6 of Chart II	100%	x	x
21	Fine Leak	MIL-STD-883 Method 1014	Cond. A2	100%	x	x
22	Gross Leak	MIL-STD-883 Method 1014	Cond.C1 or C2	100%	x	x
23	External Visual Inspection	MIL-STD-883. Method 2009		100%	x	x

7. LOT ACCEPTANCE TESTING

7.1 GENERAL

Lot-acceptance testing applies for procurement of a circuit type on a line which has been capability approved previously. Lot acceptance is performed for hybrids to be used for flight standard hardware.See Chart IV.

Lot-acceptance tests shall be performed on a sample which is a function of the lot size. Lots of similar circuit types produced in the same time frame can be combined provided that at least one sample from each lot is submitted to operating life test.

Lot Size	Lot Acceptance Test Samples "n"
1 to 25	3
26 to 50	4
51 to 90	5
91 to 150	6
151 to 500	9
501 to 3200	14
3201 to 10000	21

7.2 LOT-ACCEPTANCE PROCEDURE

A number "n" (see table above) of circuits is required for lot-acceptance test, which consists of the operating life test, electrical measurements and DPA as defined hereafter.

If lot-acceptance testing is combined with circuit type approval the minimum sample size is (n + 1) hybrids.

The extra hybrid of the circuit-type approval lot shall be kept as reference for electrical measurements and, if necessary, for performing additional tests in order to resolve discrepancies that have arisen in DPA or operating life test.

(a) **Operating Life Test** on n-1 circuits for 1000 hours. The conditions shall be: maximum load and maximum temperature as stated in Table 7 of detail specification. The parameters measured before and after the test shall be those of Table 6 of detail specification. No failures are allowed.

(b) **Electrical Measurements** according to detail specification, Tables 2 and 3. The manufacturer shall inform the orderer before performing these measurements, so that the orderer may decide whether to witness the tests or not.

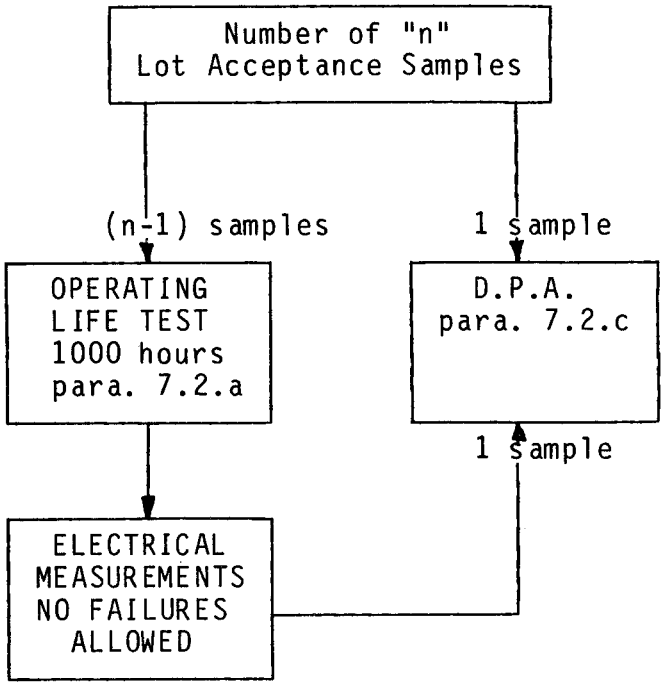
(c) **Destructive Physical Analysis - D.P.A.** This analysis shall be performed on one (1) circuit chosen at random from the fully screened lot and one (1) circuit chosen at random from the samples which have passed the operating life test. D.P.A. shall be performed by the orderer or an independent test laboratory selected by the orderer. For the circuit(s) submitted to DPA the manufacturer shall fill in the **Hybrid Circuit Technology Identification** form shown in Annex C of this specification and enclose a schematic layout with identification of components, wires and other elements important for the DPA.
DPA shall include the following tests performed according to the specified standard methods which include accept/reject criteria. The selection of the tests is greatly dependent on the technology of the hybrid. The orderer and the manufacturer shall agree on these tests during order negotiation, and the sequence together with applicable test methods shall be entered in Table 8 of the detail specification.

Typical tests from MIL-STD-883 are:

- External Visual Inspection: Method 2009
- Radiography: Method 2012
- Seal: Method 1014
- Solderability: Method 2003
- Resistance to Solvents: Method 2015
- Lead Integrity: Method 2004
- Particle Impact Noise Detection: Method 2020
- Internal Visual of hybrid and added-on cavity devices: Method 2017 and 2010
- SEM Inspection: Method 2018
- Bond Strength: Method 2011
- Substrate Attach Strength Method 2027
- Die Shear Strength: Method 2019

- Passive Chips and encapsulated components: Attach Strength. For this test no specified MIL test method is available. Criteria shall be established on the basis of line evaluation and approval test results.

CHART IV - LOT-ACCEPTANCE TESTING



8. DOCUMENTATION

8.1 DATA PACKAGE

A data/documentation package shall be required from the manufacturer for each delivery lot. Each page shall be numbered "x" of "y". The document shall identify:

- part type,
- manufacturer,
- lot,
- date on which document is issued.

The documentation packages shall include, as a minimum, the following items:

- cover sheet(s) as per Section 8.2,
- certificate of compliance as per Section 8.3,
- procurement summary as per Section 8.4, and shall be supplied with each delivery lot.

A copy of each document in the package shall be kept on file by the manufacturer for a period of three years. A copy of the cover sheet shall be sent to the orderer and show, additionally, the number of components delivered to each testing level.

8.2 COVER SHEET(S)

The cover sheet(s) of the data documentation package shall include as a minimum:

- applicable detail specification and relevant date of issue,
- applicable ESA generic specification and relevant date and issue number,
- applicable PID/manufacturing specification and relevant date of issue,
- order number,

- part type number,
- manufacturing date,
- lot identification,
- range of serial numbers,
- manufacturer's name and address,
- location of manufacturing plant,
- (if applicable) indication of modifications of detail and generic specifications,
- date and manufacturer's signature,
- name and address of orderer.

8.3 CERTIFICATE OF COMPLIANCE

This document shall certify that the delivery lot meets the requirements set forth in the applicable specifications indicating date and issue number. It shall be signed by the responsible Quality Assurance Manager and may be combined with the cover sheet(s). If supplied separately, it shall contain, as a minimum, the information specified in Chapter 8 for each page of the documentation.

8.4 PROCUREMENT SUMMARY

The manufacturer shall supply the following items:

- a record of the number of hybrids submitted to, and failed at, each screening test, starting from pre-cap visual inspection;
- a record of all "read and record" parameters of all supplementary screens, together with delta values (percentage and absolute), where required;
- radiographic photographs with reference to the serial numbers (for level B) of all delivered circuits and indicating any failure modes;
- SEM plates where applicable.

- a failed-component list and failure analysis, providing data of failure modes (e.g. drift, functional etc.) and all catastrophic rejects during screening;
- thermographic test results when performed;
- photograph of circuit.
- design activity report(s) according to Para. 3.2.3 with reference to the type approval document.
- Summary of chip lot acceptance results for the chip lots used in the hybrid.

9. DELIVERY

9.1 PACKAGING

The manufacturer shall be responsible for the packaging of devices and use the appropriate methods to prevent degradation, or damage due to electrostatic discharge, corrosion, deterioration or physical damage, and to ensure safe delivery to the orderer. He shall be responsible for any damage resulting from faulty packing and supply unpacking instructions where necessary. Hybrids shall be packaged separately or stacked, but in such a manner that they suffer no change in characteristic, or loss in inherent reliability, during shipment.

9.2 DELIVERY LOTS

Hybrids shipped against the order shall be clearly identified as such. Hybrids used for circuit qualification or lot acceptance tests shall be clearly identified as such and packed separately. Packaging containing these hybrids shall, if possible, identify the tests to which the hybrids have been submitted.
Hybrids that have failed during testing shall be delivered upon request and also packed separately. They shall be clearly identified as failed items and relevant information shall include a failure analysis of each device.

9.3 DELIVERY OF DOCUMENTATION

The documentation defined in Chapter 8 shall be delivered together with each delivery lot.

9.4 LABELS

Attached to the outer container shall be a label with the legend **"HIGH RELIABILITY SPACE COMPONENTS - HANDLE WITH CARE".** This legend shall be written in both the language of the country of origin and the country of destination. Whenever required, it shall be written also in the language of any transit country.

Each shipping container shall be marked with the manufacturer's name, part designation, lot date code and purchase order reference number.

9.5 STORAGE

Excess quantitities of screened hybrids which are produced in accordance with the requirements of the procurement documents shall be held in locked storage to ensure that they do not suffer any damage. In the case of re-use, the procedure for off-the-shelf components described in specification ESA PSS-01-60 shall be followed.

ANNEX A

DEFINITIONS

APPROVED HYBRID CIRCUIT TYPE

A hybrid circuit is considered type approved when all of the following requirements are successfully fulfilled:

a) The sequence of activities as specified in Para 3.2.3 of specification ESA PSS-01-608 is performed.

b) It is produced on a manufacturing line with a valid capability approval status.

c) It is manufactured with materials and processes listed in the PID.

d) The added-on components of the circuit meet the requirements of specification ESA PSS-01-60 and of Para 3.3.4 of ESA PSS-01-608.

CHIP COMPONENT

A component in its ultimate state of miniaturisation.

COMPONENT

A device which performs an electronic, electrical or electro-mechanical function and consists of one or more elements joined together, which normally cannot be disassembled without destruction. The terms component and part may be interchanged. Typical examples of components are transistors, integrated circuits, hybrids, capacitors, etc.

DESTRUCTIVE PHYSICAL ANALYSIS (DPA)

A series of inspections, tests and analyses performed on a sample component to verify that the material, design and workmanship used for its construction, as well as the construction itself, meet the requirements of the relevant specification and are suitable for the intended application.

ANNEX A (CONT'D)

DEVIATION
A written authorisation to accept and item which, during production or after having been submitted for inspection, is found to depart form specific requirements, but is nevertheless considered suitable for "use-as-is" or after "rework" by an approved method.

FILM NETWORK
Layers of conductive, resistive, dielectric, and/or passivating materials deposited onto an insulating substrate for the purpose of performing electronic functions

HYBRID MICROCIRCUIT
A component performing an electronic circuit function which consists of a thick- or thin-film network on a substrate which supports active and/or passive chip components connected to it.

LIMITED-LIFE MATERIAL
A material which can only be processed or stored for a limited period of time before the properties of the material fall outside those specified for the material.

LOT ACCEPTANCE
A series of tests on components which may be:
- only electrical, or
- electrical and endurance, or
- electrical, endurance and environmental

and are performed on a sample selected from the procurement lot to ensure that the production lot concerned meets the defined quality requirements.

ANNEX A (CONT'D)

NONCONFORMANCE

An apparent or proven condition of any item or documentation that does not conform to specified requirements or which could lead to incorrect operation or performance of the item or mission.
The term nonconformance is also used for failure, discrepancy, defect, anomaly, malfunction, deficiency.

PROCESS IDENTIFICATION DOCUMENT (PID)

A document which defines the technology, processes, and relevant inspection procedures applied to the manufacturing of the component or item.

PRODUCTION LOT

A production lot consists of a single device type manufactured on the same production line by the same production techniques according to the same component/part design and with the same raw materials and the same chips lot during one uninterrupted period.

SELECTED SUBLOT

As a production lot may consist of more components than required, part of such lot may be selected for a particular purpose. That part shall be called a selected sublot.

ANNEX A (CONT'D)

SYMBOLS AND ABBREVIATIONS

The symbols and abbreviations defined in MIL-S-19500, MIL-M-38510, MIL-STD-883, Specifications ESA PSS-01-60, ESA PSS-01-606, this specification and the applicable detail specifications shall be applicable.

THICK FILM

A network where the film is deposited by screen-printing methods. The thickness of the fixed film is usually in the range of 10 to 25 micrometres.

THIN FILM

A network where the film is deposited by one or more of the following processes; electrodepositing, plating, evaporation, sputtering, anodisation and polymerisation. Film thickness can be in the range of 50 to 2000 angstroms.

TRACEABILITY

The ability to trace the history, application, use and location of an item through the use of recorded identification numbers.

UNIQUE CHIP LOT

A unique chip lot is defined as a number chips produced during the same diffusion, metallisation and passivation operation.

ANNEX B

REQUIREMENTS FOR DETAIL SPECIFICATIONS

The detail specification of each hybrid circuit type procured against this specification shall contain a "Requirements" paragraph making reference to this specification and the relevant PID and define deviations from them if any, define subtechniques and materials including the types and manufacturers of added-on components, and contain the following information. For standardisation purposes, the information is to be presented as far as possible in accordance with the format used in the ESA/SCC specification system. Table numbering according to this format is summarised as follows:

Table 1	-	**Maximum ratings**
Table 2	-	**Electrical measurements at room temperature - DC and AC parameters** This table shall contain the parameters to be measured, their designated symbols, the test method and/or test circuit, the test conditions, the limits (minimum and maximum, not typical) and the unit of measurement.
Table 3	-	**Electrical measurements at high and low temperatures** Unless otherwise defined, the temperature extremes are assumed to be -55° and +125°C.

Table 4 - **Parameter drift values**
This table shall indicate which parameters are measured before and after burn-in together with maximum drift allowed (positive and/or negative).

Table 5 - **Conditions for burn-in**
This table shall indicate the ambient temperature and applied voltages necessary to ensure that the correct environment is achieved. The table shall be complemented by a circuit schematic defining all details of the test. The ambient test temperature shall be 125°C and the applied voltages shall be chosen so as to ensure that a junction temperature of 150°C is achieved by most semiconductor chips in the circuit, but not exceeded by any of them.

Table 6 - **Electrical measurements on completion of environmental and endurance tests**
These measurements shall be performed upon completion of qualification testing of the line by means of test structures, or after life testing of the actual circuits. Table 6 will be, in most cases, a repetition of Table 2, either wholly or partly. If otherwise required by the circuit being tested, full details of additional or different tests shall be supplied.

Table 7 - **Conditions for operating life test**
This table shall contain the details of the operating life test if different from the burn-in test. If not, Table 5 shall be called up.

Table 8 - **DPA sequence of tests**

The figures in the detail specification shall cover the following points:

- Drawing of package and its dimensions. Minimum and maximum values and/or tolerances in both mm and inches:
- Electrical schematics with component values and/or types:
  - pin assignment;
  - truth table or input/output conditions for functional (if required);
  - block diagram (if required);
- Electrical circuits to be used in the performance of all electrical measurements, burn-in and operating life test.

For a standardised technology description of the hybrid circuit the form in Annex C of this specification **"Hybrid Circuit Technology Identification"** shall be filled in and attached to the detail specification.

ANNEX C

HYBRID CIRCUIT TECHNOLOGY IDENTIFICATION

HYBRID NAME/TYPE NO. :	
Max. Power Dissipation:	
Max. Frequency of Operation :	
Manufacturer/Country :	
Fabrication Year :	

1. **SUBSTRATE(S)**

Material :		
Dimensions (mm) :		
Comments :		

IMPORTANT **INDICATE CLEARLY IF BERYLLIUM OXIDE IS USED AS SUBSTRATE OR CARRIER MATERIAL**

2. **CONDUCTORS**

	specify thick or thin film	
Material/type [1]):		
No. of conductor layers :		
Min. (design) conductor width :		
Min. (design) dist. betw. conductors :		
Via's dimension :		
Comments :		

NOTES: See last page.

ANNEX C (CONT'D)

3. PRINTED RESISTORS

Material/series and resistivity [1] :		
No. of resistors for this resistivity :		
Trimming method :		
Comments :		

4. DIELECTRIC LAYERS AND OVERGLAZE

Material/type [1]:		
Use [2]:		
Comments :		

5. MOUNTING OF PASSIVE CHIPS

Chip type and no. [3]:				
Method of Electr. Connection :				
Metallisation of chip termination :				
Size [8]:				
Comments :				

NOTES: See last page.

ANNEC C (CONT'D)

6. MOUNTING OF UNENCAPSULATED ACTIVE CHIPS

Chip type and No.[4]):				
Method of Mechan. Attachment :				
Method of Electr. Connection :				
Metallisation back of Chip :				
Metallisation [5] Upper Side of Chip :				
Comments :				

7. MOUNTING OF ENCAPSULATED COMPONENTS

Component type and No. :				
Package :				
Method of Mechan. Attachment :				
Method of Electr. Connection :				
Comments :				

ANNEX C (CONT'D)

8. **WIRE-BONDING**

	FUNCTION OF WIRE BOND			
	From act. chip to substrate	From pass. chip to substrate	From sub-strate to package post	From substrate to substrate
Wire Material :				
Wire Diam. (mm) :				
Wire-bonding Operation type 6)				
Up or down bond on chip :				
Comments :				

ANNEX C (CONT'D)

9. PACKAGE OR CARRIER INFORMATION

Sealed package or carrier :	
External dimensions :	
Material/ Plating of Body	
Material/ Plating of leads :	
No. of leads :	
Feed-through :	
Substrate to package attachm. :	
Sealing method :	
Comments :	

10. ADDED-ON COMPONENT LIST [9]

Description [7]:				
Manuf. type :				
Total No. per type :				
Comments :				

ANNEX C (CONT'D)

NOTES:

1. Indication of manufacturer's type or series is optional.
2. Indicate whether used for conductor isolation, capacitor realisation or overglaze.
3. Passive chip type can be: chip resistor, chip capacitor.
4. Active chip type can be: diode, transistor, integrated circuit.
5. Indicate whether the chip has its surface protected by a layer of glass.
6. Wire-bonding operation type can be: thermo-compression, ultrasonic, thermosonic, parallel gap welding, etc.
7. Added-on component description can be: diode, transistor, integrated circuit, resistor, capacitor, etc.
8. Approximate chip capacitor sizes:
   small (1.9 x 1.9 mm);
   medium (4.4 x 1.7 mm);
   large (5.6 x 5.3 mm).
9. Add more sheets, if necessary.