SECTION 6. METAL-OXIDE SEMICONDUCTOR (MOS) DEVICES

6.1. INTRODUCTION

MOS integrated circuits, particularly those of the complementary form (CMOS), are extremely well adapted electrically for use in space. Power consumption is low and MOS devices employ voltage signals rather than current signals. These features are uniquely suitable for advanced data-handling and spacecraft-control systems. It is unfortunate therefore that many MOS devices show a strong, unpredictable and long-lived response to total-dose radiation. Not all regions of space present a serious problem, but those that are so affected include earth orbits heavily used for unmanned flight, including the geostationary orbits.

If degradation of MOS devices is to be avoided in these orbits, special attention will often have to be paid to both spacecraft design and device procurement. This section will discuss the problem and indicate the best approach to its management. The mechanisms which are the most important in device degradation are attributable to ionisation (hole-electron pair creation) within the silicon dioxide layers. This effect and the consequent effects upon function are described. Structural and operational factors - particularly the thickness of, and electrical stress in, the oxide - have an important influence upon device function in the presence of radiation and are described in detail, but the most important influence derives from the material parameters of the oxide which, in turn, are critically affected by the processing conditions during and after oxide growth.

The term "MOS" has been extended to the recently developed devices in which the metal gate is replaced by a polycrystalline silicon electrode. These are distinguished by the name "silicon-gate MOS devices". Reference is made in the following pages to both discrete MOS devices and integrated circuits, particularly the complementary MOS network (CMOS) which incorporates a number of p- and n-channel transistors on a single chip. Figure 6.1(a) shows an example of a CMOS circuit configuration (2 CMOS inverters in cascade) and a schematic representation of the device structure. The typical characteristics of the MOS structure can be seen. The source and drain regions are heavily doped, diffused "islands" in the substrate or body, and the channels are the surface regions lying between source and drain.

N-type material is typically produced by doping with phosphorus while P-type may be obtained by doping with boron. The gate oxide layer, thermally grown SiO_2, is typically 1000Å (0.1 nm) thick and the metal electrodes are termed "gates".

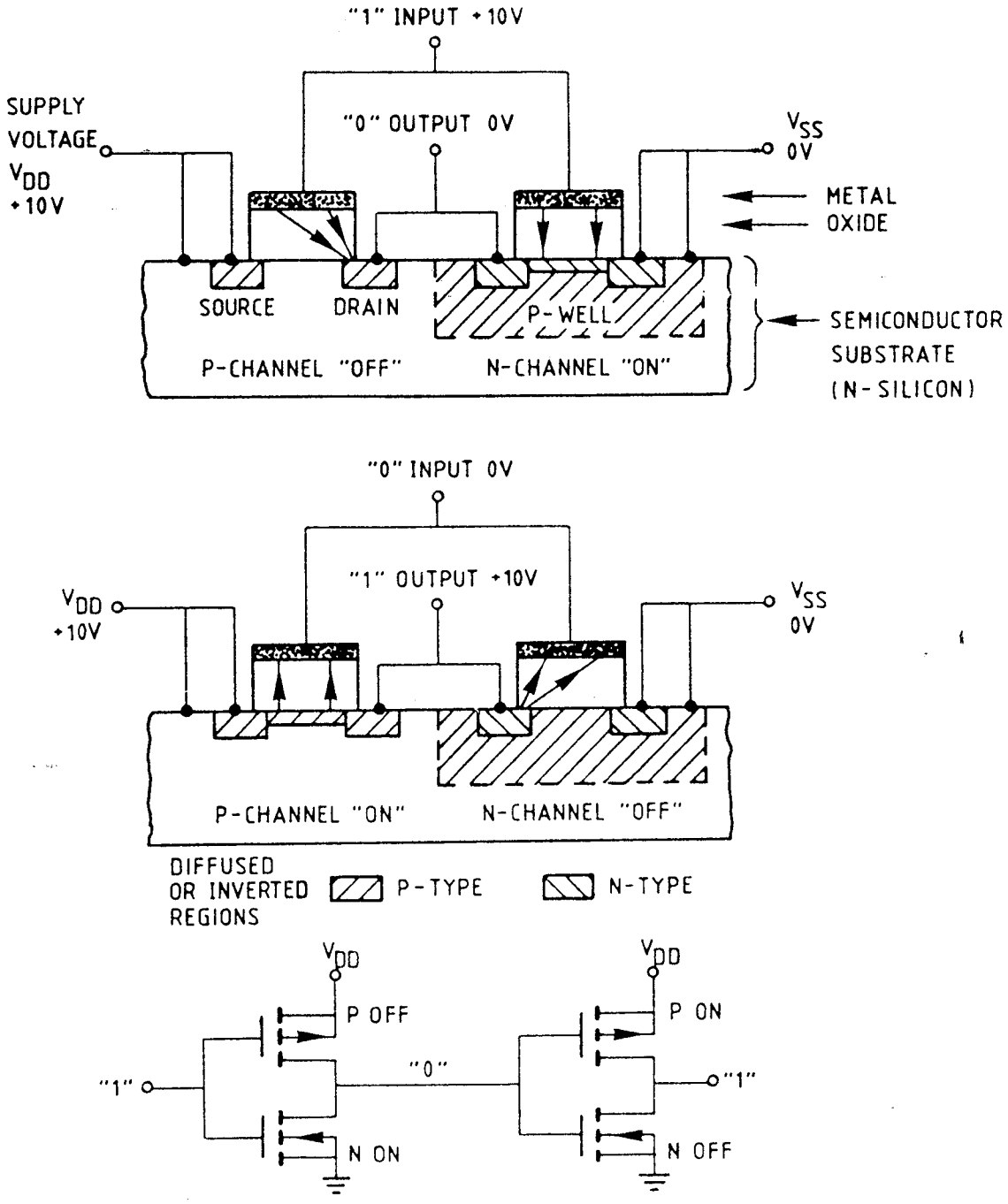
Figure 6.1(b) shows further details of a CMOS chip. The device shown is a large-scale integrated (LSI) circuit. Dimensions may be

as small as 1 micrometre, the gates are made of polycrystalline silicon and the gate oxide thickness may be as small as 0.03 nm. The thicker "field oxides" present additional radiation-effect problems.

One particular source of confusion in nomenclature should be noted here. The term "radiation-hardness" is often used to describe several different forms of tolerance to radiation in MOS and other devices. This term has a military connotation. Originally, "hard" meant "invulnerable to attack". Where possible, we will use the term "tolerance (or sensitivity) to radiation" instead of "hardness". However, the term "hardness assurance" is already widely used in the U.S. "Megarad-hard" is now used to signify "capable of withstanding one megarad of ionising radiation".

Confusion may arise on account of the military requirement to survive the transient effects of an intense burst of gamma rays and neutrons at a dose rate at least 10 billion times higher than that experienced in space. The long-lived effects or "total doses" received from this burst may be of the same order as that accumulated in a space mission, but neutron damage may be received from the military environment. From typical figures for the space and military environments, given in Table 6(1), it can be seen that transient effects, usually the dominant problem in military devices, will be negligible in the case of radiation belts. The space doses are for a typical internal location within a spacecraft structure.

Because of the "logic upset" produced in the military case, special device structures, which minimise the photocurrents produced, have been developed. These may not necessarily have good tolerance to total-dose effects. Thus, in the procurement of devices, the term "radiation-hardened" should be investigated and qualified before its relevance to space can be established. Similar distinctions should be drawn when considering testing methods.



The structure of an integrated complementary-symmetry MOS (CMOS)inverter showing typical bias and logic levels. The lower figure shows two inverters in cascade.

FIGURE 6.1 (a) - THE TYPICAL MOS STRUCTURE

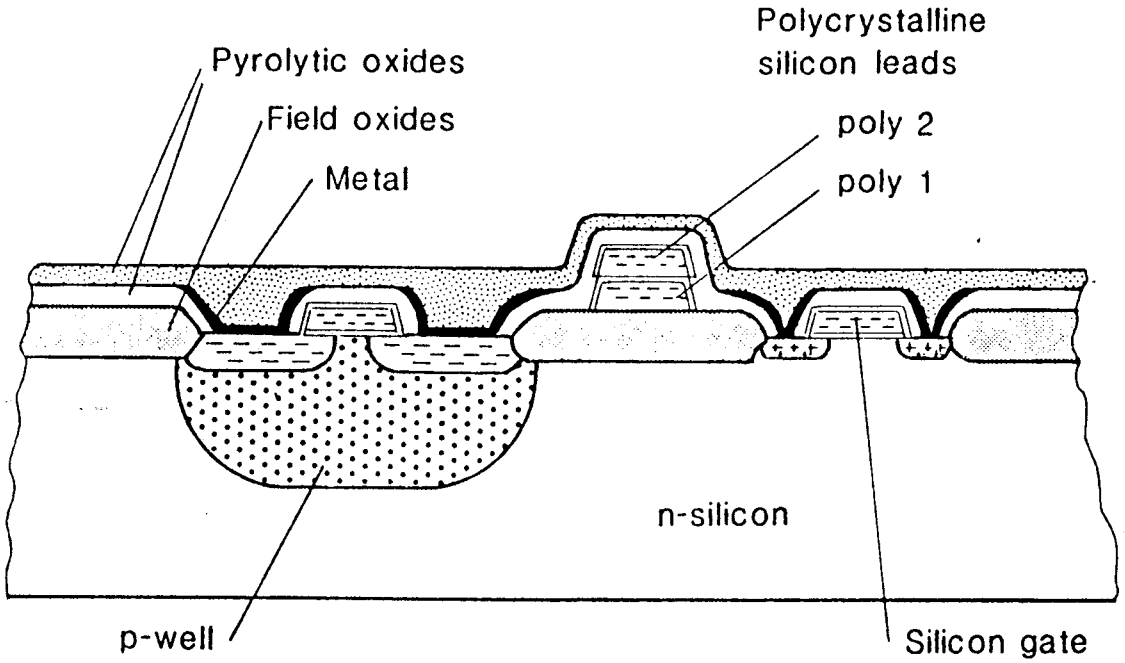


FIGURE 6.1 (b) - TYPICAL SILICON-GATE CMOS STRUCTURE OF 3 - MICROMETRE SCALE

TABLE 6(1) - COMPARISON BETWEEN TYPICAL RADIATION ENVIRONMENTS IN A MILITARY "WEAPON BURST" AND SPACE RADIATION BELTS

	Military	Space
DAMAGE : Neutron fluence (cm^{-2})	10^{14}	–
equiv. 1 MeV electron fluence (cm^{-2})	10^{17}	10^{12}
TOTAL DOSE : rad (Si)	10^{16}	10^{15}
DOSE RATE : rad (Si)	10^{11}	10^{-2}

6.2. EARLY INVESTIGATIONS

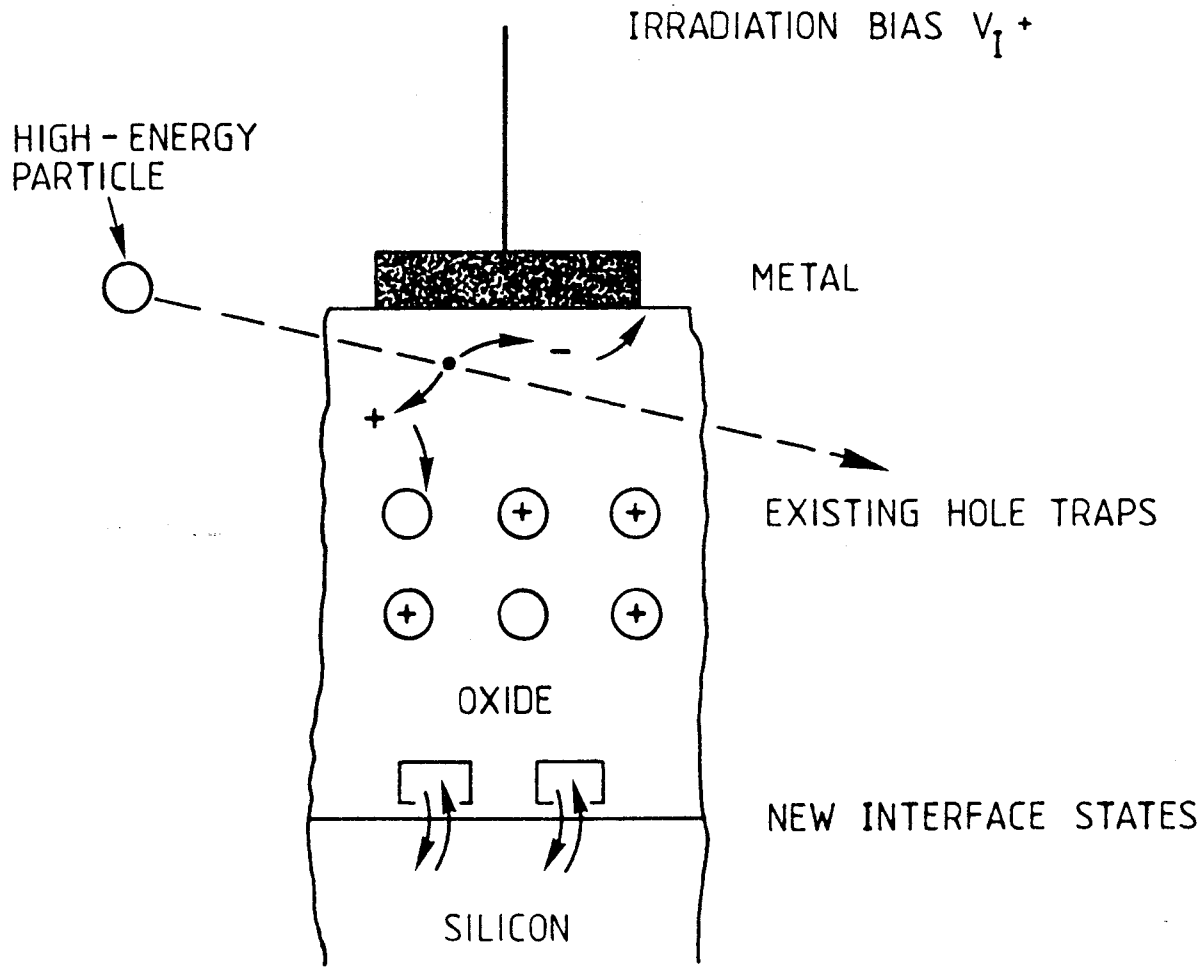
The effect of radiation on the performance of MOS devices was first noted in 1964 by Hughes and Giroux. This observation contradicted the earlier belief that because surface channel devices would not be affected by the production of minority-carrier recombination centres in silicon, they would not undergo strong changes as a result of irradiation. Even though radiation-induced charge-trapping had long been recognised as, for example, the source of colour-centre formation in bulk silica and other insulators, it was not appreciated that similar effects in the insulator layer of any MOS device would strongly influence performance.

At this time, unexpected surface degradation effects were also observed in planar bipolar transistors. It could be shown that these effects were not due solely to the well-known atomic displacement damage; charge-trapping in the passivating oxide layer was again believed to be the cause.

During 1965 and 1966, much experimental evidence was produced to support the theory that radiation-induced degradation in MOS devices was caused by the trapping of charge (holes) in the oxide layer and that the amount of charge trapped depended strongly upon the voltage across the oxide during irradiation. It was also concluded that a secondary effect, involving the rearrangement of atomic bonds at the oxide/silicon interface, was contributing to the degradation; this is the production of new "interface states".

Figure 6.2 illustrates the two effects mentioned above. Note that the term "irradiation bias" (V_I) is used to define specifically the gate voltage applied to a device during irradiation. This is commonly a steady voltage which induces the electric field in the oxide (it may however be variable during real device operation). The influence of this field is very important in determining the rate of device degradation in space. Atomic displacement damage in either the silicon or the insulator does not appear to play a significant role in these phenomena. The trapping mechanism appears to occur to

some extent in all insulator types. Preliminary attempts were made to discover the origin of the hole-trapping and to suppress it, but these did not meet with immediate practical success. Some users then settled down to try and understand, control and accommodate the large changes produced by radiation in commercial MOS devices.



The ionisation, charge transport, hole-trapping and interface-state mechanisms in the gate insulator.

FIGURE 6.2 - MOS DEGRADATION

Research and development to produce a practical "Megarad-hard" CMOS technology was funded by the U.S. Government, through Naval Research Laboratories, NASA and other agencies. Semiconductor laboratories leading the effort included Sandia National Laboratory, RCA, National Semiconductor and Harris. European governments funded research at a lower level, for example in the 1970's at GEC Hirst Research Centre, Wembley; SGS, Milan and C.E.N., Grenoble. Progress reports of the above work can be found in the annual proceedings of the IEEE Nuclear and Space Radiation Effects Conference, published regularly as the December issue of the IEEE Transactions of Nuclear Science. More recently, Japanese contributions have been made, funded by the Future Electron Devices Programme of M.I.T.I.

6.2.1. MOS failure mechanisms

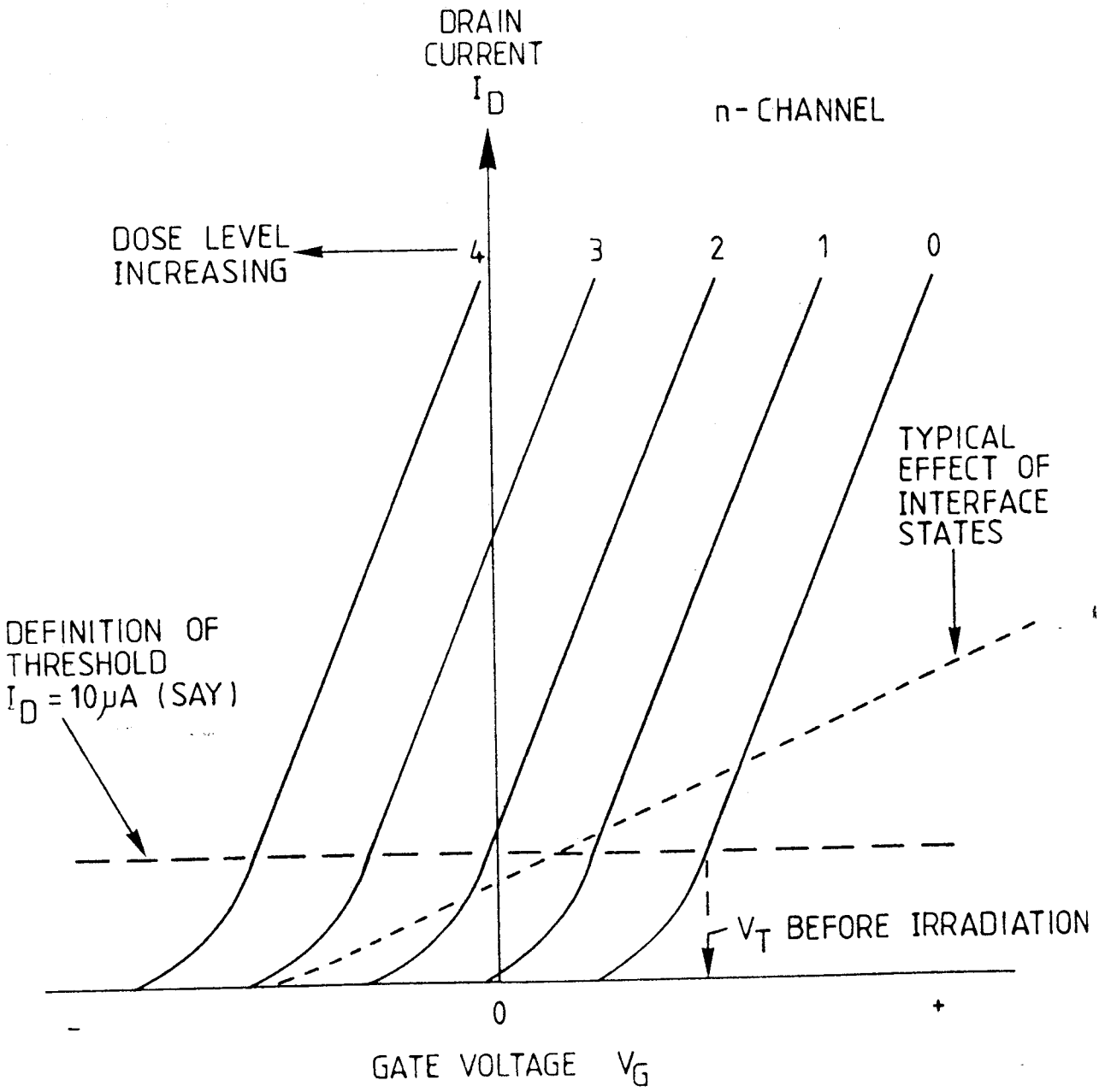
The electrical consequences of radiation-induced physical changes in MOS devices are the progressive loss of function and eventual "failure" of a MOS circuit. Figure 6.3(a) shows a series of parallel I_D-V_G curves for an n-channel device, resulting from successive increases in dose. Each of the curves corresponds to the onset of particular malfunction in, say, the CMOS logic gate shown in Figure 6.1. We can consider each type of malfunction as defining a "failure mode".

Table 6(2) lists the four major performance degradation effects which are likely to appear at the four dose levels indicated in Figure 6.3 (a). The table also gives an indication of the real dose and threshold shift associated with each failure mode in a typical CMOS circuit.

It is clear that if one were designing CMOS circuits specially, one could build in some tolerance to these effects. However, in commercial LSI circuits, the internal circuit design is predetermined and may have poor tolerance to one of the four effects noted above. Thus, "failure" cannot be defined at the level of the single device element, but is rather the point at which a particular network of devices no longer tolerates these effects. We can define a radiation dose limit or "Maximum Acceptable Dose", D_A(max), for any CMOS circuit based on the dose at which the significant failure mechanism appears for that circuit. In spacecraft applications, which are limited for power, this is usually the effect noted in Table 6(2) as "V_{TN} crossing zero (VTNZ)", which leads to large increases of quiescent current. The acceptable levels of current increase may be very low.

TABLE 6(2) - PROGRESSIVE NATURE OF CMOS FAILURE AS A FUNCTION OF RADIATION DOSE

Dose level in Fig. 6.3(a)	Failure mechanism number	Main degradation effect	Symbol	Typical values for CMOS LSI	
				Dose rad (Si)	$-\Delta V_T$ volts
1	1	Minor 'noise immunity reduction'; possibly minor loss in switching speed	NIR	8×10^2	0.2
2	2	Sharp quiescent current increase due to 'V_T of N-channel crossing zero	VTNZ	5×10^3	1
3	3	Switching speed reduction	SSR	1×10^4	2
4	4	Change of logic state impossible: 'Logic failure'	LF	3×10^4	4



Typical drain-current/gate-voltage curves for an N-Channel MOS device, showing the progressive effect of increasing radiation dose. The dose levels shown (1 to 4) correspond to the "failure mechanism" described in Table 6(2). The solid curves show the ideal case, where positive charge only is introduced into existing traps; the effect of the production of interface states on the shape of the curves is shown by the broken line.

FIGURE 6.3(a) - CMOS DEGRADATION AND FAILURE

6.2.2. The VTNZ effect and its impact

The growth of leakage, or quiescent current (I_{SS}), in CMOS devices as a function of dose is illustrated in Figure 6.3(b). This important functional consequence of threshold shift is often the most easily monitored parameter in MSI or LSI circuits. In this case, the "Maximum Acceptable I_{SS} Value" has been arbitrarily set at 0.5 μA.

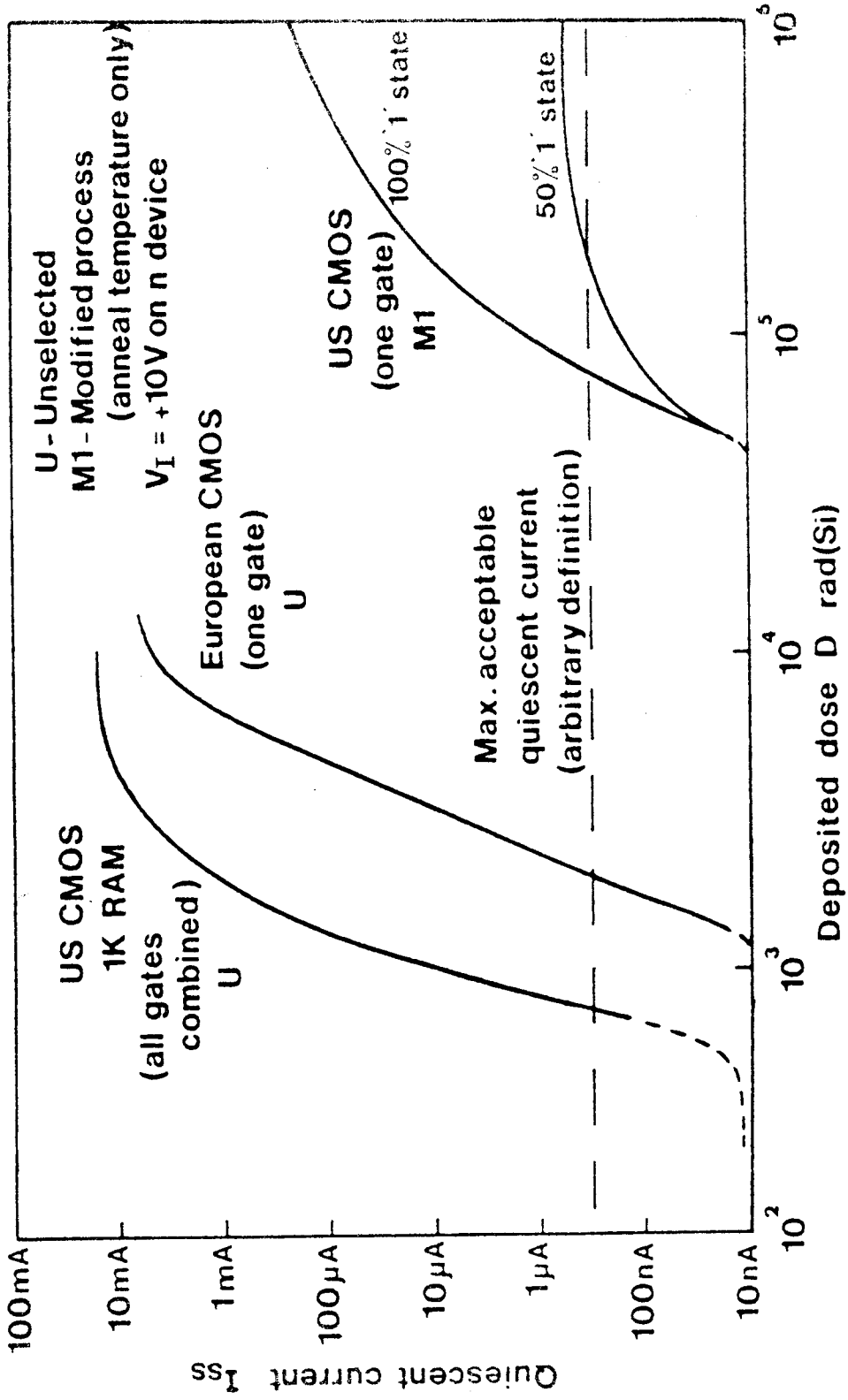
If leakage at the "maximum acceptable I_{SS} value" produces system failure, note that the maximum acceptable dose value can vary by over a hundredfold from type to type. At a constant daily dose rate, this means that the life of the system can vary by a hundredfold depending on the material parameters of the CMOS gate oxides. It is this uncertainty which makes extensive radiation testing necessary.

6.2.3. Other effects on logic operation

A CMOS gate may be regarded as a type of "potential divider" with the potential, V_{DD} , being dropped across various sections of the device according to its logic state. Clearly, a pronounced leakage current in a transistor which is meant to be "OFF" will reduce the potential difference across that channel. Thus, the difference in output voltage between the '0' and '1' states will be reduced, correspondingly degrading the input (gate) voltages to the next inverter pair. This is the Noise Immunity Reduction (NIR) noted in Table 6(2).

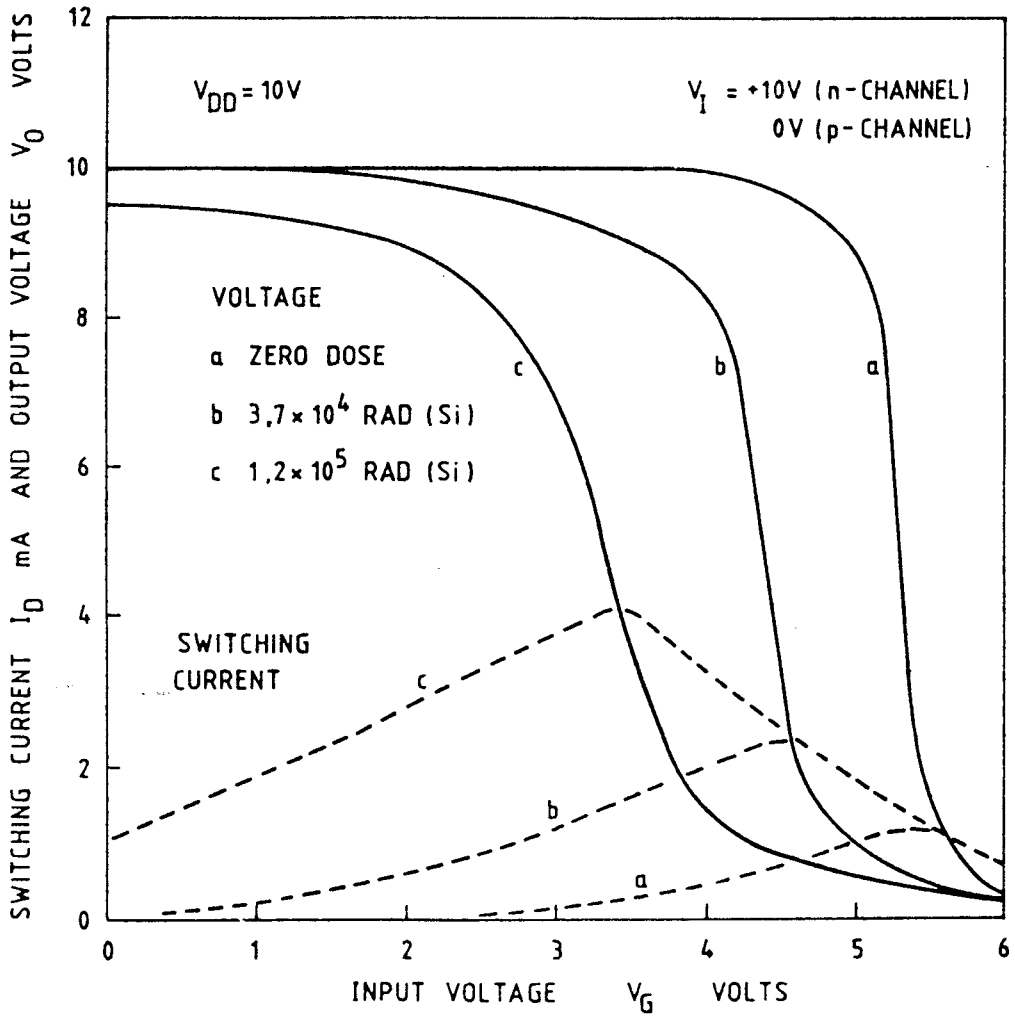
The effect of this is illustrated in Figure 6.4. The full curves show the voltage waveform associated with CMOS gate-switching before and after various doses of radiation. The broken curves show the relevant channel current which flows during the switching phase. In the experiment shown, V_{DD} was +10V and the irradiation bias was +10V for the n-channel and zero for the p-channel.

Note that, in LSI devices, leakage can occur under the field oxides and produce increases in the I_{SS} value even though the N-channel transistor itself has not crossed zero V_T.



Quiescent current (supply current when the gates are not changing state) as a function of dose in typical CMOS integrated circuits. Growth of this current is one important functional effect of the shift of threshold voltage in the n-channel element (VTNZ effect).

FIGURE 6.3(b) - LEAKAGE CURRENT IN CMOS DEVICES



Radiation-induced changes in logic transfer characteristics of a CMOS inverter. Increasing dose causes progressive loss of a logic definition and decrease in height of the output voltage step, with corresponding increase in power consumption. The left-hand side of the switching-current waveform is controlled by the N-channel component (large shift observable) and the right-hand side by the p-channel (no shift).

FIGURE 6.4 - CMOS SWITCHING CHARACTERISTICS

6.2.4. The effect of interface states on logic operation

The qualitative effect of interface states (the complex rearrangements of atomic bonding in the SiO_2/silicon interface caused by ionisation) is to distort both the I_D-V_G and C-V characteristics. The common result is that the I_D-V_G curve is reduced in slope, as shown by the broken curve in Figure 6.4. In an n-channel device, this effect is to a degree beneficial in that the threshold shift is effectively reduced. A high degree of interface state production can decrease the I_D-V_G slope so much that the threshold voltage, V_{TN}, becomes even higher than its pre-irradiation value ("rebound"). The "transconductance" of the channel (the rate of change of I_D with V_G at given gate and supply voltages) is reduced and this may lead to further degradation of switching speed in a CMOS device.

6.3. LOSS OF FUNCTION IN MOS DEVICES

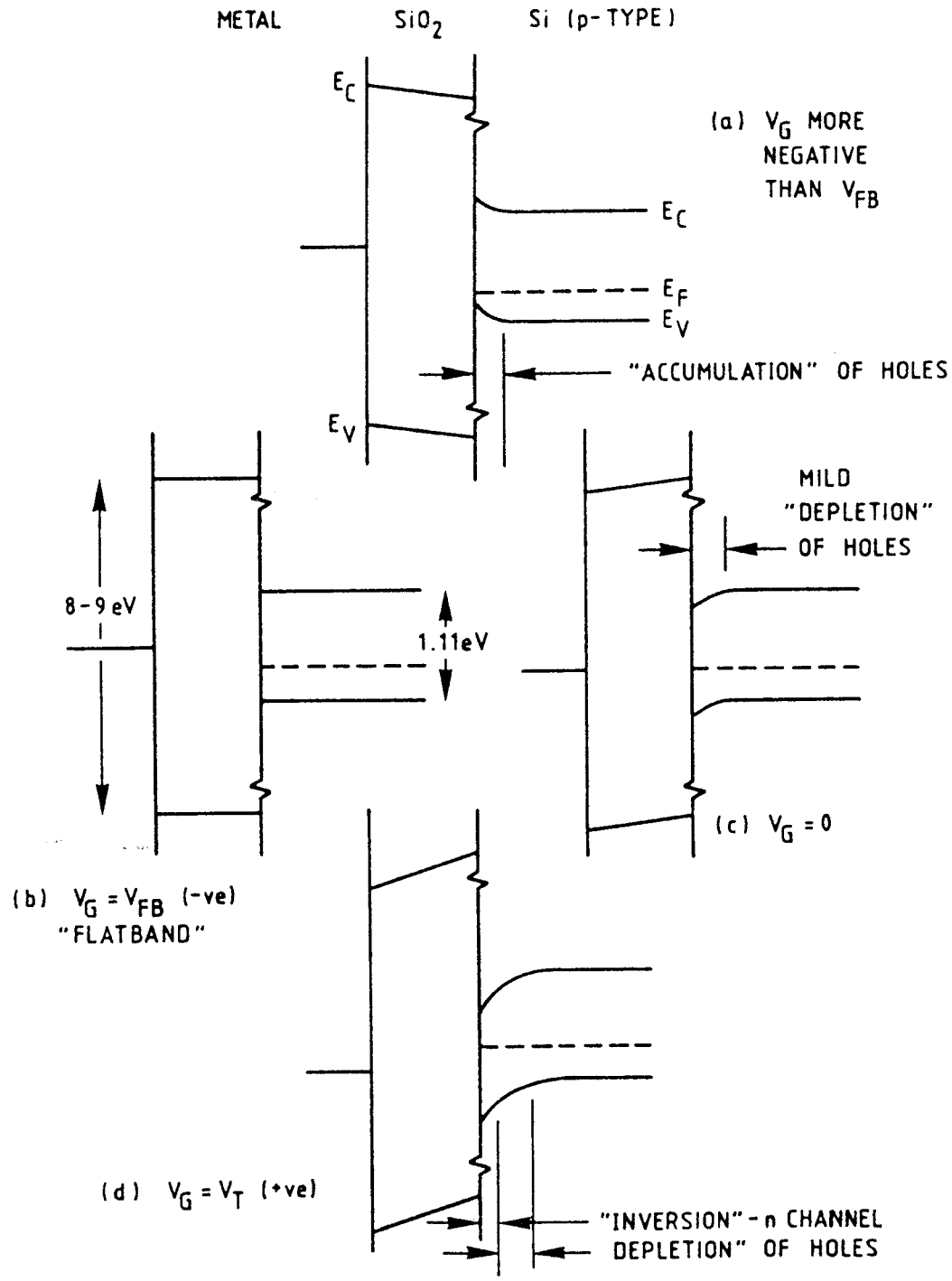
6.3.1. MOS transistor action

Figure 6.5 shows the electron energy levels of the conduction and valence bands at the interface between SiO_2 and a p-type silicon substrate (*). Note that the band-gap in silicon is 1.1 eV (the difference in energy between the conduction and valence bands) while that in the insulator, SiO_2, is about 9 eV. The Fermi level which, in an intrinsic semiconductor, is mid-way between the two bands, is nearer to the valence band in p-type silicon. If the system is in equilibrium (the gate and semiconductor are at the same potential), the Fermi level must remain constant throughout the two regions. As shown, the differences in work function between the semiconductor and the gate electrode must then be resolved across the interface through bending of the Si energy bands.

In simple terms, the downward bending of the silicon energy bands at the interface may be interpreted as having the effect of pushing the majority-carriers, holes in p-silicon, away from the interface, leaving a narrow "depletion" region of ionised immobile acceptor atoms (boron) in energy states just above the valence band.

Application of a low negative voltage to the gate (with respect to the substrate) will create an electric field across the insulator and, initially, have the effect of flattening the energy bands at the interface.

(*) For further details of the solid-state physics of MOS function, refer to textbooks by Grove and Sze.



The electronic energy levels at the oxide/silicon interface showing band bending and the 'Flatband' condition. Band bending in the silicon at zero gate voltage will result from a difference in work function between the silicon and the gate electrode and from the presence of fixed oxide charge.

FIGURE 6.5 - ENERGY BANDS AT THE INTERFACE

The voltage at which the bands are perfectly flat is known as the "flatband voltage", V_{FB}. Further increase in negative voltage will cause the bands to bend upwards, creating an "accumulation" of majority carriers, holes in p-silicon, at the interface.

Application of a voltage between the source and drain junction of a MOS transistor in the "accumulation" condition will not cause a channel current to flow, owing to the conflicting rectifying actions of the two p-n junctions (source/substrate and substrate/drain).

Application of a positive gate voltage, on the other hand, will cause the energy bands to bend further downwards. This will have the initial effect of "pushing" more holes away from the interface, increasing the width of the depletion region. With increasing positive gate voltage, the depletion will reach a "limit" and "inversion" will occur. At this point, there is a rapid generation of conduction band electrons in the surface region. The conduction band at the surface will now be very close to the Fermi level and, in this respect, the silicon at the surface will resemble n-type material in its transport properties (hence the term "inversion"). A voltage between n-type source and drain, V_{DD}, will now cause conduction through this region, called the "channel". The gate voltage at which inversion is sufficiently established to cause a measurable channel current to flow (typically 10 μA) is defined as the "threshold voltage" (V_T).

The picture given above is simplified, but will perhaps assist in understanding the mode of operation of this device and the mechanism of radiation-induced degradation. There are of course no sharp divisions between accumulation, depletion and inversion.

6.3.2. Flatband and threshold shift

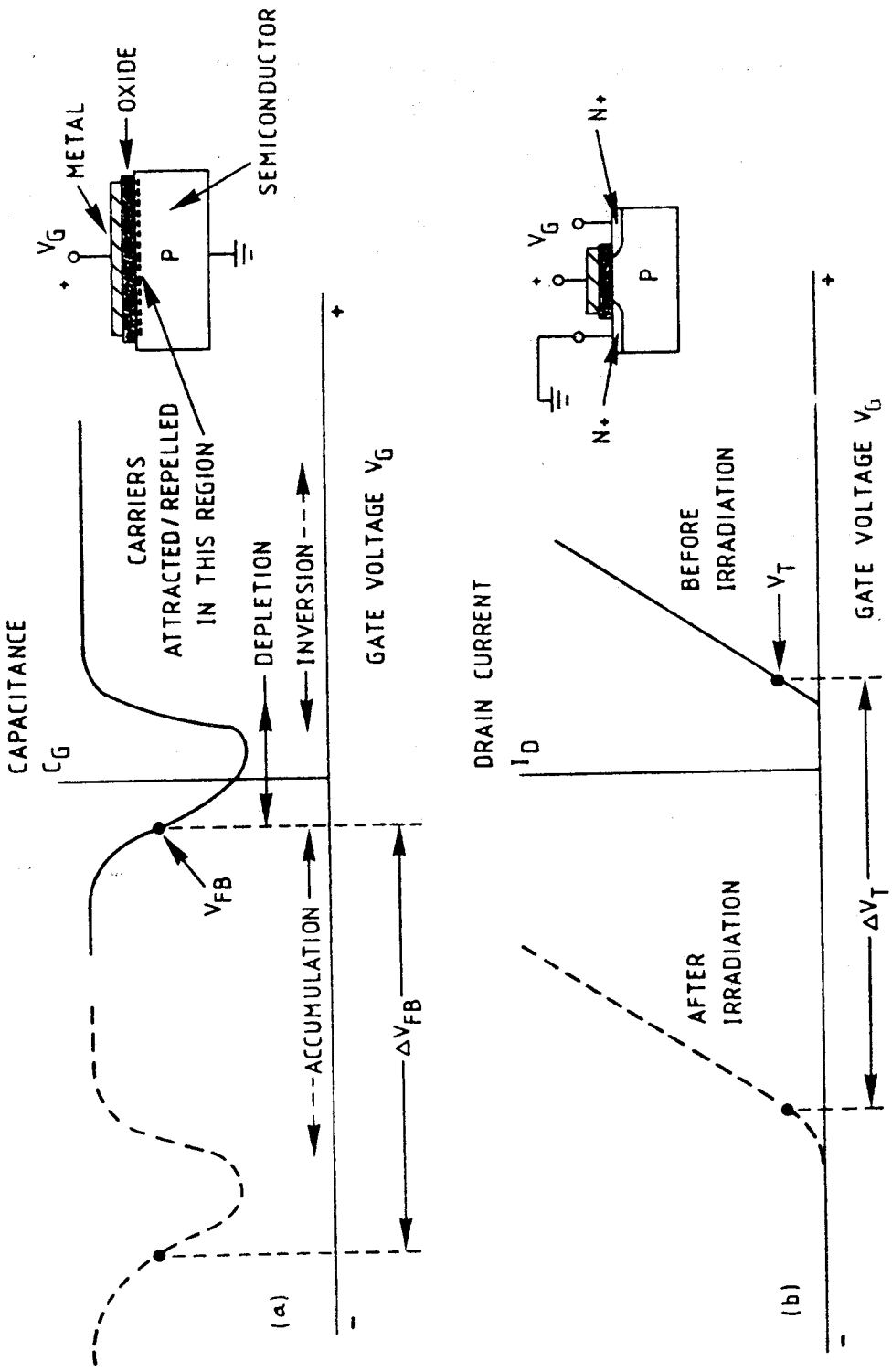
The threshold voltage of a MOS transistor is ascertained by measuring the channel current (usually termed "drain current)", I_D as a function of the gate voltage, V_G, at a constant supply voltage, V_{DD} (see Figure 6.3 (a)). The resulting characteristic curve for a p-substrate device is shown in Figure 6.6. Flat band voltage is usually estimated by plotting the small signal gate capacitance (C_g) versus the gate voltage of the device. The resulting "C-V curve" for a P-substrate device is of the form shown in Figure 6.6(a). The minimum in this curve reflects the transition from "depletion" to "inversion" conditions. Comparing Figures 6.6 (a), note how the value of V_T on the I-V characteristic is always aligned with a point near this minimum. The flatband condition is known to occur when the ratio C/C_O is approximately 0.8. Note that this measurement does not involve the measurement of channel current and, in fact, can be accomplished by means of an MOS capacitor with appropriately doped silicon substrate; source and drain diffusions are not

required. MOS capacitors are therefore a useful aid in the laboratory investigation of radiation effects.

Positive charge (trapped holes) induced by ionisation in the oxide layer of a MOS device will have the same qualitative effect on the potentials in the silicon as the application of a positive gate voltage, it will bend the energy bands further downwards and tend to induce inversion in a p-type substrate.

An alternative interpretation of this effect, without involving energy bands, is to say that the trapped positive charge induces negative image charge in both the gate and substrate; the charge in the substrate therefore increases the n-type conductivity in an n-channel device. Thus, a smaller threshold voltage will then be registered. Given sufficient trapped charge, inversion may be established by the charge alone and a "leakage current" will flow in the channel even in the absence of a gate voltage. This is the VTNZ effect in Table 6(2).

If V_T of the n-channel has passed zero, the device is "ON" when it should be "OFF". Similarly, the existence of trapped charge will mean that a greater negative gate voltage will be required to achieve the flatband condition. Thus, simple trapped-charge accumulation results in an essentially parallel shift of the C/V and I_D-V_G characteristics. Discussion of these shifts in threshold, V_T, and flatband, V_{FB}, voltages forms the major part of this section. If we ignore various distorting effects, V_T is equal to V_{FB}. As described, the degree of parallel shift observed in MOS devices varies very widely with the material parameters of the insulator layer.

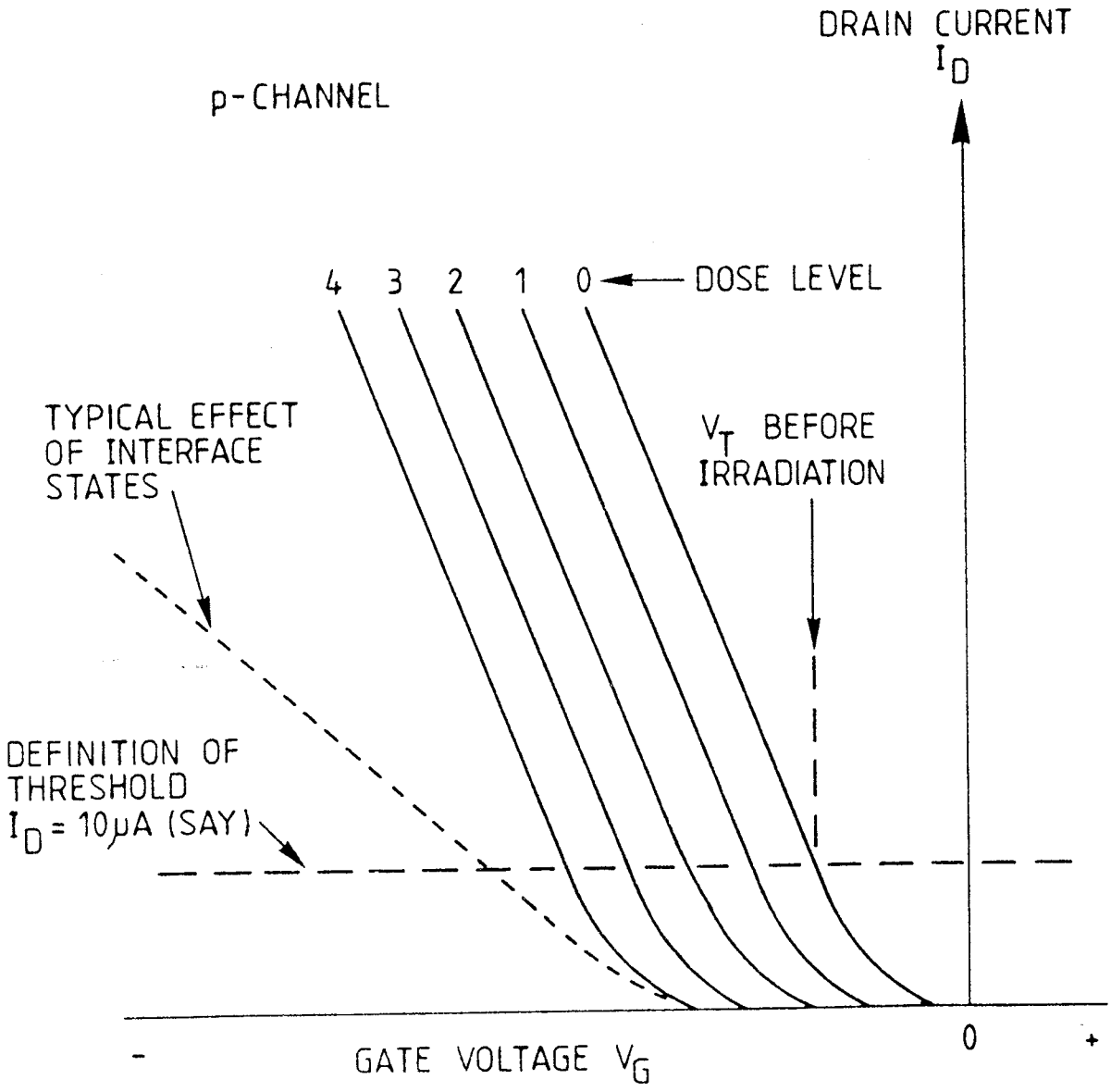


Typical variation of capacitance and drain current with gate voltage showing the shifts in flatband and threshold voltages due to trapped charge (no interface states)

FIGURE 6.6 - MOS CHARACTERISTICS

6.3.3. Equivalent effects in P-channel devices

While, in the absence of space charge build-up, an n-channel MOS requires a positive gate voltage to cause the channel to conduct, a p-channel devices requires a negative bias. As shown in Figure 6.7, the parallel shift in the I_D-V_G characteristic caused by trapped charge means that an increasing negative bias is required to operate the device. At high radiation doses, it may therefore become impossible to switch the device "ON". Additionally, the creation of interface states, resulting in a typical characteristic as shown by the dotted curve, must always - in contrast with n-channel devices - make matters worse.



Typical radiation-induced shift in the drain-current/gate-voltage characteristic of a p-channel device. Leakage current will not be a problem in this case, but progressively higher gate voltages will be required to invert the channel region.

FIGURE 6.7 - DEGRADATION OF P-CHANNEL MOS

6.4. DEGRADATION MODELS OF MOS DEVICES

6.4.1. A simple analysis of radiation effects in MOS devices

As part of the "Fulmer Radiation Effects Engineering Handbook" project, simple prediction models were developed to deal with threshold voltage shift in MOS devices as a function of dose and electrical stress applied during irradiation. These were subsequently published (Freeman and Holmes-Siedle, 1978).

The physical model used is in accordance with current research, but uses simplified assumptions with respect to trap location in the oxide and yield of available charge. It employs a "worst-case" (linear dependence) of charge build-up on dose. The result is an analytical method suitable for characterising the behaviour of commercial MOS devices under laboratory radiation test and the subsequent extrapolation of the test data to degradation with time in space.

In the analysis, laboratory test data are used to characterise the gate oxide of an individual transistor by an A-value. This is a charge-trapping probability and the most sensitive devices have an A-value of 1.0. The threshold voltage shift in space, ΔV_T, is predicted with the aid of the formula:

$$\Delta V_T = R.A.D. \qquad \text{.....6(i)}$$

where R is calculated from oxide thickness and other parameters while D is the mission dose predicted for the device in a given position in a satellite. If the original V_T values cannot be measured in the laboratory, the manufacturer can supply the original value of V_T for the devices as used in integrated circuits. Given these data, we can calculate the earliest time at which the device may malfunction in space.

Refinements of the model can deal with electrical stress effects, interface effects and post-irradiation effects (Freeman and Holmes-Siedle, 1978; Holmes-Siedle and Adams, 1983; D.K. Nichols, 1983).

6.4.2. Importance of electrical conditions during irradiation

Radiation effects in MOS devices are unusual because these devices are extremely sensitive to the application of voltage, especially gate voltage, V_I, during irradiation. This arises directly from the physical mechanism which, as explained earlier, involves the transport of charge across the gate oxide. The yield of charge available for trapping is very sensitive to the value of the field in the oxide film when the charge pairs are being generated by the irradiation. This is dealt with in the simple analytical model, described earlier, by the use of a calculated charge yield, f(E).

While experimental results vary from this owing to interface effects, the use of the charge yield factor gives an acceptable "worst-case" model for powered devices. However, the prediction of "zero degradation" for unpowered devices is not correct and test data should be used to establish the effect of devices in a "resting condition".

The terminology adopted here for the gate bias values applied during irradiation is as follows:

$V_I +$: positive bias applied to gate during irradiation,
$V_I -$: negative bias applied to gate during irradiation,
$V_I 0$: zero bias (gate shorted to body) during irradiation.

Thus, for example "irradiation at $V_I + 5$" would describe the application during irradiation of +5V to the gate relative to the silicon body or substrate of the device. The oxide field, E_I, created thereby in an oxide thickness of 0.1 μm would be 50V per micrometre. In a CMOS gate in the "1" condition with $V_{DD} = 5V$, the n-channel device is in the $V_I + 5$ condition, but the p-channel device is in a different condition, not unlike "$V_I 0$".

6.4.3. Intermittent biasing

It has been known for some time that when the electric field across the oxide layer of a MOS device is released during irradiation, the trapped charge begins to decline. This is due to the neutralising effect of photoelectrons emitted into the oxide by the electrodes. This mechanism is effective even if the rate of cycling of the field were many times per second. Thus, for devices which are subject to cycling, the maximum acceptable dose is likely to be higher, typically by a factor of 5, than if the irradiation bias were constantly applied. Figure 6.8 shows the marked effect on the maximum acceptable dose of "50% cycling" (V_I applied for half the time). Use of a lower bias value not only increased the acceptable dose, but also enhanced the effect of cycling. It should be noted that the broken sections of the curves in this figure tend towards a very high dose value.

A further illustration of the effect of intermittent biasing is shown in Figure 6.9. Here, irradiation biases of zero and -9V are applied to a typical p-channel MOS device. If the cycling procedure is interrupted and the bias thereafter held constant, the resulting "growth curve" should gradually approach the upper and lower limit curves. There is scope for introducing a "resting" policy, either within the chip or over the whole subsystem. Such redundancy would significantly prolong the useful life of all MOS components in space. However, the build-up of interface states often continues during irradiation at zero bias; therefore, caution should be exercised in applying this technique. The best approach is to

simulate in the laboratory the type of cycling expected in use and operate the devices in this mode during laboratory irradiation tests.

6.4.4. Gate oxide thickness dependence

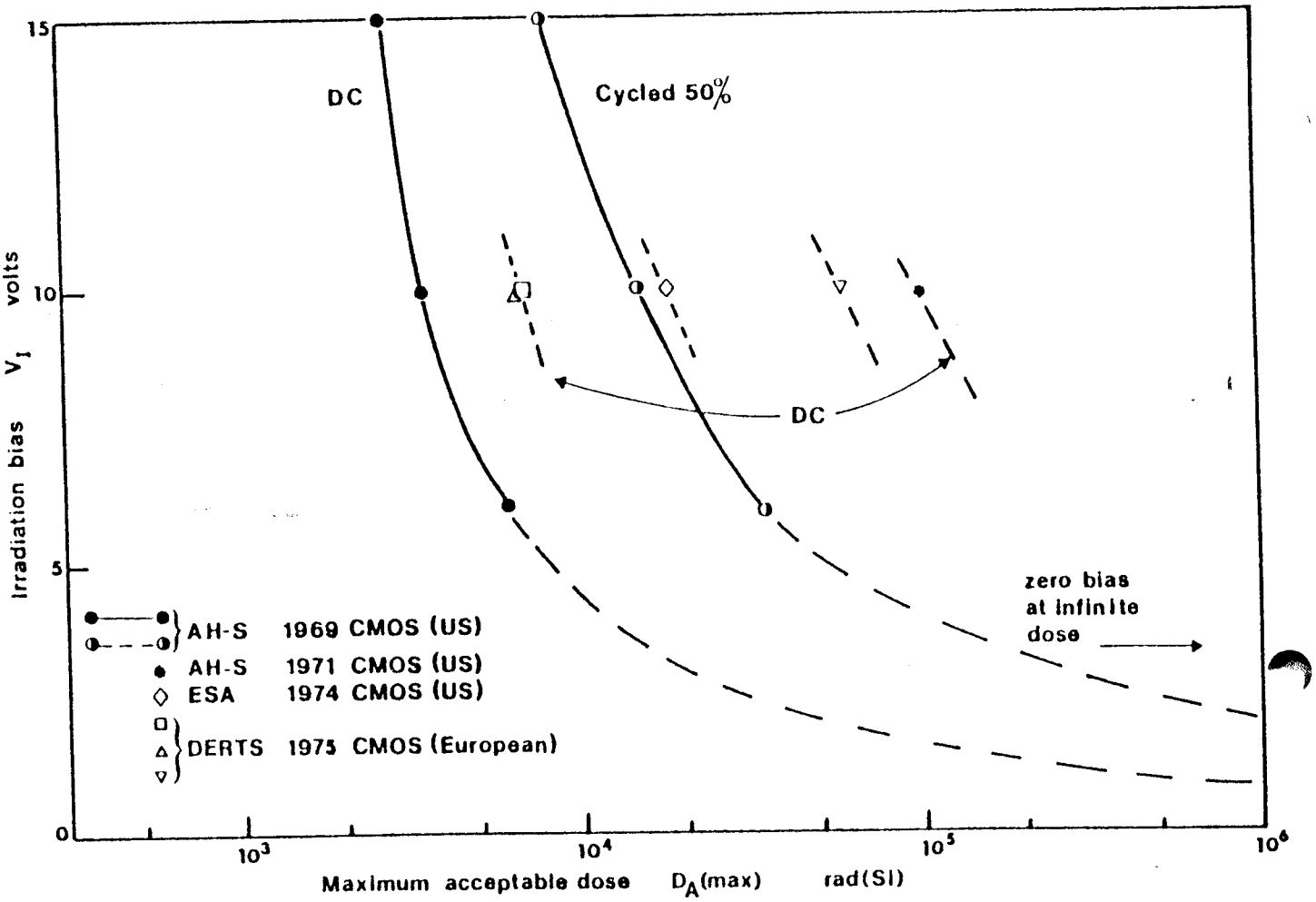
Experimental work on oxide thickness dependence, described by Derbenwick, Gregory and Fossum (1975), indicates that radiation-induced threshold shifts vary as the cube of the oxide thickness, d_{ox}^3, if the oxides are grown directly to a number of desired thickness values. Hughes and Powell (1976) disagree with the conclusions of Derbenwick and colleagues and show experimental evidence of a d_{ox}^2 dependence even for oxides grown to varying thicknesses. In the very simple model of derived threshold shift, described earlier in this report, threshold voltage shift is effectively dependent upon the square of the oxide thickness.

6.4.5. Simple engineering model of MOS degradation

The equations derived in the simple analytical model described above have been used to construct the set of curves shown in Figures 6.10 to 6.13. These figures show examples of a number of possible sets of curves which could be derived from the model. As shown in the insets, some typical values of oxide thickness and charge distribution have been selected. In modern technologies, the oxide thickness values may be lower than those shown.

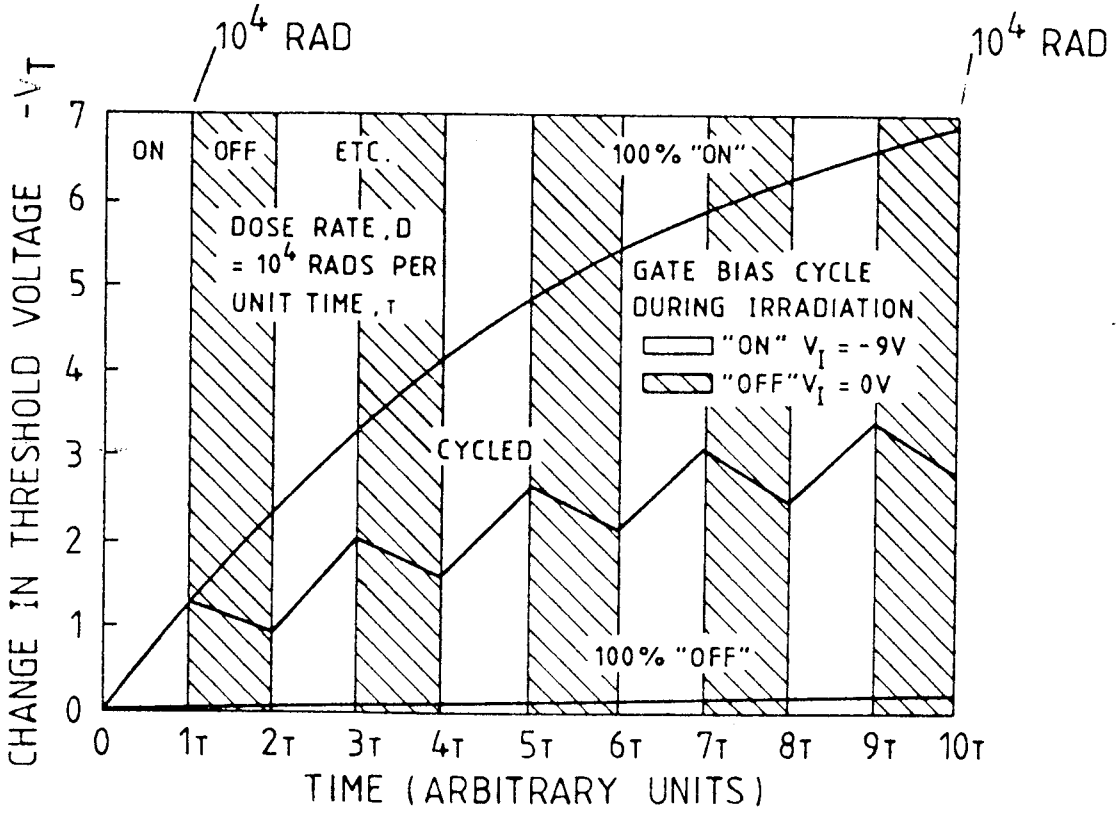
Figures 6.12 and 6.13 show initial growth and both types of saturation for a range of 'A' values from 1.0 ("soft") to 0.01 ("hard") with V_I equal to 10V. Note that the case of the unpowered device ($V_I 0$ condition) is not covered here. Experimentally, a finite charge build-up is found for improved devices although the simple model predicts no change. Here, each case should be examined experimentally, although research is proceeding on models for the unpowered case (Hughes, 1985; Holmes-Siedle, Adams, Pauly & Marsden, 1985).

These curves may be combined by the engineer in a variety of ways. Figure 6.12 may be regenerated for V_I = +8V merely by displacing the whole set of curves by the same horizontal distance by which the 8V curve is displaced from the 10V curve in Figure 6.10.



The "maximum acceptable dose" for some specific devices as a function of irradiation bias. The beneficial effect of "50% cycling" in the 1969 series is clear. Some later measurements of "maximum acceptable dose" at a single bias value are included for comparison; these were all obtained under conditions of continuous operation.

FIGURE 6.8 - THE EFFECT OF INTERMITTENT BIAS



Threshold voltage shifts as a function of time (equivalent to dose) for a typical p-channel MOS device subject to zero bias, 50% cycling, or constant bias during irradiation.

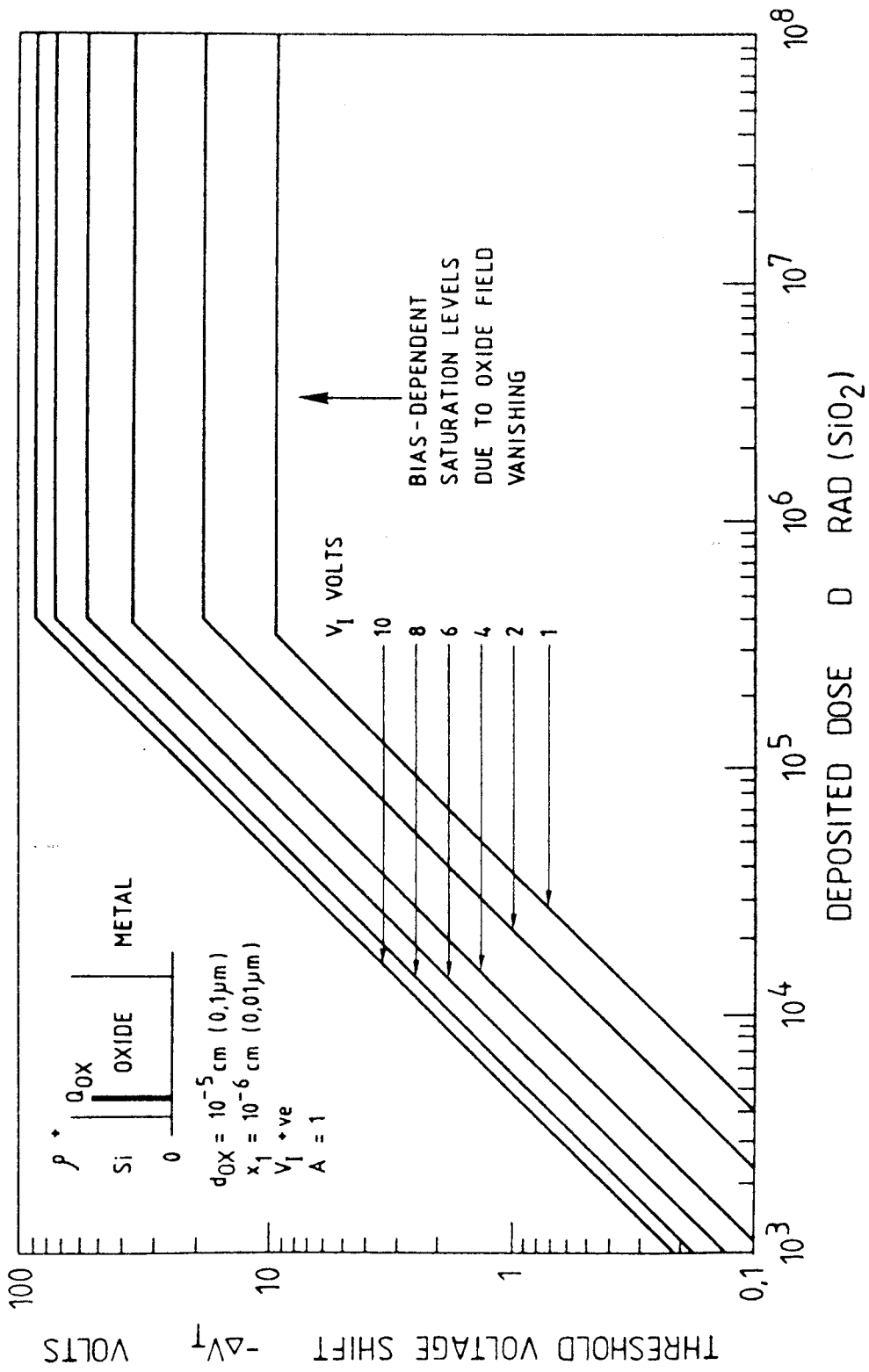
FIGURE 6.9 - THE EFFECT OF INTERMITTENT BIAS

By comparing experimentally determined V_T growth curves with theoretical sets such as those illustrated, it should be possible to obtain a measure of radiation sensitivity of a MOS device in terms of the trap density and "trapping probability" ('A' value) of the oxide (*).

(*) Experimental data at low doses will indicate the 'A' value; those at very high doses the trap density.

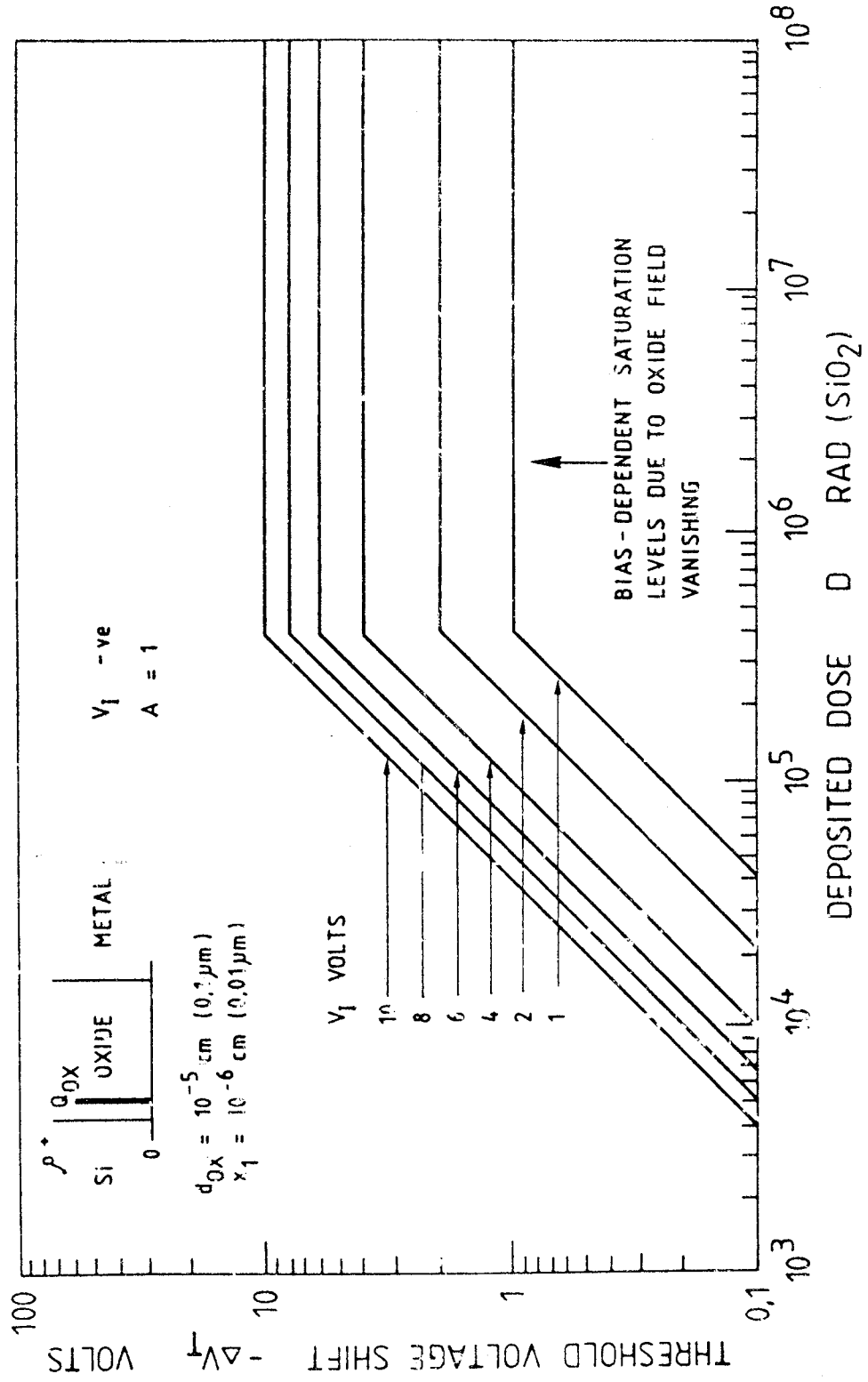
6.4.6. Classification of "hard", "soft", and "medium"

Figure 6.14 shows a classification scheme based on the "growth curve" format presented earlier. The figure is for device irradiation under a positive gate bias of 10V. An oxide thickness of 0.1 nm is taken. The format is divided into three areas: "hard", "medium" and "soft". The position of a device test result in this framework is a useful indication of the suitability of that device for use in the space environment. Experimental results generally follow the "corridors" shown.



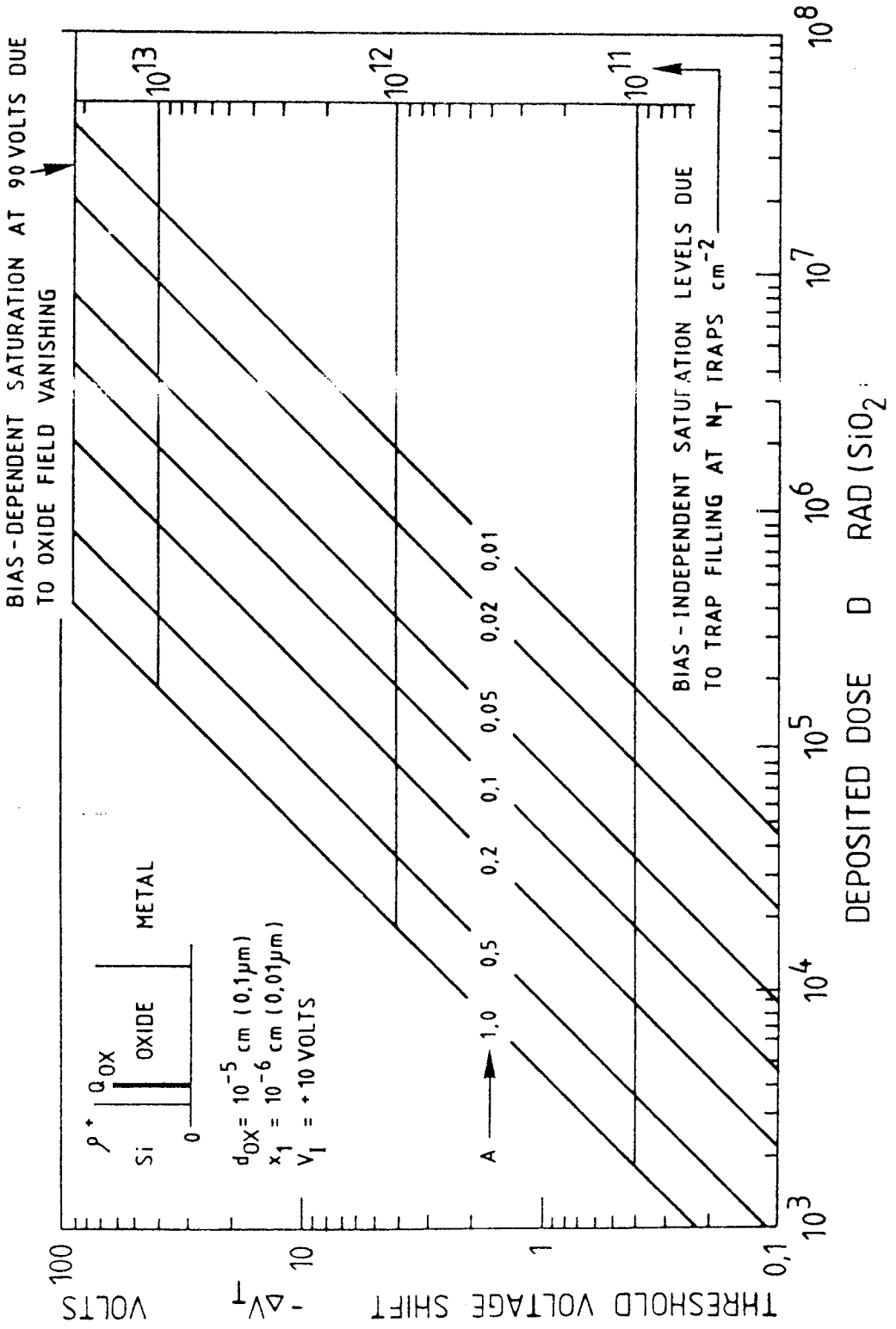
Simple model of threshold shift as a function of dose for several values of positive irradiation bias, with trapping probability equal to unity.

FIGURE 6.10 - ENGINEERING GROWTH CURVES



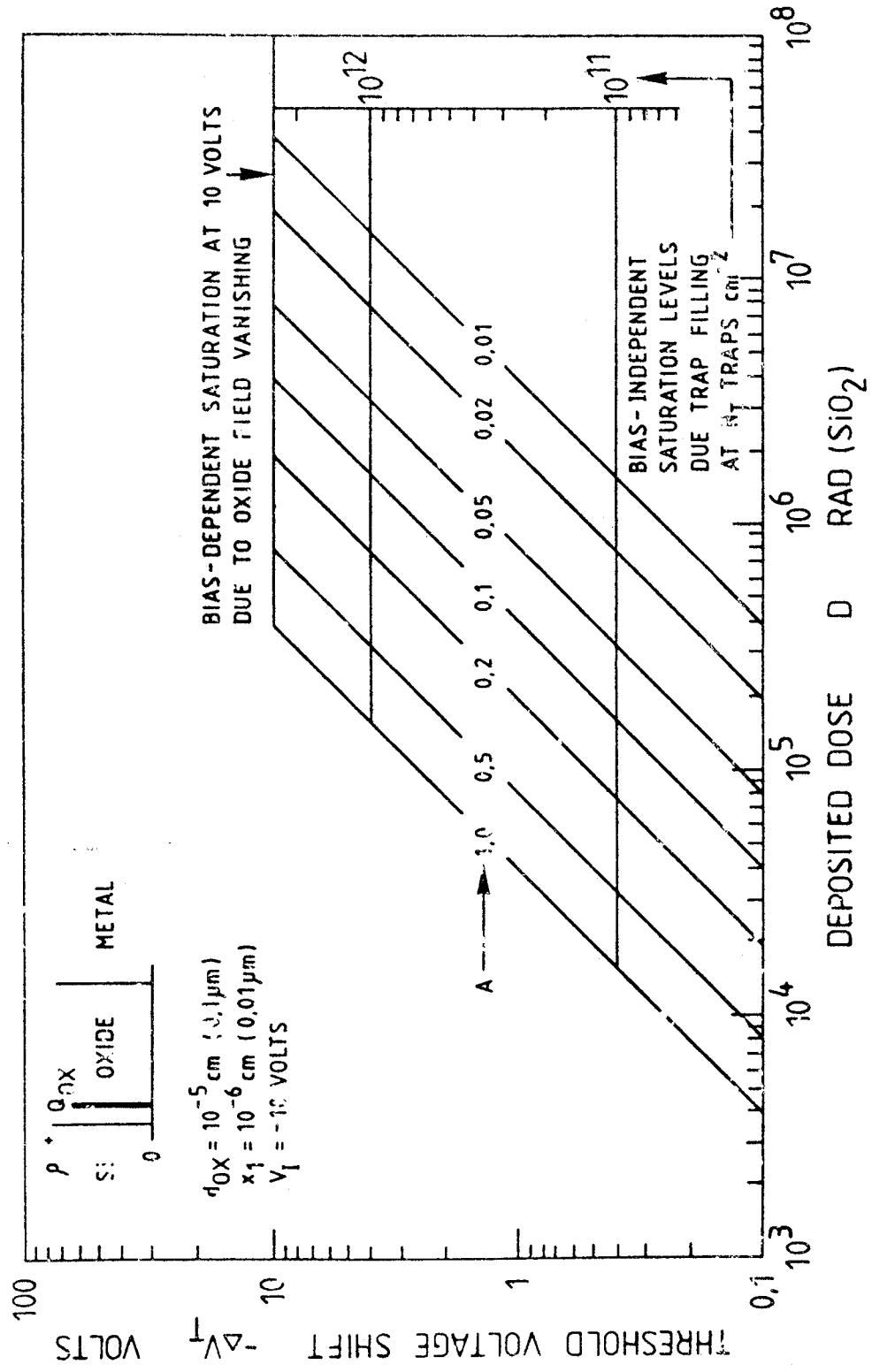
Simple model of threshold shift as a function of dose for several values of negative irradiation bias, with trapping probability equal to unity.

FIGURE 6.11 - ENGINEERING GROWTH CURVES



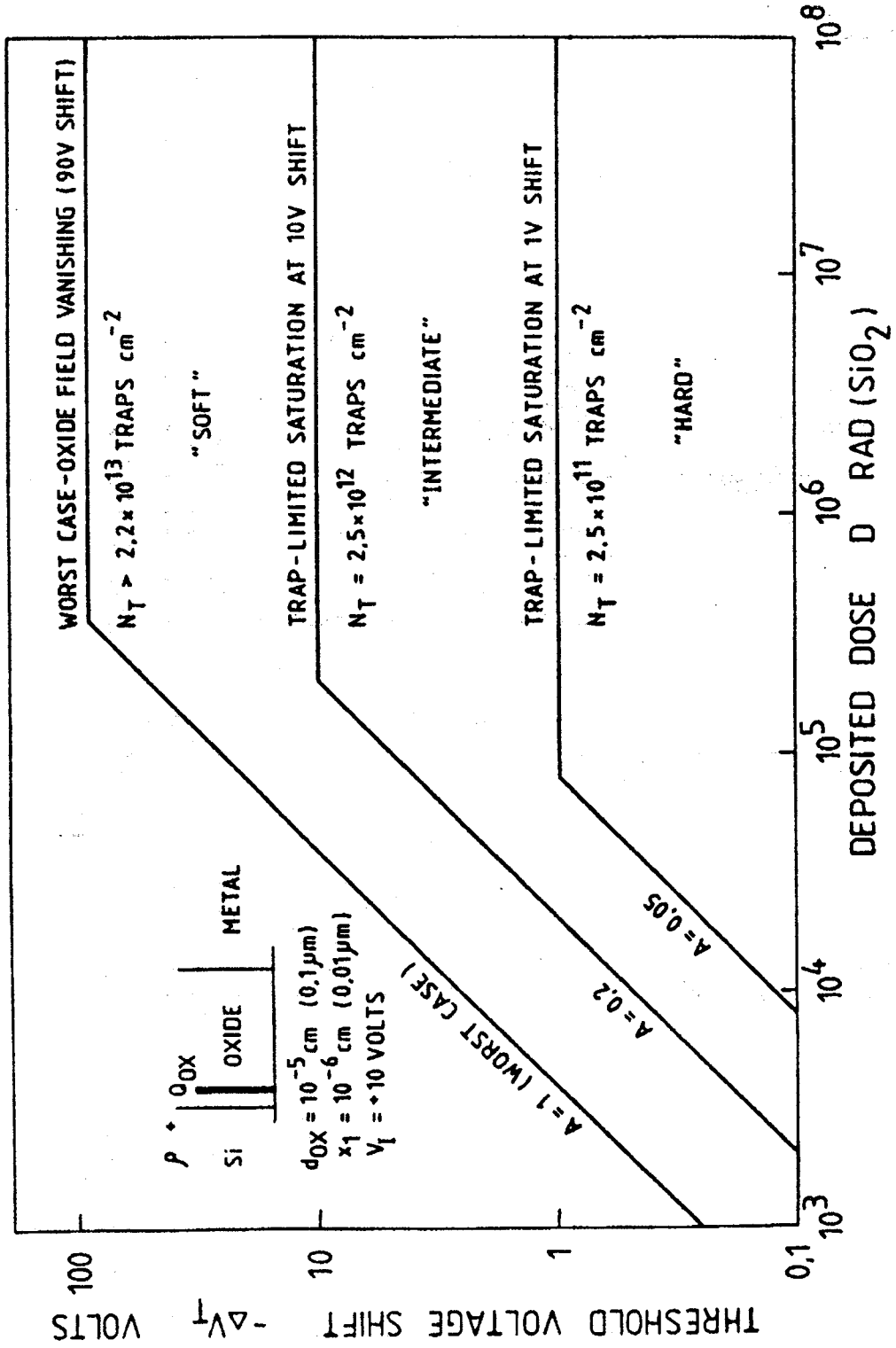
Simple model of threshold shift as a function of dose for several values of trapping probability at +10V bias.

FIGURE 6.12 - ENGINEERING GROWTH CURVES



Simple model of threshold shift as a function of dose for several values of trapping probability at -10V bias.

FIGURE 6.13 - ENGINEERING GROWTH CURVES



The "growth curve" format divided into proposed areas corresponding to the degree of radiation sensitivity. Devices are under +10V irradiation bias with trapped charge sheet as shown.

FIGURE 6.14 - PRACTICAL MOS DEGRADATION MODEL

6.5. LATE EFFECTS

6.5.1. High-temperature annealing

Early in the investigation of hole-trapping in MOS systems, it was discovered that the trapped charge could be removed ("annealed") without trace by heating the device to a temperature near 300°C.

The "irradiate-anneal" cycle could be repeated many times with little alteration. However, these results were puzzling because they conflicted with the evidence from physics experiments which pointed to a high activation energy required for the trapping of holes. The exact mechanism of thermal annealing has not been established, but Danchenko and colleagues (1968) have proposed that the effect is brought about by electrons being injected into the Si-SiO_2 interface from the silicon. Figure 6.15 shows a comparison between Danchenko's results and some by Holmes-Siedle and Groombridge of irradiation of MOS capacitors with X-rays and V-UV light. Also shown are results by the same authors of the annealing of the interface states.

6.5.2. Room-temperature annealing

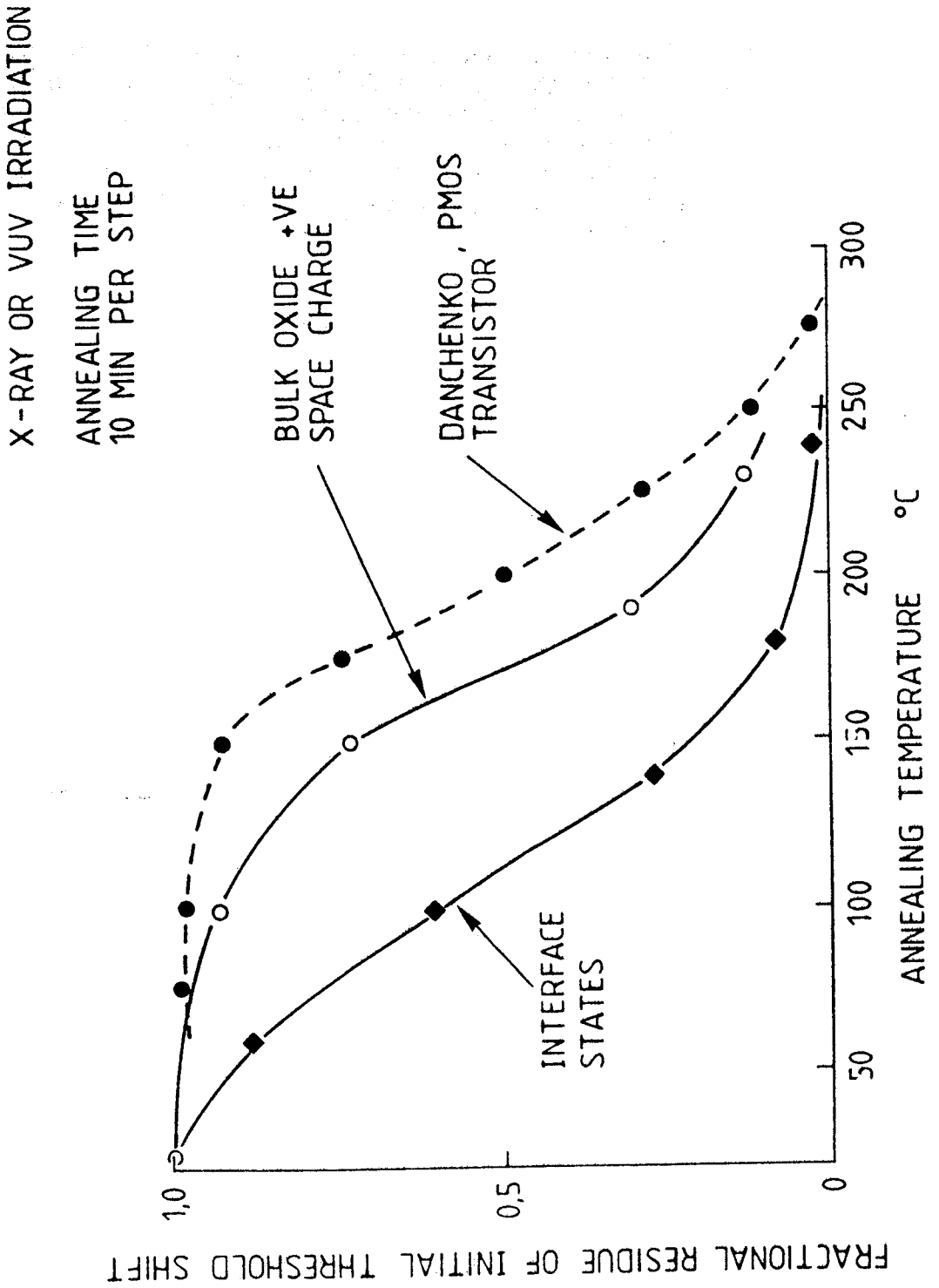
6.5.2.1. General

The rate of relaxation of the charge trapped in MOS structures is extremely variable, as is demonstrated by the spread of effects shown in Figure 6.16 (Winokur et al, 1983). Simple CMOS inverters from five different manufacturers were irradiated fairly rapidly and then observed for the next 10^6 seconds (about 11 days). Some n-channel devices had recovered less than 10%; others had undergone a large recovery, with V_T even overshooting the original value (this is known as "rebound"). The p-channel transistors are seen to be degrading further with time ("reverse annealing").

6.5.2.2. Prediction model

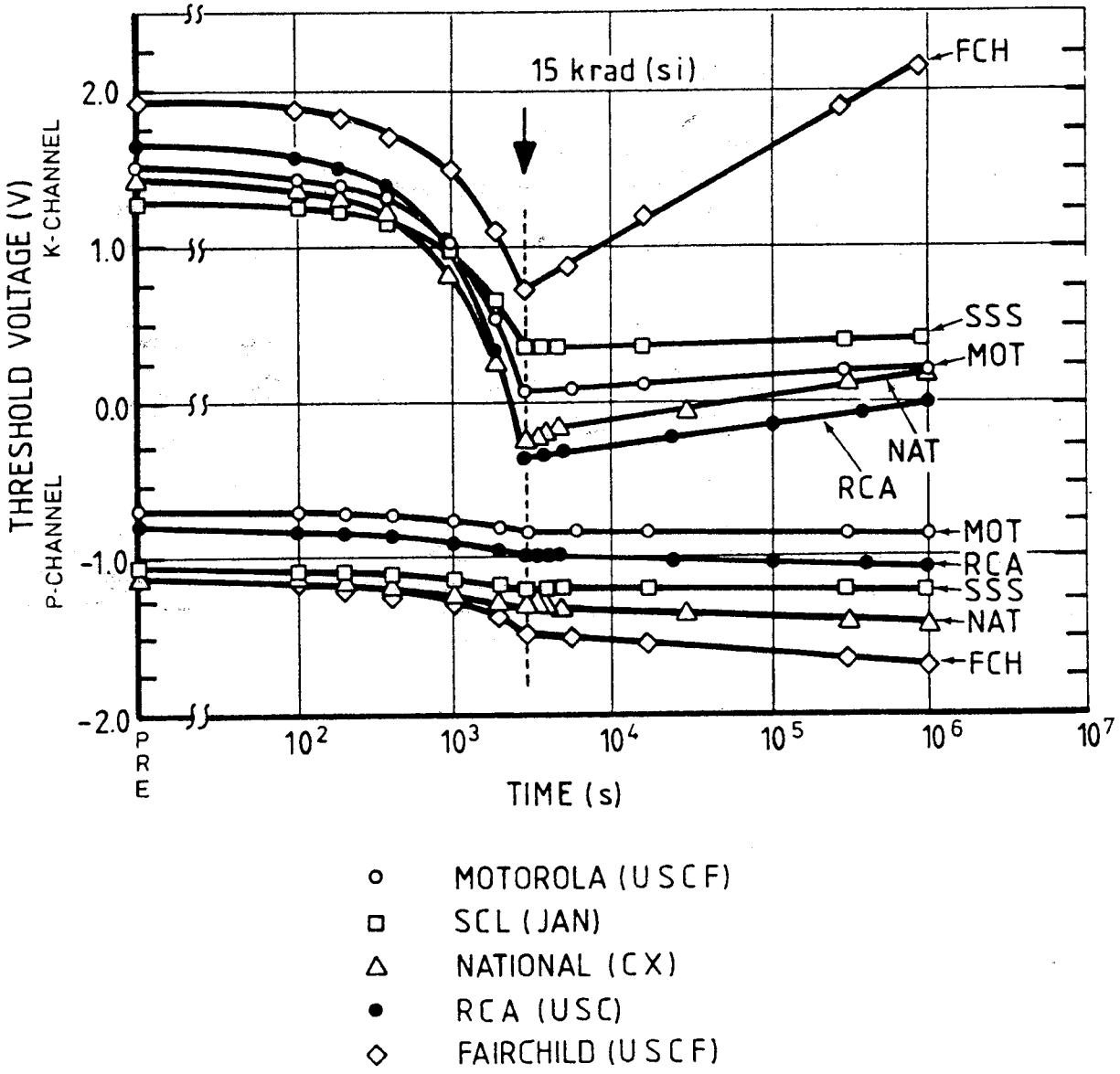
Winokur (1983) has produced an analysis of the above recovery effects which is useful for spacecraft design because it allows us to perform tests in a reasonably short time and to extrapolate the results to long times, say, several years in space. By the use of simple linear system theory, a mathematical value - the "annealing slope" - is extracted from the test data. A high slope value implies a rapid recovery characteristic in the laboratory test and predicts a milder degradation in space at low dose rates. If this technique is used in projects, caution has to be exercised in device selection because the same manufacturer may produce batches with different recovery characteristics.

Brucker (1982) and Holmes-Siedle and Adams (1985) have found that p-channel devices are often slower to recover than n-channel ones. Also, interface effects can cause p-channel threshold voltage shifts to become even larger as time progresses. In a 10-year study of ultra-soft p-channel devices used as space radiation dosimeters, a typical recovery over 10 years was between zero and 20%.



Experimental results showing the fractional residue of radiation-induced threshold shift as a function of isochronal annealing temperature.

FIGURE 6.15 - THERMAL ANNEALING OF THRESHOLD VOLTAGE SHIFT



Threshold voltage curves for n- and p-channels of commercial 4007 inverters both during and following a 5-rad(Si)/s ^{60}Co irradiation. Dashed vertical line at 3000 s denotes end of irradiation. (Winokur 1983).

FIGURE 6.16 - THRESHOLD VOLTAGE CURVES FOR N- AND P-CHANNELS

To illustrate the wide variety of possible annealing rates, Figure 6.17 shows some of the results quoted above compared in terms of fractional recovery with log (time). The annealing curves are straight lines on this scale and slopes vary from 3 to 25% per decade of time. Also shown on this chart are p-channel devices exhibiting increased degradation with time (curve 'd'). Both this "reverse annealing" effect and the "rebound" of n-channel devices, mentioned earlier, are explained by the build-up of new interface states with time. See for example Oldham (1984); Schwank et al (1983).

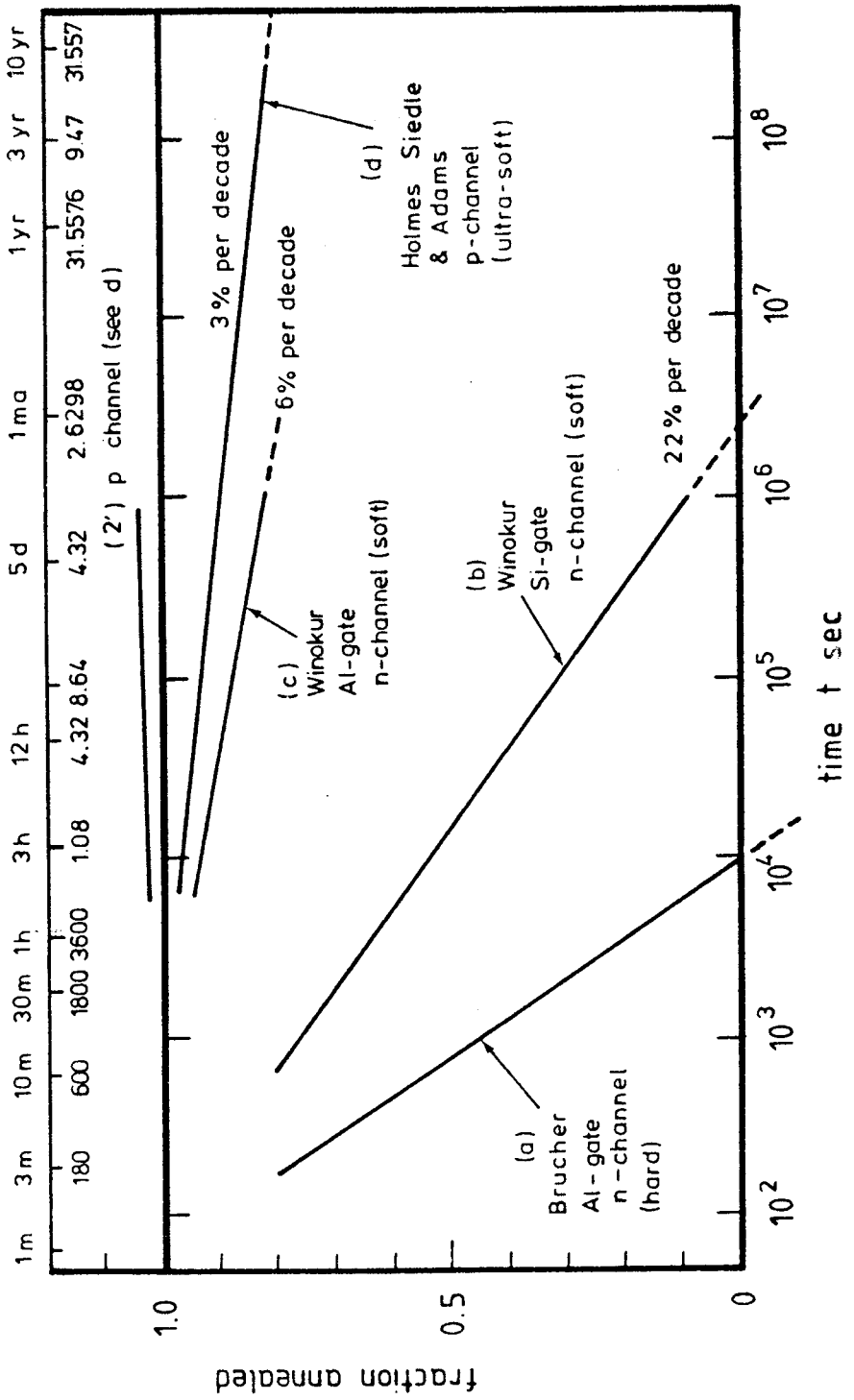
A NASA-sponsored group of investigators (Brucker et al, 1982, 1983; Stassinopoulos et al, 1983, 1984; Danchenko et al, 1968, 1980, 1981) have made extensive studies of late irradiation effects in MOS devices. This work included a detailed investigation into the relative effects of electrons, protons and gamma radiation on a uniform batch of CMOS inverters of the 4007 type. This batch, containing a fairly "soft" type of oxide, exhibited recoveries of V_T shift in the region of 35% in a year. Particle type had some influence on the mode of recovery.

6.5.3. NASA/JPL workshop on "post-irradiation effects"

6.5.3.1 General

Sponsored by NASA, Jet Propulsion Laboratories, Pasadena, USA, held a workshop on "Post-irradiation Effects" in 1983 to assess the impact of room temperature annealing on spacecraft project engineering work such as device and radiation testing specifications. The physics of room temperature annealing is only partly understood, but sufficient testing has been done to enable an approximate mathematical model to be developed for the main recovery effects. If further work proves this model to be reliable, we may be able in due course to apply "annealing coefficients" to devices which are to be operated in space at a very low rate. The workshop discussed these questions with a view to evolving proper methods for handling the recovery and rebound effects in the development of aerospace devices and equipment. Some of the panel's conclusions are given in the following section.

The terms "Late radiation effects" or "Post irradiation effects" are to be preferred to "Room temperature annealing". The latter term implies heating and recovery while irradiated MOS devices may degrade further with time at room temperature or below. The term 'late radiation effects' is already used in medicine.



Typical post-irradiation changes in MOS devices as a function of log (time) at room temperature. Trapped charge in the oxide may relax rapidly, especially in "hard" n-channel transistors (a), or very slowly as in the ultra-soft (dosimeter) devices shown in (d). (b) and (c) are examples from an analysis of CMOS devices by Winokur (1983).

FIGURE 6.17 - ROOM TEMPERATURE ANNEALING

One objective of the workshop was to identify the key problem of Late Radiation Effects (L.R.E.) as they vary in detail with the semiconductor device technology in question. While the nature of the mechanisms had to be borne in mind as a unifying factor, the key issue was how best to characterise various technologies with respect to late radiation effects. This may involve research into the improved measurement of device parameters as well as into the development of new sample preparation and irradiation procedures.

6.5.3.2. Technology

The major problems caused by Late Radiation Effects (L.R.E.) derive from the complexity of integrated circuits (ICs) and the multi-function nature of the "anneal" which can include reverse-annealing and rebound effects. As a result, in large-scale ICs, a loss of functionality is sometimes found to occur later. This effect is difficult to predict on a mechanistic basis because of the highly complex relations between IC functionality and the drift of device parameters. The effect is also technology dependent. The IC technologies most significantly affected are:

- CMOS MSI to VLSI,
- NMOS LSI to VLSI,
- Bipolar VHSIC,
- Bipolar analogue.

It is predictable that recessed-oxide technology (e.g. LOCMOS) will introduce several new degradation modes which may contribute to L.R.E.

Other structures in which L.R.E. problems may be expected are:

- GaAs devices (neutron effects) and
- Power MOS devices.

6.5.3.3. Parameters affected

Serious drifts in device parameters with time in the 1 minute to 1 year time-frame include the following:

(a) For a wide range of technologies, the following apply:
  - recovery and overshoot of V_{TN} with time,
  - continued degradation of V_{TP} with time,
  - continued degradation of transconductance or gain with time,
  - continued increase of junction reverse leakages with time,
  - continued build-up of field-oxide inversion paths with time,
  - recovery in propagation delay.

(b) For a limited range of technologies, the following also apply:
- late changes in MOS transistor edge effects (CMOS-SOS),
- the loading of on-chip VBB generators by leakage paths (NMOS),
- tub-to-tub leakage (VHSIC-bipolar ICs),
- nonuniform charge rearrangement on source drain axis during post-irradiation cycling (short-channel devices),
- the reverse annealing of h_{FE} (bipolar analogue),
- degradation of power MOS devices,
- rapid recovery in bit error rates vs time.

6.5.3.4. Measurement technique

As IC elements become smaller, the need to expand the range of device parameters measured becomes urgent (e.g. the conventional meaning of "threshold voltage" becomes too vague). Also, as IC complexity increases, more complex functional parameters (e.g. "shmoo" plots) must be followed as a function of time after irradiation. Therefore, we must attempt to define new post-irradiation measurement procedures for ICs which are appropriately sensitive to post-irradiation drifts and which will permit considerably improved predictions of the drift of IC performance parameters with time. Typical parameters to be considered in new post-irradiation measurement procedures are:

- the minimum operating voltage (V_{DD} (min)) of an IC,
- the "shmoo" plots for an IC,
- effective surface mobility of a transistor channel,
- the "bipolar snap-back" effect in MOS IC's,
- the charge-pumping currents of a transistor.

6.5.3.5. Acceleration techniques

It is possible that accelerated ageing techniques will be combined with improved parameter measurement to improve the accuracy of long-term performance prediction. Research is warranted, especially into the exploitation of modern burn-in techniques and the validity of elevated temperature post-irradiation treatments of various technologies.

6.5.3.6. Use of test patterns

The use of technology test patterns in radiation evaluation will solve some problems in late radiation effects (especially the statistics of failure). In some cases, the adoption of a test-chip evaluation programme by a spacecraft system contractor could allow that contractor to relax the radiation-effect design margins used in system design and, hence, lead to a reduction of the shield weight associated with the design.

The test patterns should include both (a) simple structures such as capacitors and ring-dot transistors and (b) complex networks as appropriate such as logic string, ring oscillators and memory cells.

6.5.4. Annealing of cryogenic devices

MOS devices irradiated at cryogenic temperatures exhibit larger radiation-induced shifts than those irradiated at room temperature. More charge is trapped in the oxide at low temperature, although much of the excess is removed if the device is warmed to room temperature. Boesch and co-workers (1976) have characterised this process.

6.6. DOSE RATE EFFECTS

It has been explained earlier that if a MOS device is prone to "room temperature annealing", then the radiation-induced shift of V_T will be affected by the dose rate used, so long as the shifts are measured immediately after irradiation. It has also been explained that this is not a true dose-rate effect, but the effect of concurrent processes of charge build-up and charge-trapping. Winokur's recent work shows that if allowance is made for the latter factors in the calculation of end-of-life state of the device, the dose rate used in gamma irradiations can be varied between a few rads per hour and thousands of rads per second without affecting the end result many days after irradiation has ceased. In other words, no fundamentally different physical processes occur during accelerated testing compared with the slow rate expected in space.

6.7. OTHER EFFECTS IN MOS DEVICES

6.7.1. Interface states

The effects of radiation-induced states on MOS devices are strong, especially in high-technology IC's having thin gate oxides. The main effects are:

(a) lowering of transconductance,

(b) distortion of I_D-V_G characteristics,

(c) generation of "slow states" and a resulting slow drift of V_T with time (Holmes-Siedle and Adams, 1983).

Effects (a) and (b) have been incorporated in the simple models discussed earlier.

6.7.2. Atomic displacement damage

Transport of carriers in the channel of an MOS device is by majority carrier conduction. The effect of atomic displacement damage on this transport is slight at the levels likely in space and any such changes are almost certain to be swamped by the oxide and interface effects already described. The conduction of majority carriers in the channel of an MOS device is lower than that in bulk silicon due to collisions with interface states. Changes in transconductance of the channel, owing to the ionisation-induced build-up of interface states would therefore be expected to overshadow the effects of changes in resistivity caused by displacement damage in the silicon itself. (Note that this change in transconductance is illustrated by the distortion of the I_D-V_G curves in Figure 6.3(a).

Even though displacement damage will not be a significant factor in the space environment, it is worth while to note very briefly the factors that affect the resistivity of bulk silicon. The resistivity, ρ, of bulk silicon is controlled by majority carrier mobility, μ, (which, in turn, is controlled by the number of centres in the silicon that scatter majority carriers) and by the carrier concentration, N_O.

$$N_o = \frac{1}{q\, N_o} \qquad \text{..... 6(ii)}$$

where q is the charge on the electron.

Defects produced by atomic displacement can reduce the carrier concentration, N_O, by trapping. This effect is called "carrier removal" and is proportional to radiation fluence. Thus, carrier concentration after irradiation, $N\phi$, is given by:

$$N_\phi = N_o - \phi \frac{\Delta n}{\Delta \phi} \qquad \text{.....6 (iii)}$$

'where $\Delta_n/\Delta\emptyset$ (for n-type) or $\Delta\rho/\Delta\emptyset$ (for p-type) is termed the "carrier removal rate".

Table 6(3) shows some experimental values for electrons, protons and neutrons. For the silicon of a typical n-channel MOS device, for which N will be about 10^{16} cm^{-3}, it is clear that the effect of 10^{15} damage-equivalent 1 MeV electrons will be a change of only a few percent in concentration.

Damage in most operational orbits is much lower than this (see Section 7.10) and, even at the peak of the proton belt, will not be over 10^{16} damage-equivalent 1 MeV electrons.cm^{-2} per year behind 1 g.cm^{-2} aluminium. At geostationary altitude, because of

the virtual absence of protons, bulk damage rates are completely negligible within the spacecraft.

Concerning changes in the mobility term in equation 6(iii) caused by increased scattering of majority carriers by displacement defects, Gregory (1973) shows that this change would be only a few percent at a neutron fluence of 10^{14} cm^{-2}. This fluence is equivalent to over 10^{15} 1-MeV electrons cm^{-2}. As indicated above, damage in most operational orbits will be much lower than this.

TABLE 6(3) - CARRIER REMOVAL RATES ($\Delta n/\Delta\phi$) FOR 1-OHM CM SILICON UNDER PARTICLE IRRADIATION

Particle	Energy (MeV)	Carrier removal rate (cm^{-1})				Ref.
		$\Delta n/\Delta\phi$		$\Delta n/\Delta\phi$		
		Cz	Fz	Cz	Fz	
Electrons	1.7	0.31	1.3	0.2	0.2	55
Protons	4.5 - 207	1000	1000	1000	1000	56
Neutrons	0.01	6	9	13	13	55

Cz = Czochralski crystal growth method
FZ = Float-zone refined crystal
Removal rates for protons are approximate

6.8. COMMERCIAL AND HARDENED MOS DEVICES

6.8.1. Processing variables

The key to the radiation sensitivity of MOS devices lies in the preparation of the gate insulator layer, at present invariably grown by various methods of thermal oxidation of the silicon wafer. As explained in Section 6.4, this sensitivity varies with the concentration of hole-traps in this layer and, although research has been intensive, there is still controversy about:

- the exact structure of the hole-trapping defects,
- the exact mechanism of their generation during growth and annealing of the oxide and
- the best methods of controlling their generation.

The important point is that, apparently, small variations in growth temperature, annealing temperature, subsequent metallisation, silicon quality and cleanliness, and oxidation ambient, can make a large difference in hole-trap concentration. Although considerable attention is paid to these "process parameters" in commercial MOS devices, it still appears that the control exercised is often not close enough to maintain a uniform level of radiation sensitivity. V_T shifts for a given dose vary from unit to unit and from batch to batch, giving a serious problem of "scatter".

For a cost-conscious small purchaser of devices, such as a space equipment manufacturer, a still more unfortunate fact is that the MOS process parameters chosen by manufacturers on grounds of profitability are well removed from those which produce low radiation sensitivity. For example, while the current "recipe" for the

best tolerance to radiation calls for such features as slow oxide growth to limited thickness in specially purged dry oxygen furnaces at low temperature, low temperature anneal, deposition of metal without electron beam heating and "tailoring" for high V_T, commercial LSI circuits are often made to a recipe which includes fast oxide growth in non-purged furnaces (for high throughput), thicker oxides (for fewer pinhole defects), silicon gate electrodes (for self-alignment and low V_T) and high temperature anneal (for low V_T and high yield).

Furthermore, competition in the area of switching speed causes the manufacturer to "tailor" V_T to as low a value as possible. While a high-reliability LSI integrated circuit can be easily produced to the first recipe, few manufacturers offer such a device as a commercial product.

Thus, the problem of high and varying sensitivity of commercial devices to total dose may remain for some time. It must be circumvented by a mixture of pre-selection, batch monitoring, protection of components from the external environment and the procurement of special alterations, by the manufacturer, of his process.

6.8.2. Memory technology

For data storage in spacecraft, it is likely that CMOS static RAM's will be the most widely used form of semiconductor memory. First, the static memory configuration is less prone to upset than the dynamic form; second, the low power drain of the CMOS form not only suits the power requirements of the spacecraft, but the drain is so low that a small emergency battery can be used to maintain data if the main spacecraft power fails. The main advantage of the NMOS dynamic memory in the commercial field is very high information-storage density. In spacecraft circuitry, the greatest value is placed on process reliability and tolerance to noise and various radiation effects. CMOS circuitry is preferable in most of these respects so long as "latchup" effects are suppressed. The information density of CMOS devices may have to be limited for space because, at high bit densities, single-event upsets may become too frequent unless specialised measures are taken.

6.8.3. Microprocessor technology

6.8.3.1. General

Data processing and control functions in spacecraft will employ microprocessors distributed throughout the equipment. As with memories, CMOS devices are preferable to NMOS and bipolar forms. However, several relevant differences between memories and microprocessors may also be stated. First, the radiation-

induced power drain due to a few microprocessors is of less importance than that due to a large array of memories.

Second, it is simpler to apply local shielding to single microprocessor chips achieved than to arrays of memories. The choice of microprocessor for radiation environments will rest on total dose functional tolerance and the proneness of the system to errors induced by cosmic rays and other disturbances.

6.8.3.2. Hardened technology

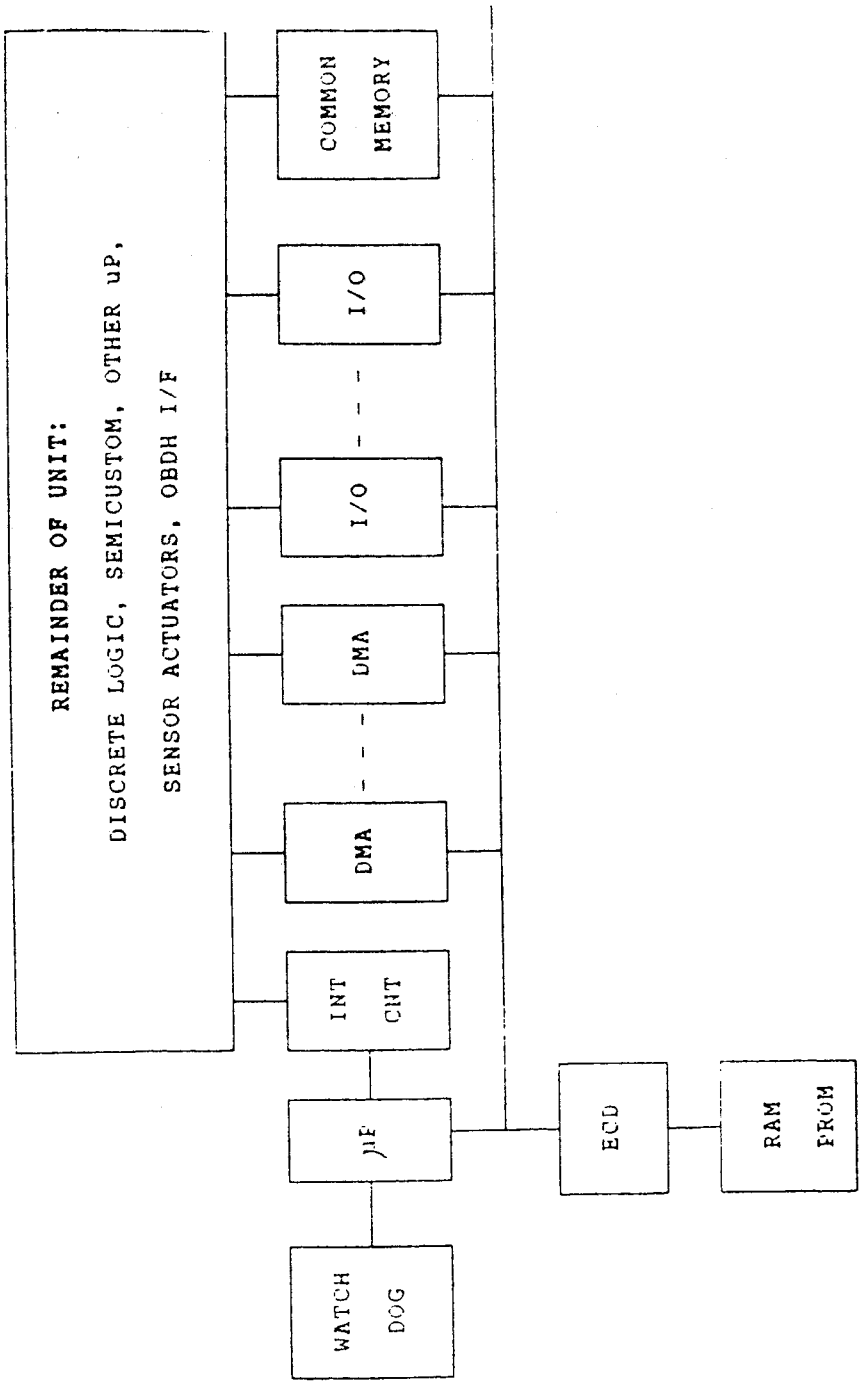
One example of a hardened microprocessor is the 8-bit 80C85RH. This is a hardened CMOS version of the Intel 8085 NMOS microprocessor. It was developed by Sandia National Laboratories and is being marketed in Europe. The 80C85RH offers a functional copy of the NMOS 8085 and is fully software compatible. Power reduction of 90% is claimed and the microprocessor and its peripheral devices have a power supply operation range of 4.5 to 11V. Total dose hardness levels of 10^6 rad (Si) have been recorded on tests.

Latchup-free operation is obtained by the use of an epitaxial substrate as the starting material in the fabrication process. For further reduction in power consumption, the microprocessor clock may be stopped without loss of data because the memory devices are fully static. The peripheral devices include a 256 x 8 RAM, a 2k x 8 ROM, an I/O decoder, a level converter, a bus transceiver and an I/O port.

Further hardened technologies now becoming available in Europe are based on silicon-on-sapphire technology and cover semi-custom gate array and cell-based design as well as Random Access Memories up to 64 Kbits. The SOS technology is extremely hard to total-dose (hundreds of kilorads) as well as being latchup-free and immune to SEU.

6.8.4. Spacecraft system technology

An example of the practical use of MOS memories and microprocessors in complex systems is available in ESA's On-Board Data Handling (OBDH) programme. Figures 6.18 to 6.20 (Walker, 1985) show some aspects of the organisation of this system and the complexity of radiation effects involved. The requirement for tolerance to radiation in this system has given rise to ESA Applied Research Programmes in the radiation-hardening of European MOS technology.



Key

P = Microprocessor
INT CNT = Interrupt Controller
DMA = Direct Memory Access
I/O = Input/Output
I/ED = Interfaces
ICD = Error Correction and Detection

Examples of above

Central Terminal Unit
Intelligent Remote Terminal Unit
On-board Computer
Mass Memory Controller
Sensor Electronics
Attitude Control System

FIGURE 6.18 - TYPICAL FORM OF MICROPROCESSOR - CONTROLLED SPACECRAFT SUBSYSTEM

Device/ character-istics	In orbit as of 1985	Forefront devices 1985	Future	System implications
Micropro-cessors	Various 8-bit µ P's	8086, etc.	80 C 86, 1750, 31750, 80386	-Increasing use of UP + large capaci-ty memory through-put SIC units. -Increasing decisi-on-making capabi-lity on-board. -Possibility for more autonomy for mission manage-ment, adaptive control and crisis management.
Memories	1 K RAM	16 K RAM	25 K RAM	
Logic	Lp TTL (CMOS)	Lp STTL, CMOS	ALS, CMOS, HCMOS	MOS technology increasing
Periphe-rals	–	– DM INT.	AC CONT., etc.	Hardening by design, if possible.
Semi-custom	–	Circa 5%	Increasing	
Geometry	–	Circa 3 µm	Decreasing	More bit errors
Total rad-iation dose -Majority	2 - 5 K rad	1-12 K rad 20-50 K rad	Increasing	Prediction, test and quality control are problems.
-Special MOS parts	–			
Single events Upsets	–	Several events/day	More events per day	
Testability	–	100%	Unknown	

FIGURE 6.19 - TRENDS OF IN-USE DIGITAL DEVICES ON SPACECRAFT: SYSTEM IMPLICATIONS

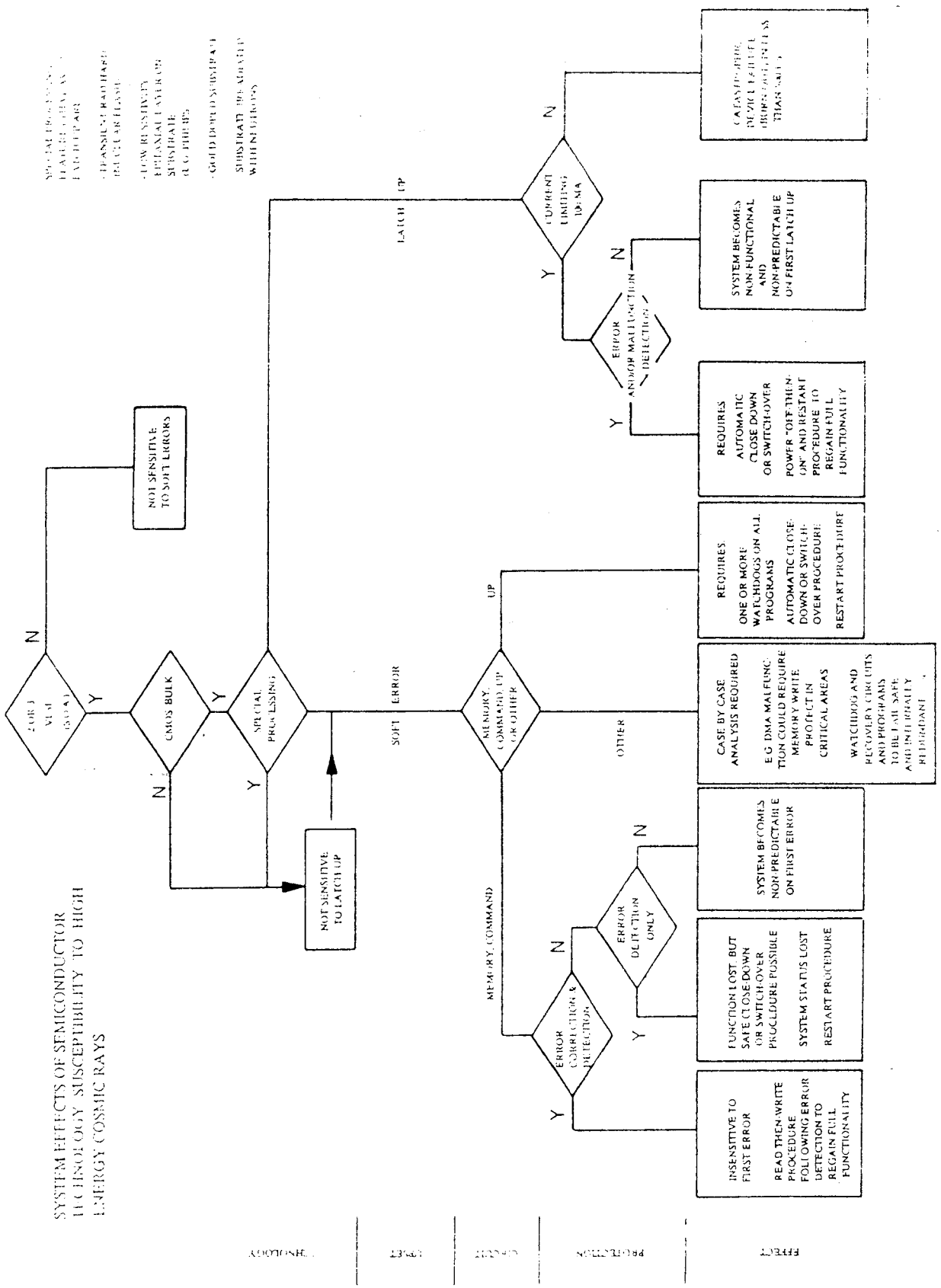


FIGURE 6.20 - SYSTEM IMPLICATIONS OF COSMIC RAY EFFECTS (E > 1000 MeV) FOR DIGITAL TECHNOLOGY

6.9. COMPILATION OF RADIATION DATA

The radiation test data for commercial MOS devices are available, but too voluminous for inclusion. Data banks have been established for the collection and dissemination of such data. These include:

- ESA Radiation Effects Data Base (includes total dose and single event upset data on a wide range of devices,
- Hahn-Meitner Institut, Berlin: "Data Compilation of Irradiation Tested Electronic Components", HMI-B353 (loose-leaf Computer-Printed Data Sheets),
- SPIRE Compilation (available through U.K. Ministry of Defence (AWD), London),
- Kaman-Tempo, Santa Barbara, USA (incorporating the data bank initiated by U.S. Army (HDL), Adelphi, MD, USA),
- NASA (available through Product Assurance Group, Goddard Space Flight Center, Greenbelt, MD, USA),
- SPACERAD Compilation (available through Jet Propulsion Laboratory, Pasadena, CA, USA and accessible via DARPANET electronic mail system).

6.10. CONCLUSIONS

This section has dealt extensively with the radiation sensitivity of MOS devices because this class of devices will be used more and more on spacecraft, the types available will become more varied and complex and the radiation sensitivity of some of these components will continue to present an engineering problem. This can still be said despite the appearance of new recipes for "hard" oxides and their adoption for a few commercial device types. This may alleviate the problem in a few cases, but it is predictable that the suppliers of many desirable MOS devices, including NMOS and CMOS LSI circuits, will not choose to employ these recipes. Thus, the overall radiation problem of MOS devices is likely to remain for many years.

This section is an attempt to state the physical problem and to propose practicable methods of classifying and predicting the response of MOS devices from all quarters of the market place. The effect of processing on mass commercial technology should be understood and applied to the practical schemes outlined here for introducing the required overall "hardness" into a system (i.e. a whole piece of equipment). In this way, the designer retains flexibility in his choice of circuits, but can also take advantage of improved processing technology in an unforced manner as and when this technology reaches the required level of acceptability.

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