

Test Plan  
Box No.

- 1 Reference number of Test Plan (3 digits, starting from 001).
- 2 Reference (issue and revision with dates) of the irradiation Test Plan.
- 3 ESCC Component Number.
- 4 Component designation.
- 5 Manufacturer/user Irradiation Test Specification (number, issue, revision).
- 6 Device Family: ESCC Generic and Detail Specifications (number issues and revisions).
- 7 Acceptance Class: Applicable Type of Acceptance (i.e. acceptance of diffusion lot of wafers or procurement lot acceptance).
- 8 Sample size and number of control devices.
- 9 Project or Test Programme requiring this test.
- 10 Component family.
- 11 Component group.
- 12 Device package.
- 13 Manufacturer's name and address.
- 14 Test facility name and address.
- 15 Originator of Test Plan (name and telephone number).
- 16 Name of facility and type of radiation source.
- 17 Type of exposure (single or multiple).
- 18 See Items 22 and 23.
- 19 Level of Interest.
- 20 Single exposure: specification of values at the chip of dose and dose rate (or fluence, flux and duration in the case of particles).
- 21 Multiple exposure: specification of number of exposures, doses and dose rates (or flux and duration of each exposure).
- 22 Irradiation conditions: remote or in situ, biased or unbiased. (Note 1)
- 23 RT Anneal conditions (Note 2):
  - Room temp (°C)
  - Anneal time (hr)
  - Ageing temp. (°C)
  - Ageing time (hr)

- 24 List of electrical parameters to be listed. (Description as per "Electrical Measurements for Total Dose Radiation Testing" of the Detail Specification).
- 25 Irradiation Test Sequence describing each step of each test to be performed and requirements related to these steps.
- 26 Remarks should contain items of special note or importance which should be considered during the test programme, especially the time-dependence of radiation response and the need for accelerated ageing and variation from lot to lot.

**NOTES:**

1. If the device is not biased during any stage, then all leads must be shorted in a conductive medium.
2. A single bias circuit and voltage value shall be used for all of the stages specified here and this shall be the worst case bias except in the case of evaluation testing when bias conditions are being investigated.