ESCCON 2011

European Space Components Conference
ESA ESTEC
(Newton 1 and 2 Conference Rooms)

Final Programme of Wednesday 16-March- 2011
Chairman: R. de Marino, ESA

14:00 – 14:20	The business roadmap. Trends for the future T. Gouvernel, Head of Strategic Business Development, e2v
14:20 – 14:40	In-orbit anomalies due to radiation. Lessons learnt R. Ecoffet, Senior Expert Radiation, CNES
14:40 – 15:00	EEE Parts Procurement for constellations O. Rémondière, Director of Operations Quality Assurance, Thales Alenia Space
15:00 – 15:20	The experience of commercial components insertion in GAIA P. Peres, ASTRIUM Toulouse; A. Gómez, CRISA
15:20 – 15:45	The coordinated procurement of EEE components for ATV M. Veith, Project Manager, TESAT-Spacecom
16:15 – 16:40	ESCC Evaluation and Qualification Programme J. Howley, Enterprise Ireland; G. Joormann, DLR; J. Wong, ESA
16:40 – 17:00	Optoelectronics: risk management of problems encountered A. Bensoussan, Senior Components Expert, Thales Alenia Space Toulouse
17:00 – 17:40	Challenge for advanced payloads: Next generation ASICs, FPGAs and Advanced Conversion components needs (1) and developments (2) (1) L. Baguena, Thales Alenia Space, M. Childerhouse, Astrium; (2) F. Malou and D. Dangla, CNES; L. Hili and D. Merodio, ESA

ESCC

e2v,
The business roadmaps, the trends for future

Thierry Gouvernel, Head of Strategic Business Development
e2v Grenoble
ESCCON 2011, Noordwijk

e2v

e2v is a leading global provider of **technology solutions** for high performance systems;

delivering **solutions, sub-systems and components**, to advanced systems companies, for specialist applications

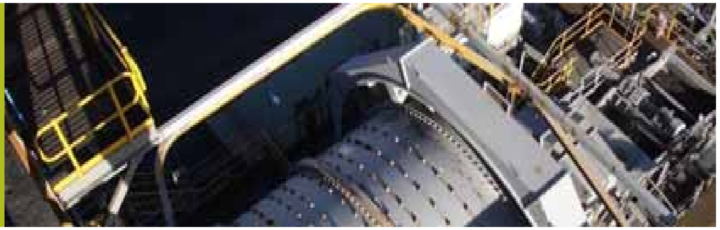
within medical & science, **aerospace & defence**, and commercial & industrial markets.

e2v at a glance

- Founded: 1947
- Annual sales: **$320 million**
- Corporate HQ: Chelmsford, England
- Listed on the London Stock Exchange and FTSE4Good index
- Employees: approx 1500, of whom approximately a third are engineers and scientists
- 6 production facilities: 3 in England, 1 in the US, 1 in France and 1 in Switzerland
- Sales made to over 50 countries

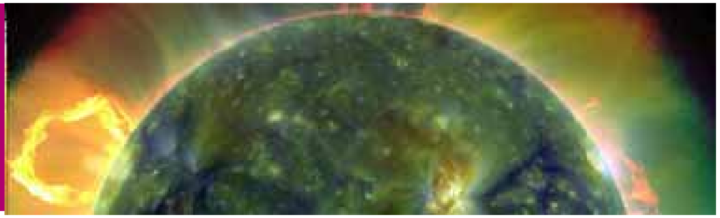
Sales by Division

RF power solutions (tubes)



$105m

High performance Imaging solutions



$86m

Hi-rel semiconductor solutions

$81m

technology solutions for high performance systems

Quality

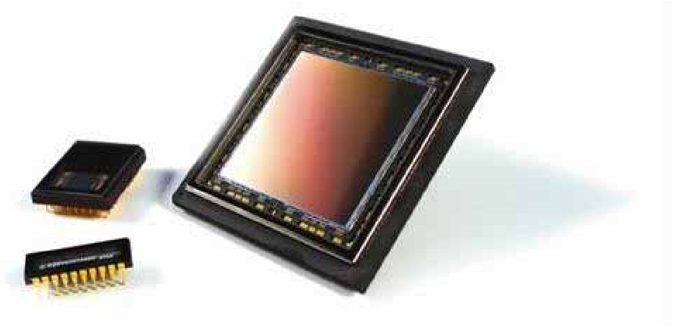
e2v's operational centres are certified to:

- ISO9001:2008
- ISO/TS 16949:2002 (Lincoln and Corcelles automotive products)
- **AS/EN9100** (Grenoble and Santa Clara aerospace semiconductor products)
- **MIL-PRF-38535** custom microcircuit certification (Santa Clara, Grenoble)
- **ESCC** (European Space Components Coordination)
- Environmental Management System (EMS): ISO14001
- BITC environmental index: Gold rating

High performance imaging solutions

High performance imaging solutions for programmes requiring CCD & CMOS sensors and cameras for:

- Space and earth observation imaging
- Science and life science imaging
- Machine vision
- Ophthalmology
- Dental x-ray systems



Imaging / Market segments

Automatic data collection

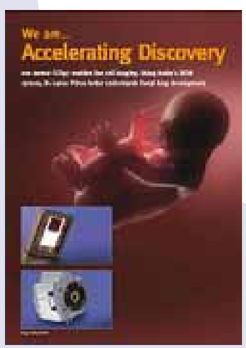
Dental radiography

Ophthalmology

Machine vision

Living planet observation

Land Earth observation



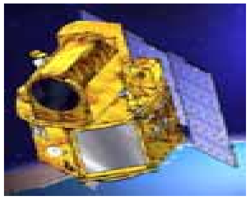
Science

Defence

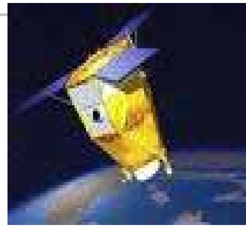
Astronomy & space science

e2v Imaging devices,
Enabling Earth Observation Satellites

e2v



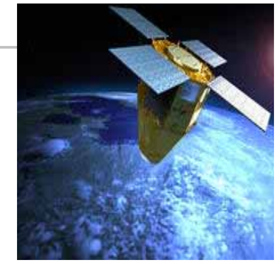
THEOS - Thaïlande



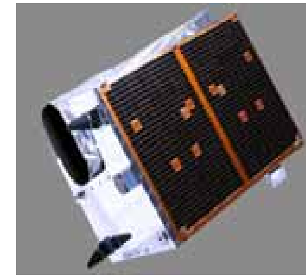
PLEIADES - France

SPOT – France

Helios - CNES - DGA



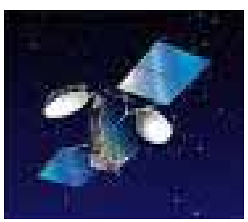
CSO MUSIS - France



RapidEye - Canada

FORMOSAT1 - Taiwan

OFEK – ISRAEL

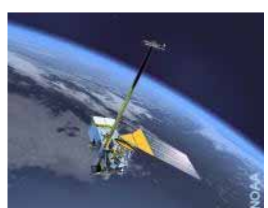


VnredSat1 - Vietnam

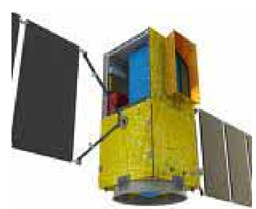
Göktürk- Turkey

ALSAT-2A -Algeria

MAPING – China

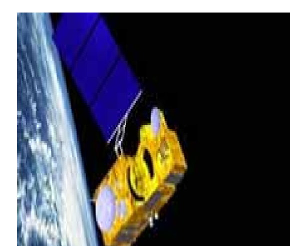


LASP - USA



AMAZONIA - Brazil

GCOM - Japan



SEOSAT - Spain

Imaging Core technology roadmap

Plaform approach to support several markets

e2v

Markets

CCD platforms
- Low noise L3, hiRho, backthinning, 6 inches — 1,5 ML, high speed (2ML) → Astronomy, Scientific, Space Science, Earth Observation, OCT & Machine Vision

CMOS platforms (fabless)
- ***Low noise (L2-CIS)*** 6 e -→ <2 e-, BT, GS,Snapshot pixel → Scientific, Defence, Astronomy, ADCS
- ***High Speed Linear*** Linear, Small pixels, TDI → MV, OCT, Earth Obs.

Subsystems
- Extension of CCD high speed linear , iCMOS → MV, OCT
- CCD Proximity electronics for Space → Astronomy, Space
- Dental IO: extended OS, alignment function, … → Dental

Post-process (fabless)
- coating, BT for external designs → Astronomy, Space Science, Earth Obs.

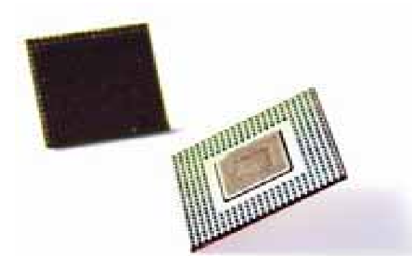
Back-end
- Packaging, test/caraterisation, screening & qualification services → UK: Astronomy, Space Science, Scientific; GNB: MV, Earth Obs.

Hi-rel semiconductor solutions




Hi-rel semiconductor solutions for aerospace & defence programmes requiring:

- Lifecycle management
- Hi-rel microprocessors
- High speed data converters
- High reliability ICs with lifetime continuity of supply
- Assembly & test services
- MRAMs



High-Rel Semiconductors
Applications

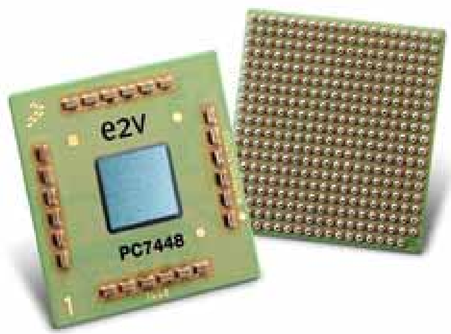
Defense & Aerospace
- Radars
- Electronic warfare
- Counter measures
- Telecom Satellites

Avionics
- Flight computers
- Flight control systems
- Voice data recorders
- Displays
- Engine control

Industrial and Instrumentation
- Down-hole drilling
- Instrumentation : DSO, Data Acquisition
- Scientific : HEP, Radioastronomy

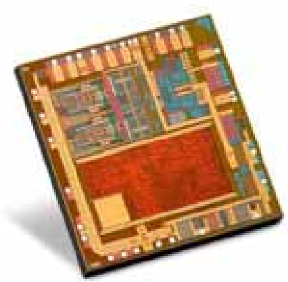
Semiconductor Partner Program

Broadband data converters



Hi-rel Microprocessors

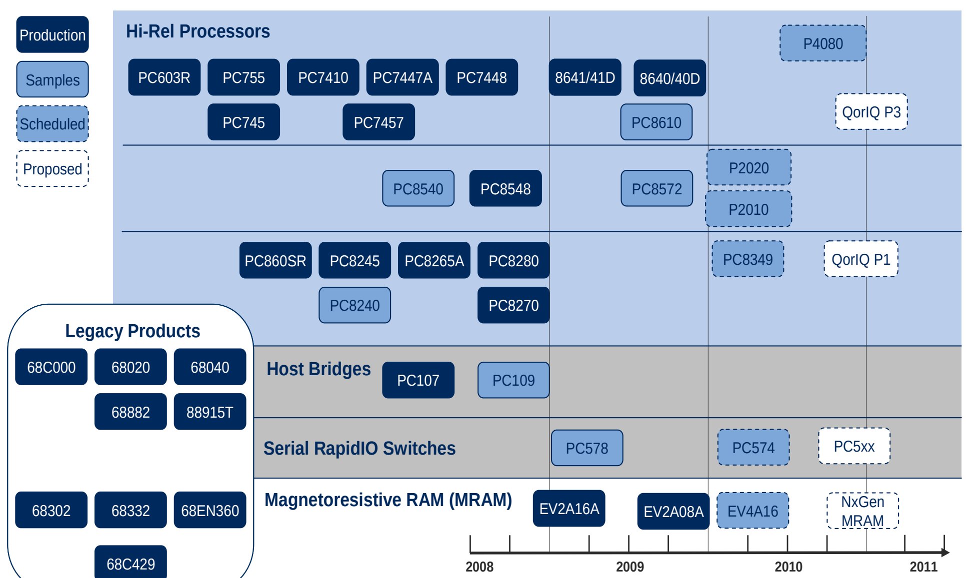
- three decades of hi-rel assembly and test and strategic partnerships
- products sold under e2v brand with full warranty - hi-rel performance guaranteed
- continuity of supply (20 to 30 years) for aerospace and defence OEM's
- market leaders in data converter (ADC / DAC) solutions
- product roadmap with strategic partners



ASICs

MRAMs

High power ISM transceivers

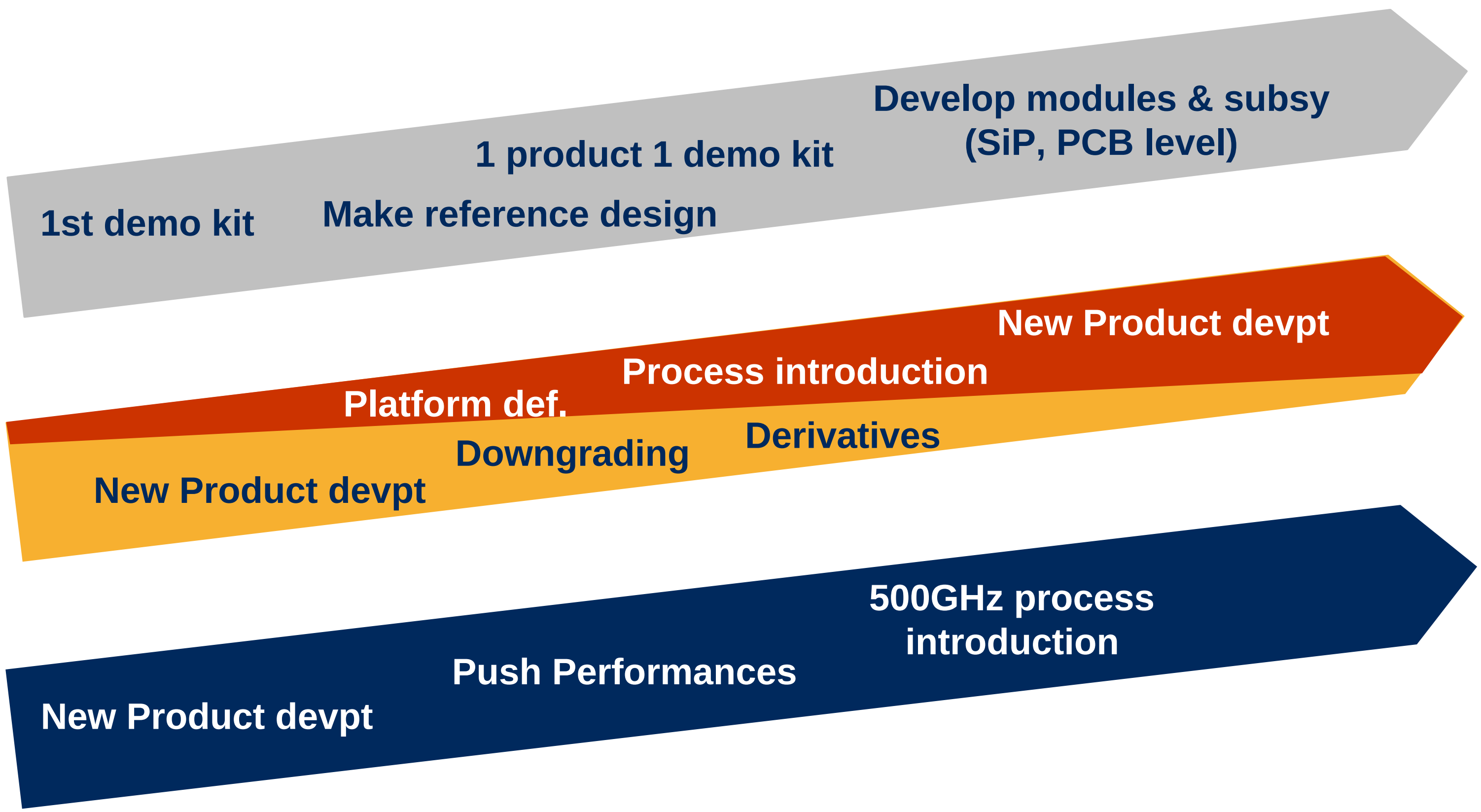


Focus on Data Converters:
Technology platform overview with upcoming steps

Verticalization
Control the BOM
Accelerate
design- in

<u>highly integrated</u>, high perf ADC/ DAC at <u>low power</u>

world class performance ADC/DAC



Ecosystem | CMOS / Advanced BiCMOS | BiCMOS | Bipolar

Data Converters Product Offering
by application's frequencies of operation

S-Band RF Applications

EV10AS150
10bit
2.5GSPS
ADC

EV12DS130
12bit
3GSPS
DAC

L-Band RF Applications

EV10AS180
10bit
1.5GSPS

EV10AQ190
Quad 10bit
5GSPS

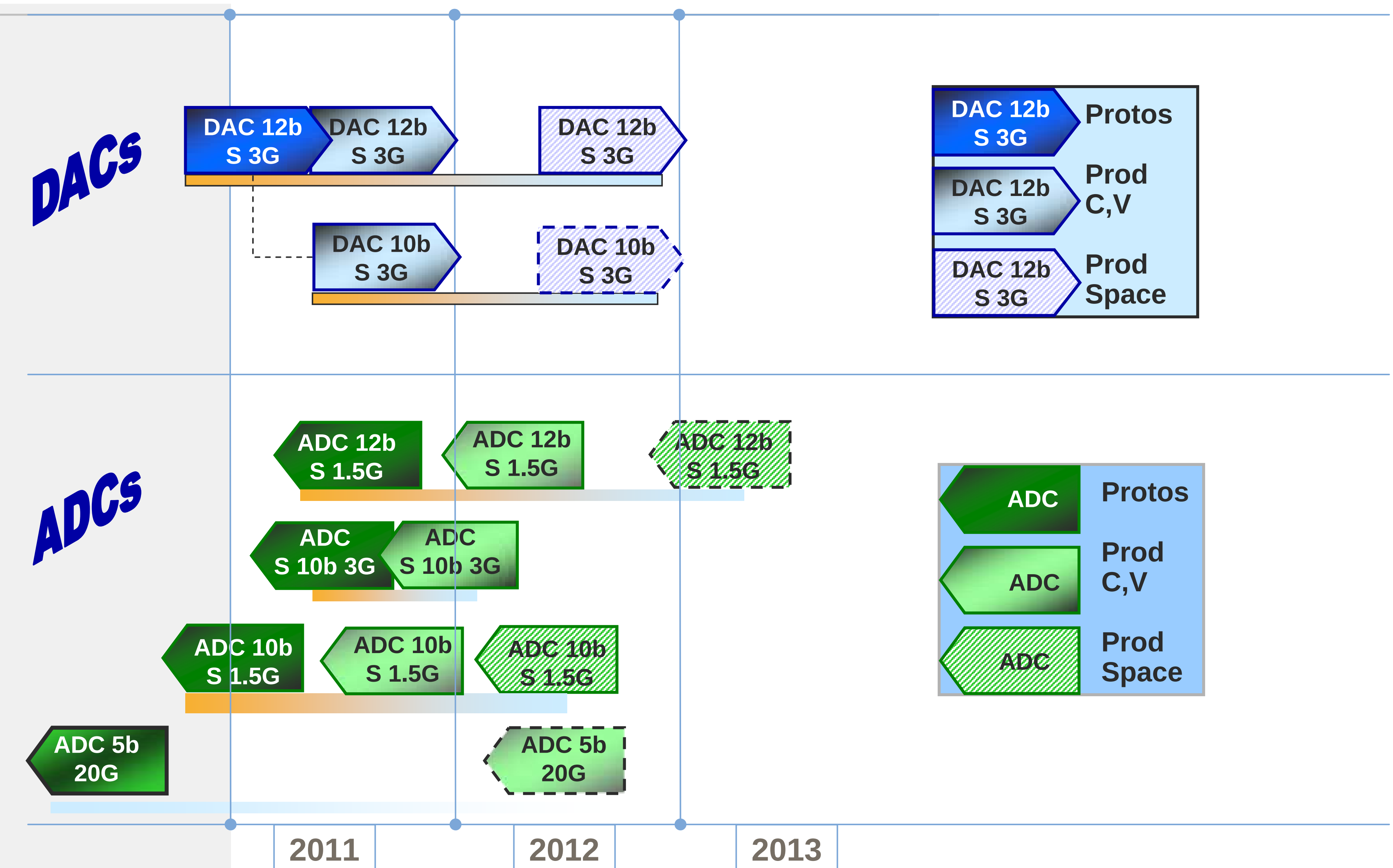
Time Domain Applications

EV8AQ160
Quad 8bit 5GSPS

AT84AD001C
Dual 8bit 1GSPS

Data Converters Roadmap

e2v



Assembly & Test Services

Premier Assembly and Test Services
for high reliability semiconductor products

Largest independent ATH in Europe

Class 100 assembly clean rooms

First in class test equipment

Assembly & Test Services
Grenoble Industrial facilities - Packaging Line

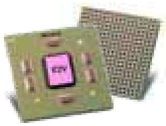
- **Hermetic ceramic packages**

  DIL | CPGA | CQFP | CLCC




- **Flip-Chip packages**

  CBGA | Hi-TCE CBGA

- **High-Rel ICs**

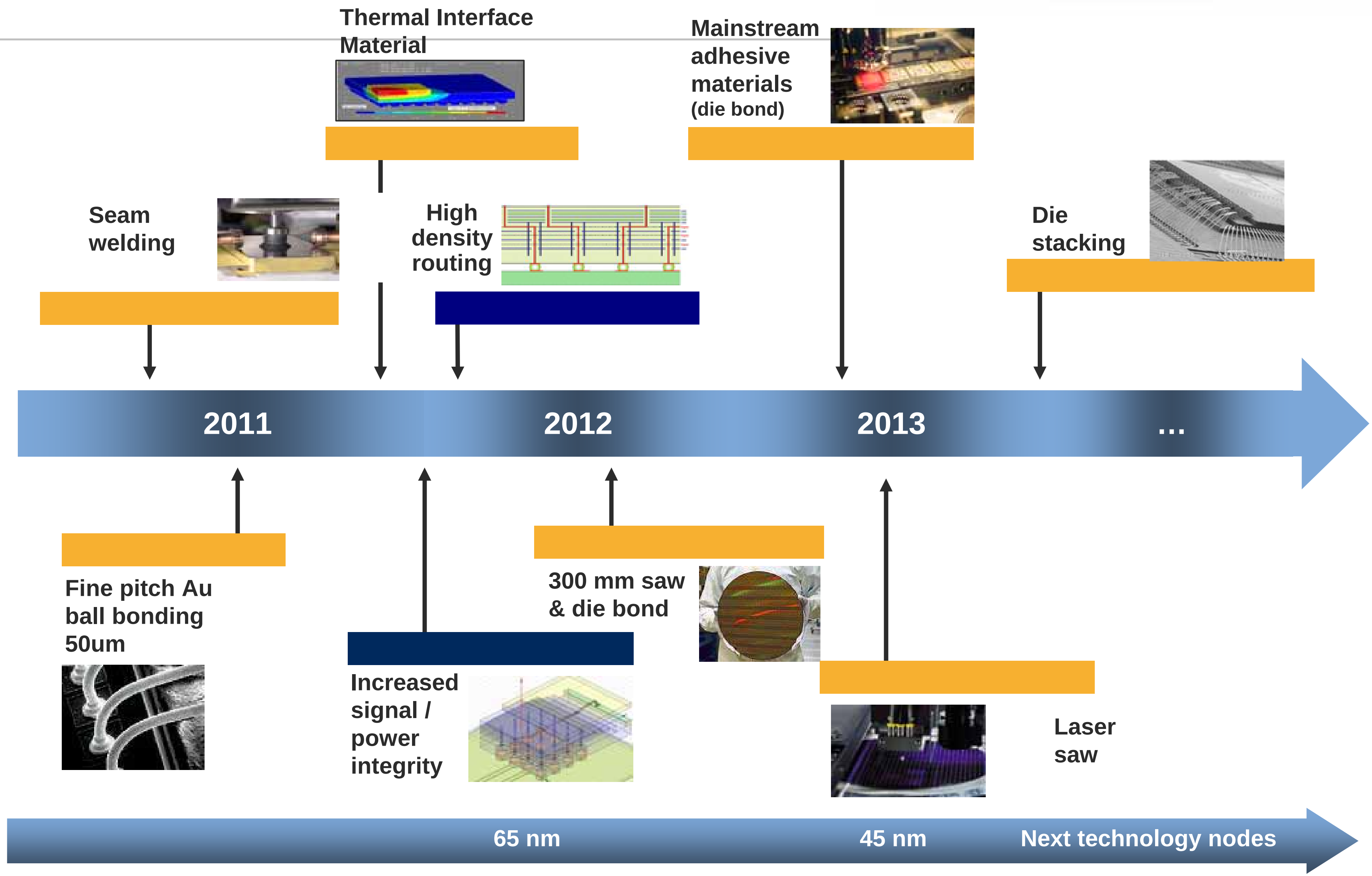
  Industrial, aerospace and military applications

- **Image sensors**

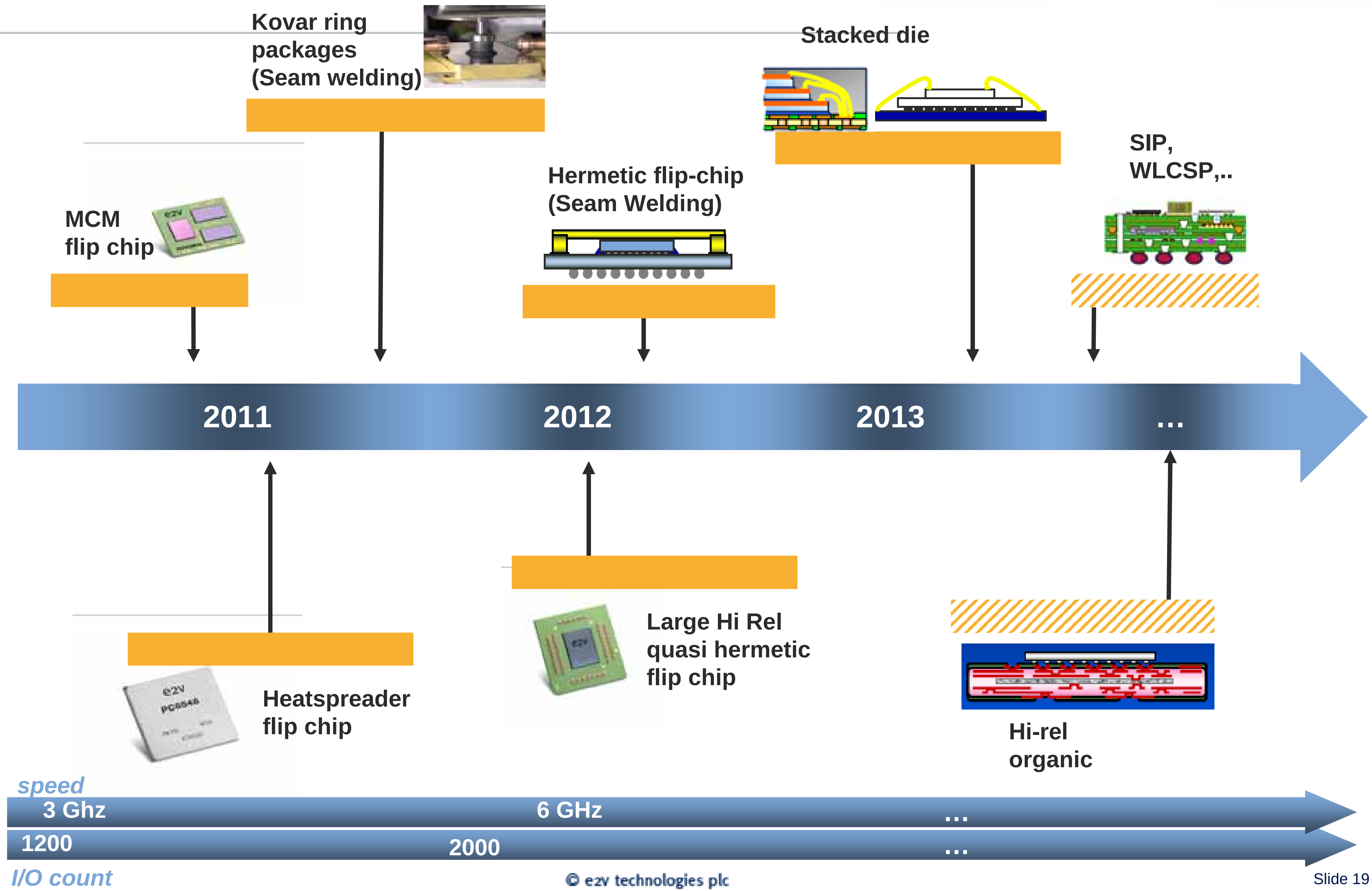
  Industrial, space and medical applications

Road Map

Package & Assembly Process evolution



Package Road Map,
for high speed, high pin count devices



Assembly & Test Services
Grenoble Industrial facilities - Test Line

- **Automatic Test Equipments**

  CCD & CMOS image sensor

    Teradyne A393, A565IH, IP750
    and dedicated test-bench

  Mixed & RF IC

    Teradyne A567 (x3), A585

  Digital IC

    Teradyne J971, J973, Tiger, Ultraflex

    NextTest PTHF64

  Dimensional test:

    ICOS CIT120

- **Low/high temperature handlers and probers**

    EG4080/4090/6000 probers

    Multitest, Delta design.

- **Reliability and burn-in :**

    Secasi- AEHR – ELES oven

Life cycle extension
Examples & References related to wafer banking




- 20+ years : 8-bit microprocessors (68XX)
- 12+ years : 32-bit microprocessors (68XXX), ARINC Controller, ADCs
- 10+ years : Digital/Mixed signal ASICs, 8-bit microcontrollers (HC811E2, HC11)

All commitments to customers entirely fulfilled, no product shortage ever !

In summary,
e2v commitment to Space market

- European Semiconductor Industrial partner for supply chain, back-end and long term support of complex products:
  - semiconductors, image sensors, high speed data converters, life cycle extension…
- Space components solutions and roadmaps, in synergy with adjacent markets (Civil and Military Avionics, Defence, Medical, Scientific & Industrial)
- Bridge between commercial semiconductor industry/technologies and the specific needs of Aerospace market.

Thank you!

www.e2v.com

CENTRE NATIONAL D'ÉTUDES SPATIALES

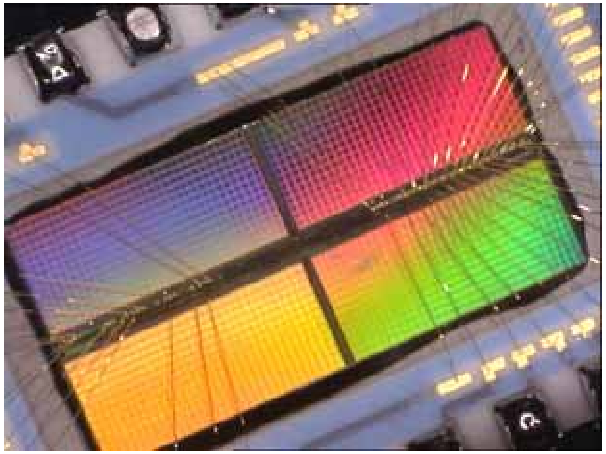
In-orbit anomalies due to radiation. Lessons learnt

Robert Ecoffet, CNES, France

Technical context

- **A problem which is** specific **to space applications**
- **A** major **dimensioning** constraint **for on-board systems**
- **Very** fast evolution **of electronic technologies**

- **Performance often leads to** cutting edge **designs**
- **A strong economic drive toward** margin reductions
- **More** exposed **missions**
- **Smaller satellites (less shielding)**



Dimensions : 0.1 µm²
(or 0.3 µm x 0.3 µm)
for a 1-Gbit DRAM cell

Time : 1 ps
for a 1-GHz processor

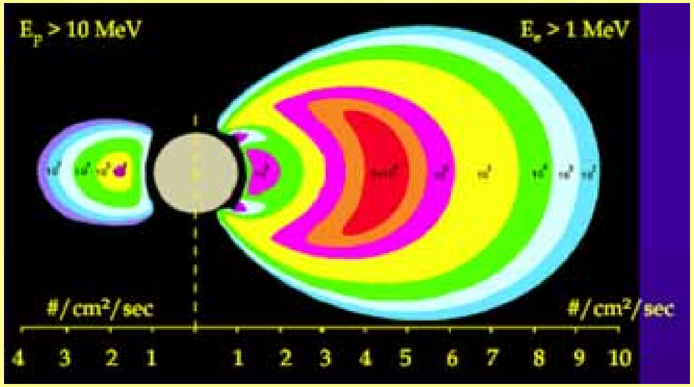
Charge : 1 µV
for a 22-bit ADC

256 Mbit SDRAM : more transistors in a single chip than in a whole 1980's spacecraft designs

(GALILEO Jupiter probe for example)

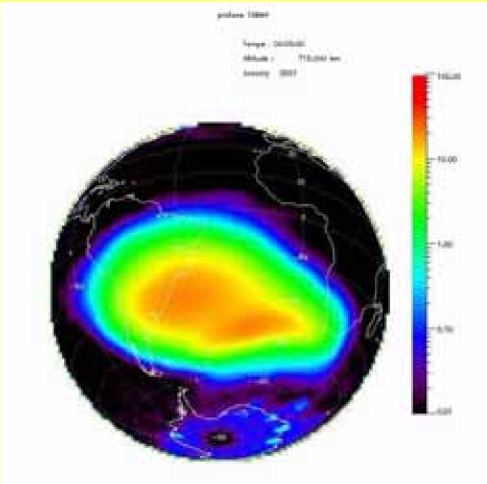
Space environment radiation sources

Radiation belts

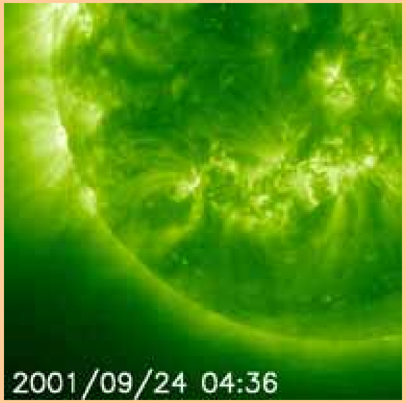


Protons — keV- 500 MeV

Electrons — eV ~ 10 MeV

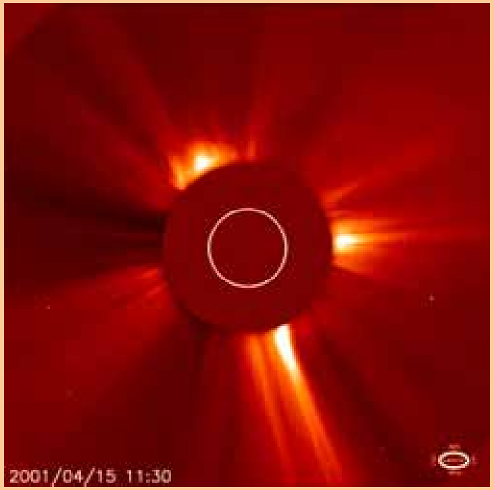


Solar flares



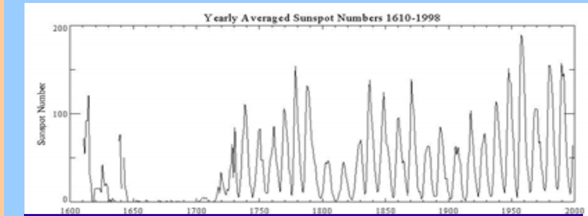
Protons — keV- 500 MeV

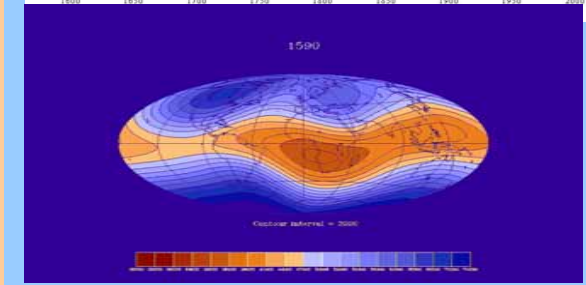
Ions — few 1-10 MeV/n



Cosmic rays

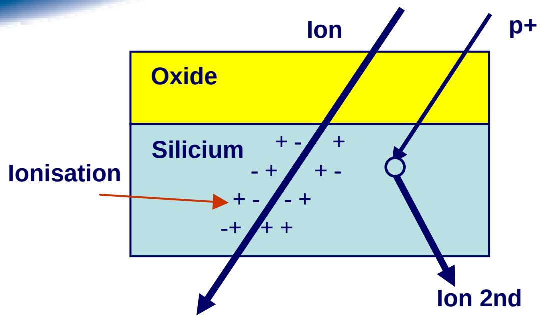
Ions — max ~ MeV/n

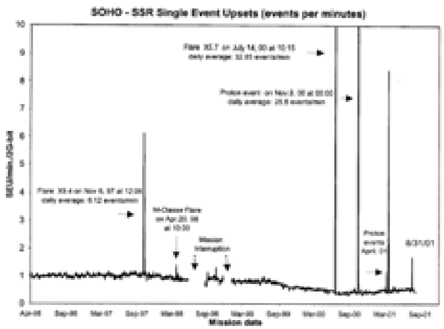


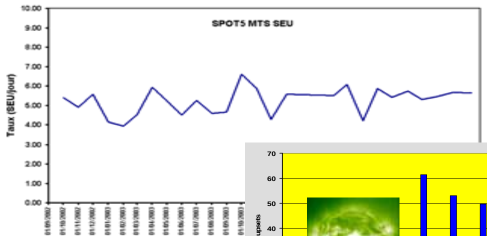


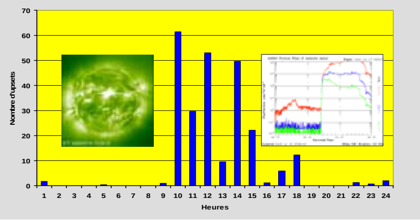
Main types of radiation effects

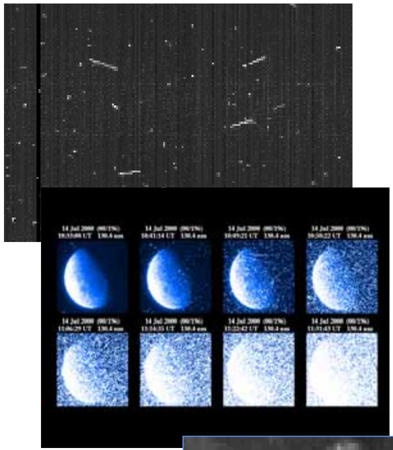
Single event effects

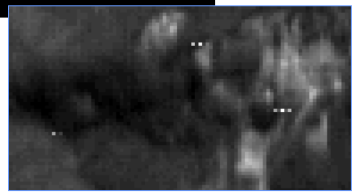




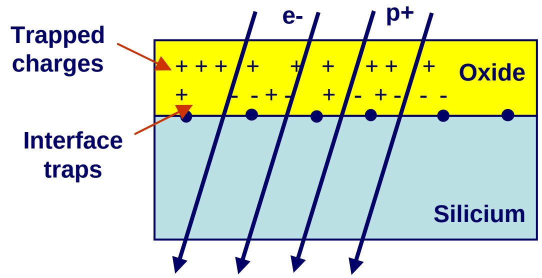


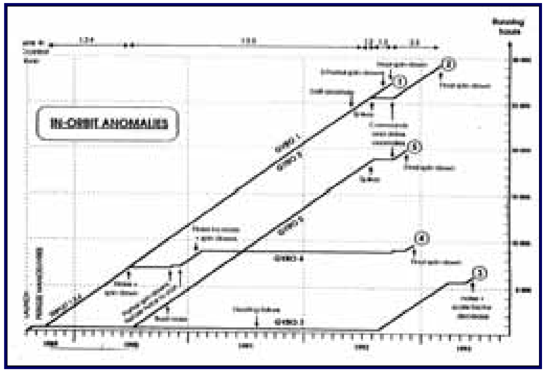


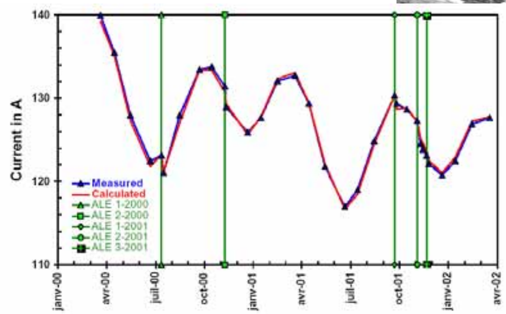




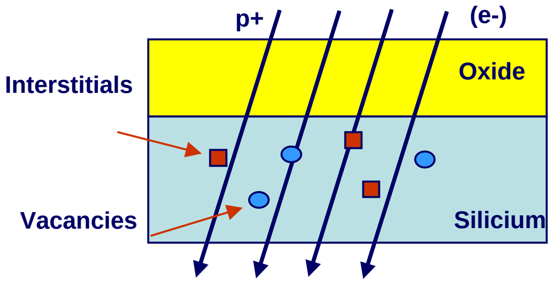
Ionising dose

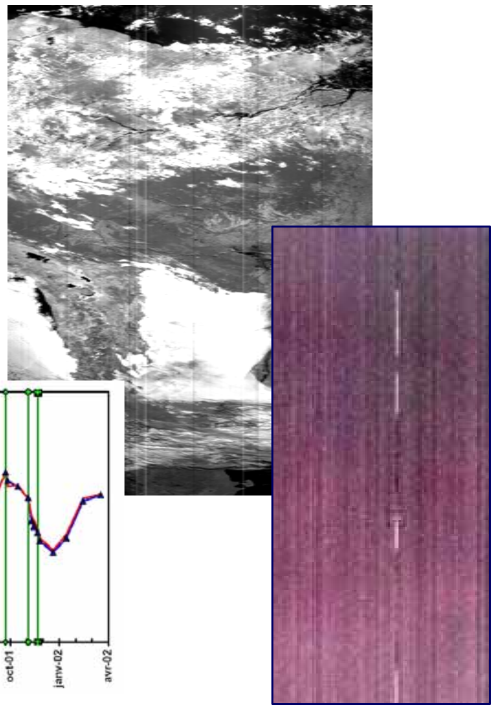






Atomic displacement





Known (to the author) system effects

Electrical Architecture (Generic) **- Equipment loss** **- Self switch-off, disjunction, reset, reboot, redundancy swapping**	**Dose, Latch-up (SEL)** **SET**
On-board energy **- Solar panel degradation**	**Dose, Displacements**
Attitude and orbit control system **-Possible attitude loss** **-Star tracker out of loop** **-Inertia wheels disturbances** **-Switch off ion thruster**	**SEU** **Proton transients (SAA, flares)** **SET** **SET**
On board management **-Disturbances of on board computer, resets, mode refusal, safe-hold mode** **-Mass memory**	**SEU**
Imaging systems **-« UFOs »** **-Hot pixels, RTS** **-Dark current, non linearity,… etc**	**Proton transients** **Displacements** **Displacements, dose**
Time references **- Frequency jumps**	**Dose on SAA passes or flares**

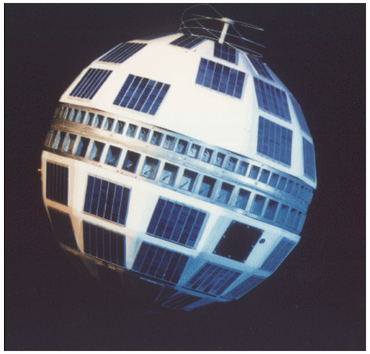
Cumulated effects

- Few records, evidenced in degraded mission cases, harsh planetary environments, or ultra-sensitive systems

- Artificial radiation belts
- HIPPARCOS
- The GALILEO probe at JUPITER
- Ultra sensitive systems

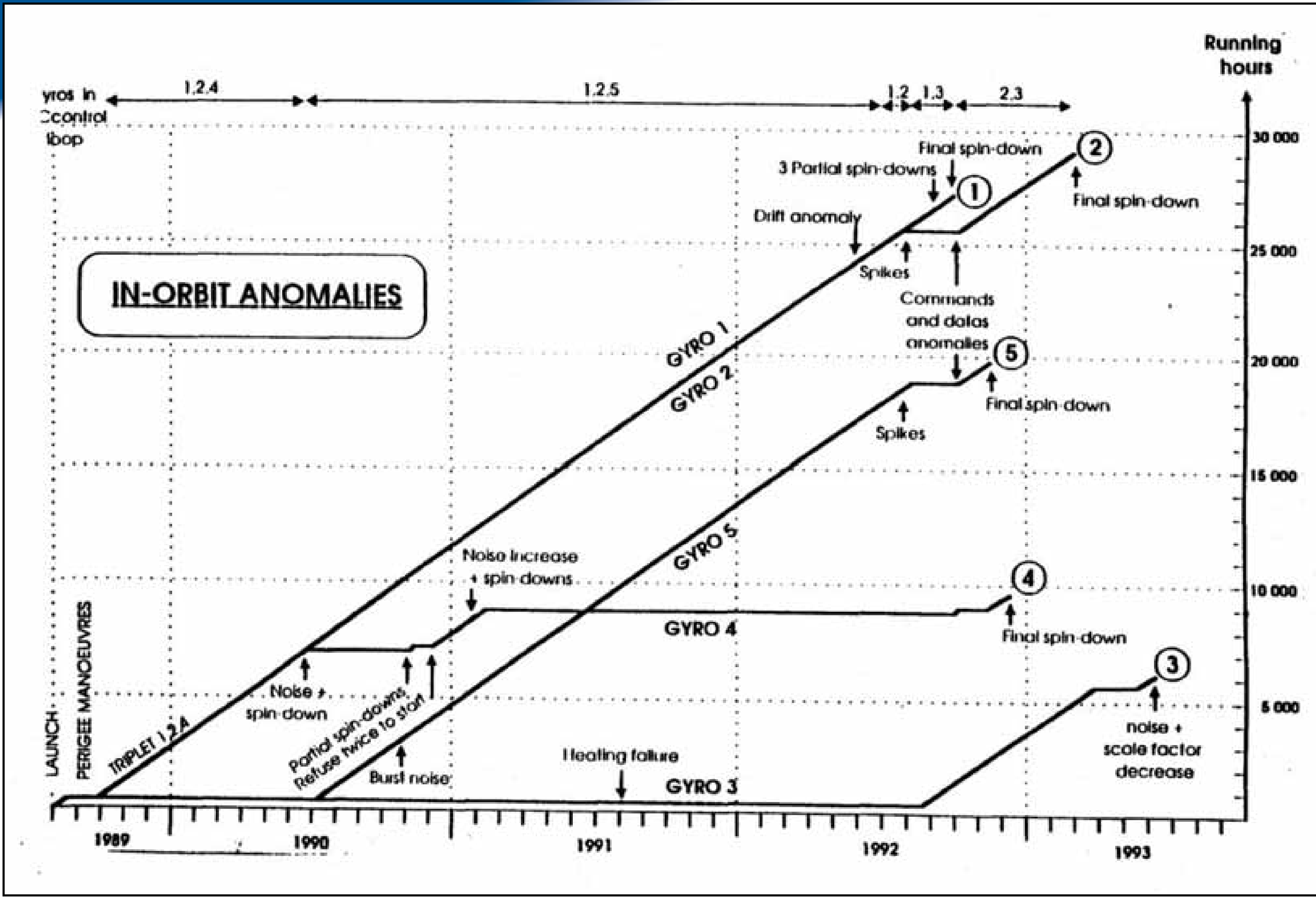
Artificial radiation belts

- 9 July 1962 : Starfish nuclear experiment
- 10 July 1962 : launch of TELSTAR-1
- 21 Feb 1963 : TELSTAR loss (diode)
- 7 satellites lost in 7 months



Explosion	Location	Date	Yield	Altitude km	Nation
Argus I	South Atlantic	8-27-58	1 kt	~200	USA
Argus II	South Atlantic	8-30-58	1 kt	~250	USA
Argus III	South Atlantic	9-6-58	1 kt	~500	USA
Argus III	South Atlantic	9-6-58	1 kt	~500	USA
Starfish	Johnson Island (Pacific)	7-9-62	1 Mt	~400	USA
?	Siberia	10-22-62	? 100s of kilotons	?	USSR
?	Siberia	10-28-62	submegaton	?	USSR
?	Siberia	11-1-62	megaton	?	USSR

HIPPARCOS



GYROSCOPES

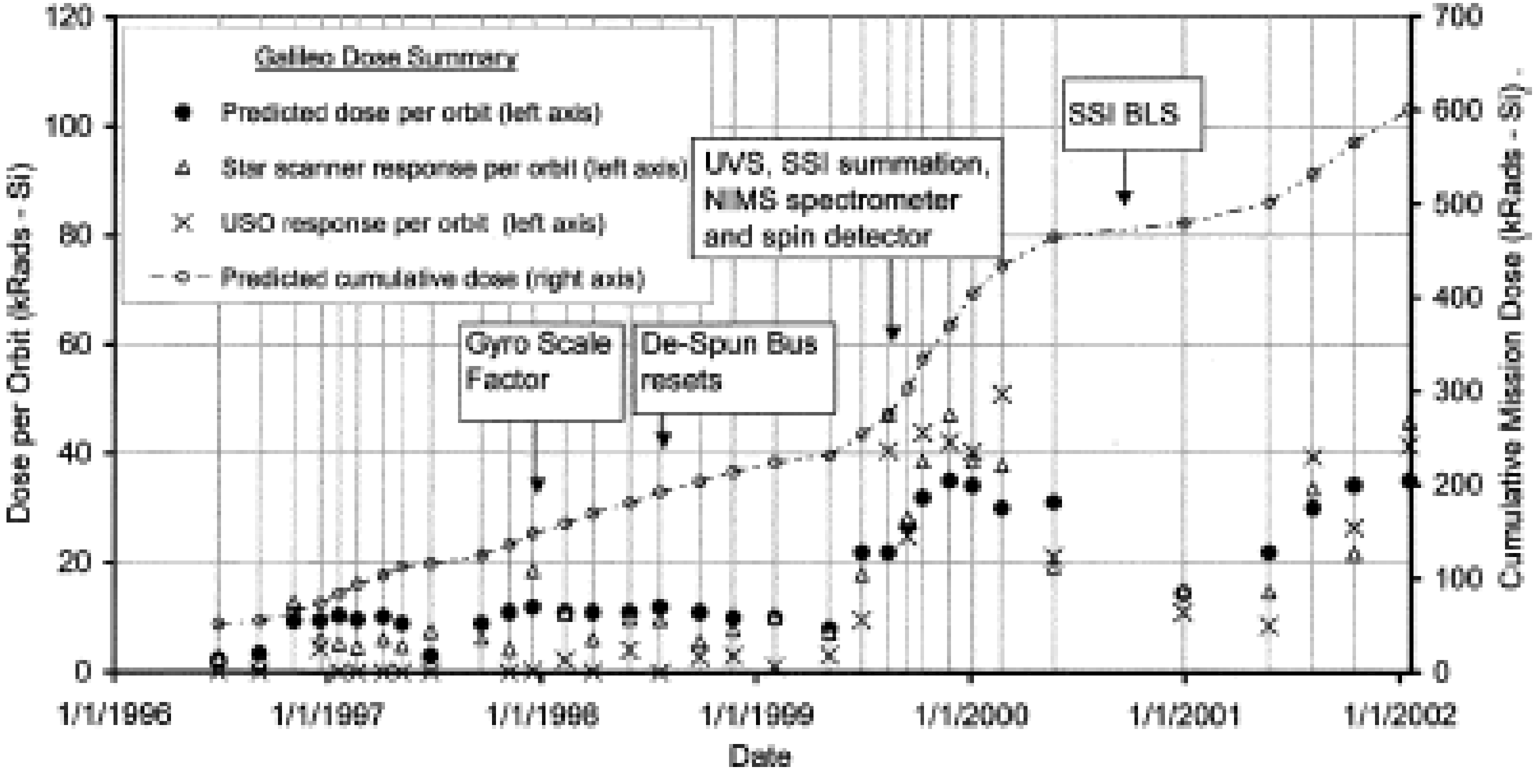
Both nominal and redundant units failed successively

Attributed to TID degradation of bipolar PROMs and optocouplers

Nominal mission lifetime exceeded in more aggressive orbit.

GALILEO probe at JUPITER

- Timeline of effects



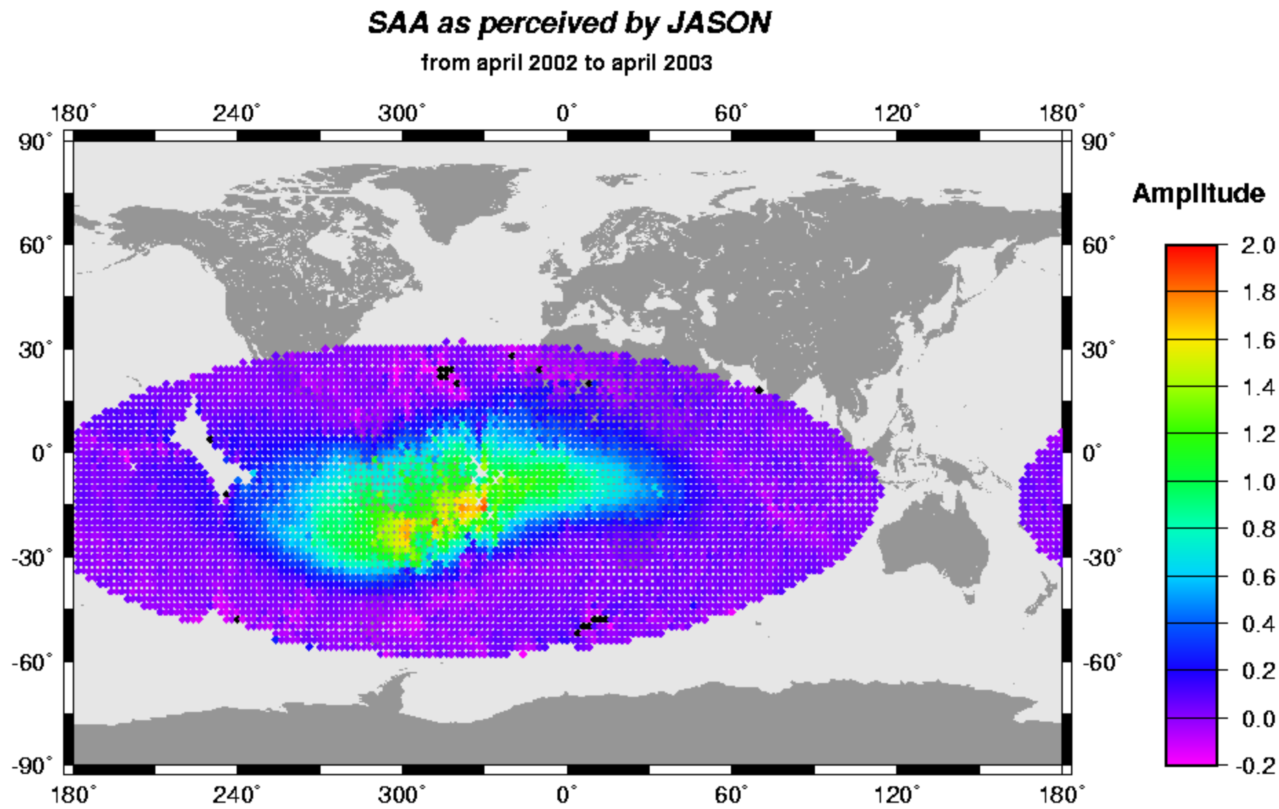
GALILEO probe at JUPITER

- After Amathea encounter, data collection stopped
- Deepest orbit in the radiation belts
- Spacecraft switched to safe mode (proton SET in command and data system)
- Recorder could not be played back
- Problem due to OP133 LED in tape position encoder
- JPL used a current annealing strategy
- Recorder was restarted and data retrieved

This is a perfect example of the application of excellent radiation effects knowledge in a practical mission case

Ultra-sensitive systems

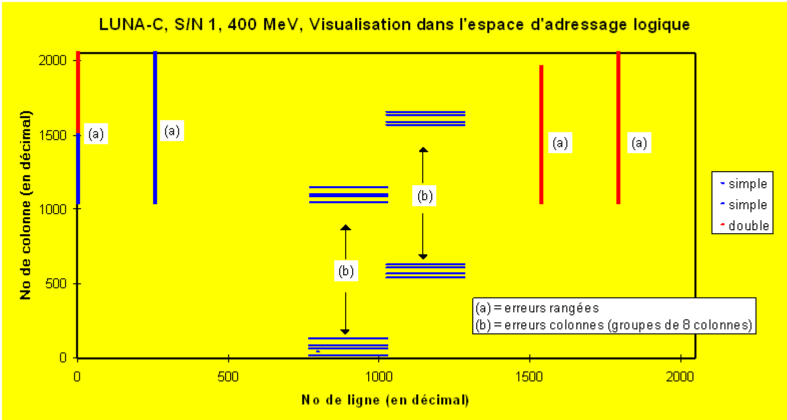
- DORIS / JASON-1 frequency shifts

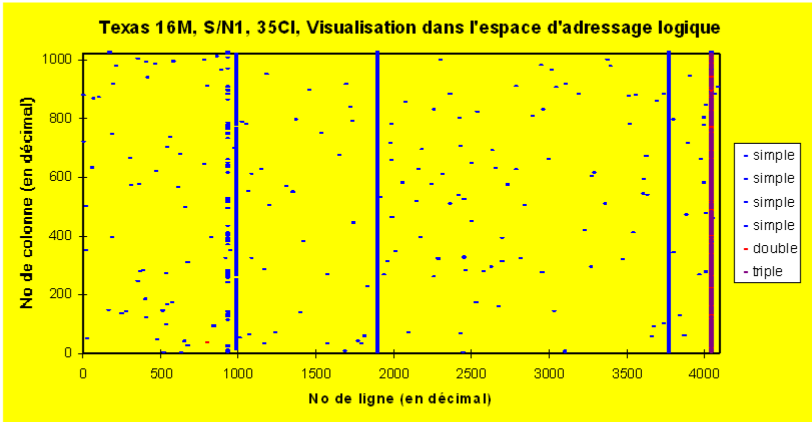


Single event effects

- Numerous records, major contributor to radiation induced spacecraft anomalies

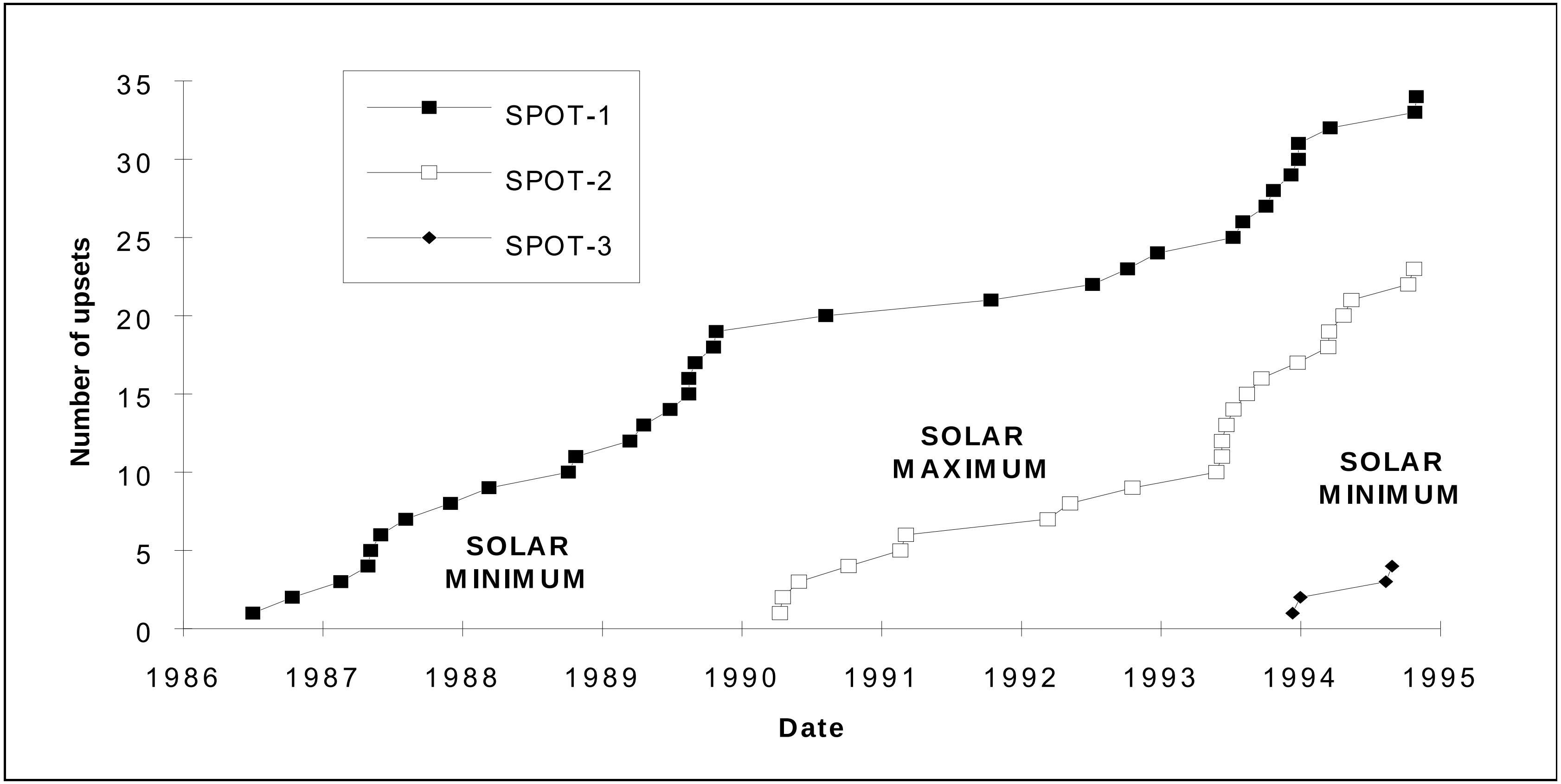
- Galactic cosmic rays
- Solar particles (protons, ions)
- Trapped protons





Cosmic ions

SPOT-1, 2, 3 OBC upsets (SSO orbit)



Cosmic ions

SOHO at L1 events (except SSR)

TABLE I
ESR EVENTS

Date	Unit	Event
04/12-1996	ESR	Attitude Control Unit – PSU reset
19/11-1997	ESR	Attitude Control Unit – self switch-off
03/03-1998	ESR	Centrale Data Mana. Unit – switched
28/11-1999	ESR	Attitude Control Unit – PSU reset
07/01-2000	ESR	Attitude Anomaly Detector – spurious
28/11-2000	ESR	Attitude Control Unit – PSU reset
14/01-2001	ESR	Attitude Control Unit – PSU reset

TABLE II
BDR EVENTS

Date	Unit	Event
12/01-1997	BDR1.2	Switch-off triggered by protection
01/04-1997	BDR1.1	Switch-off triggered by protection
16/05-1998	BDR2.1	Switch-off triggered by protection

TABLE III
VIRGO EVENTS

Date	Unit	Event
09/09-1996	VIRGO	Crashed – self switch-off event
07/05-1997	VIRGO	Latch-up - self switch-off event
20/05-1997	VIRGO	Latch-up – self switch-off event
26/05-1998	VIRGO	Power fail – self switch-off event
12/07-1999	VIRGO	Latch-up in DAS – (1st SEL)
11/02-2000	VIRGO	Latch-up in DAS – (2nd SEL)
30/03-2001	VIRGO	Latch-up in DAS – (3rd SEL)

TABLE IV
LASCO EVENTS

Date	Unit	Event
19/03-1996	LASCO	Voltage anomaly – requiring reboot
10/06-1996	LASCO	Voltage anomaly – requiring reboot
19/12-1996	LASCO	Voltage anomaly – requiring reboot
26/04-1998	LASCO	Hung-up – requiring reboot
28/03-2000	LASCO	PROM off – requiring reboot

Power supply events : SETs on PM 139 or UC1707J

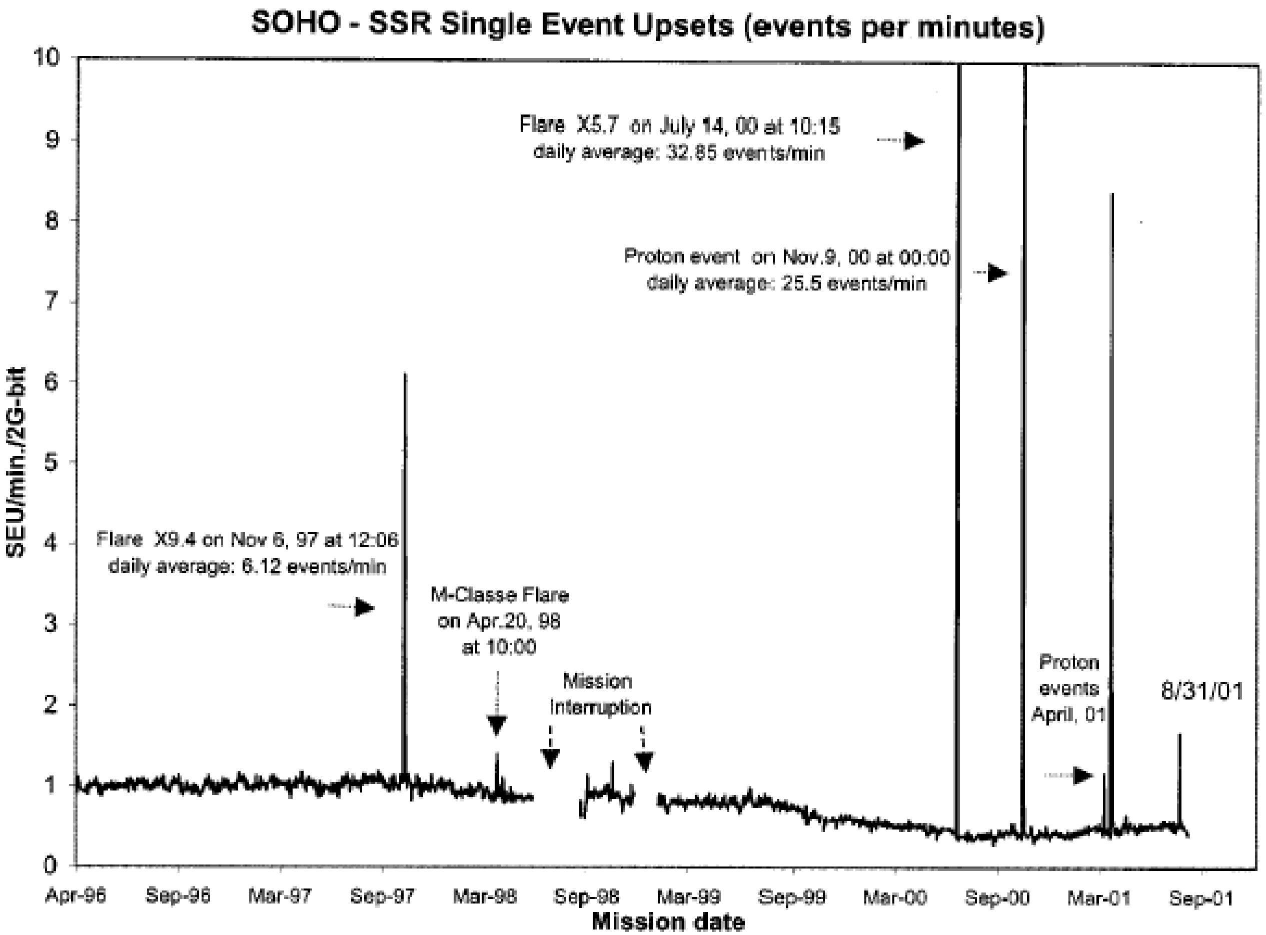
Solar particles

MAP at L2 processor reset

- **MAP (NASA spacecraft) orbiting at L2**
- **5 November 2001, switch to safehold condition**
- **Due to processor reset**
- **3-7 November 2001 : large solar event**
- **Solar ion SET on PM139 from reset circuitry**
- **Consolidated by CREDO / MPTB (QinetiQ UK) measurement of flare ions**

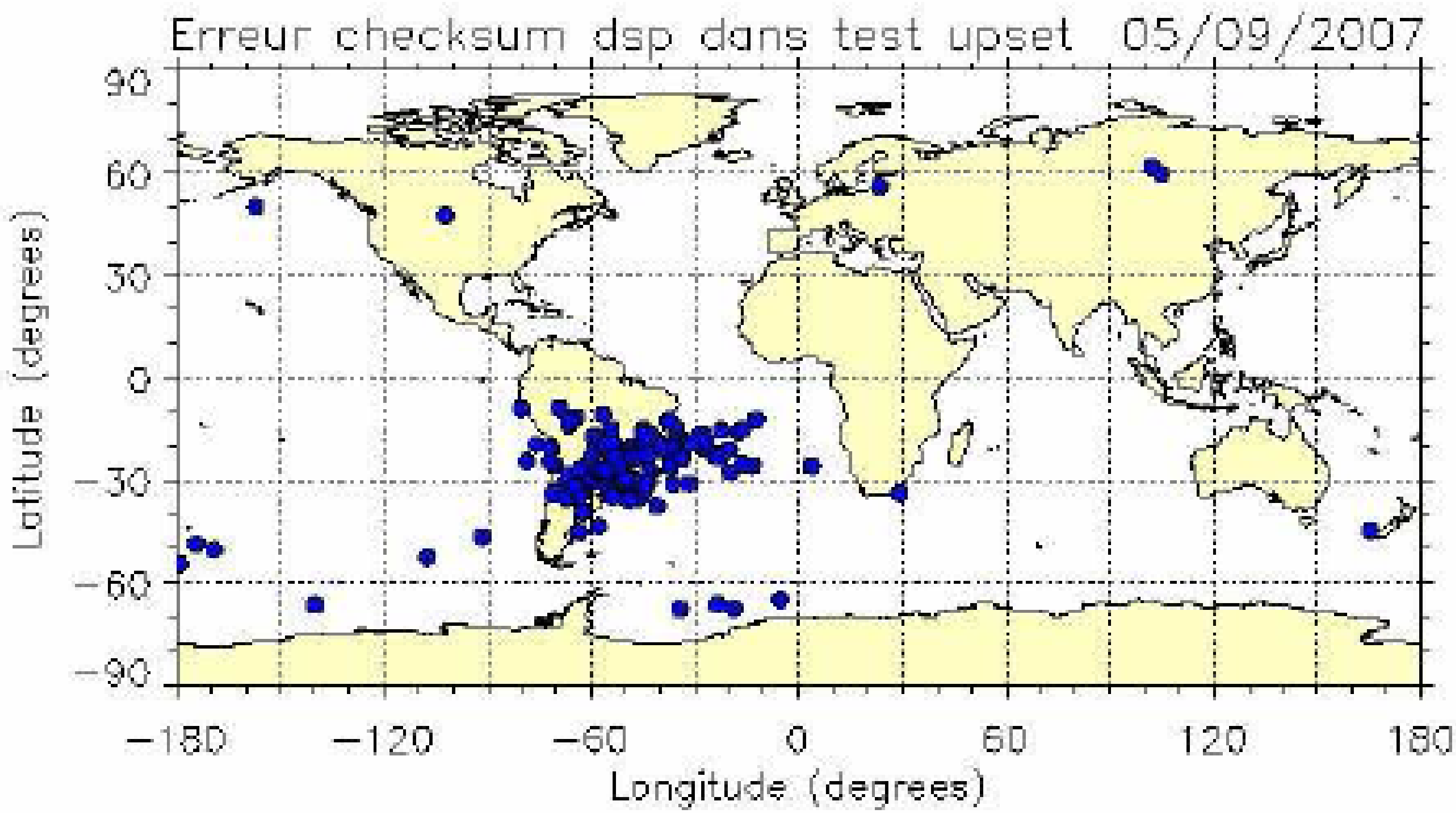
Solar particles

SOHO at L1 SSR upsets



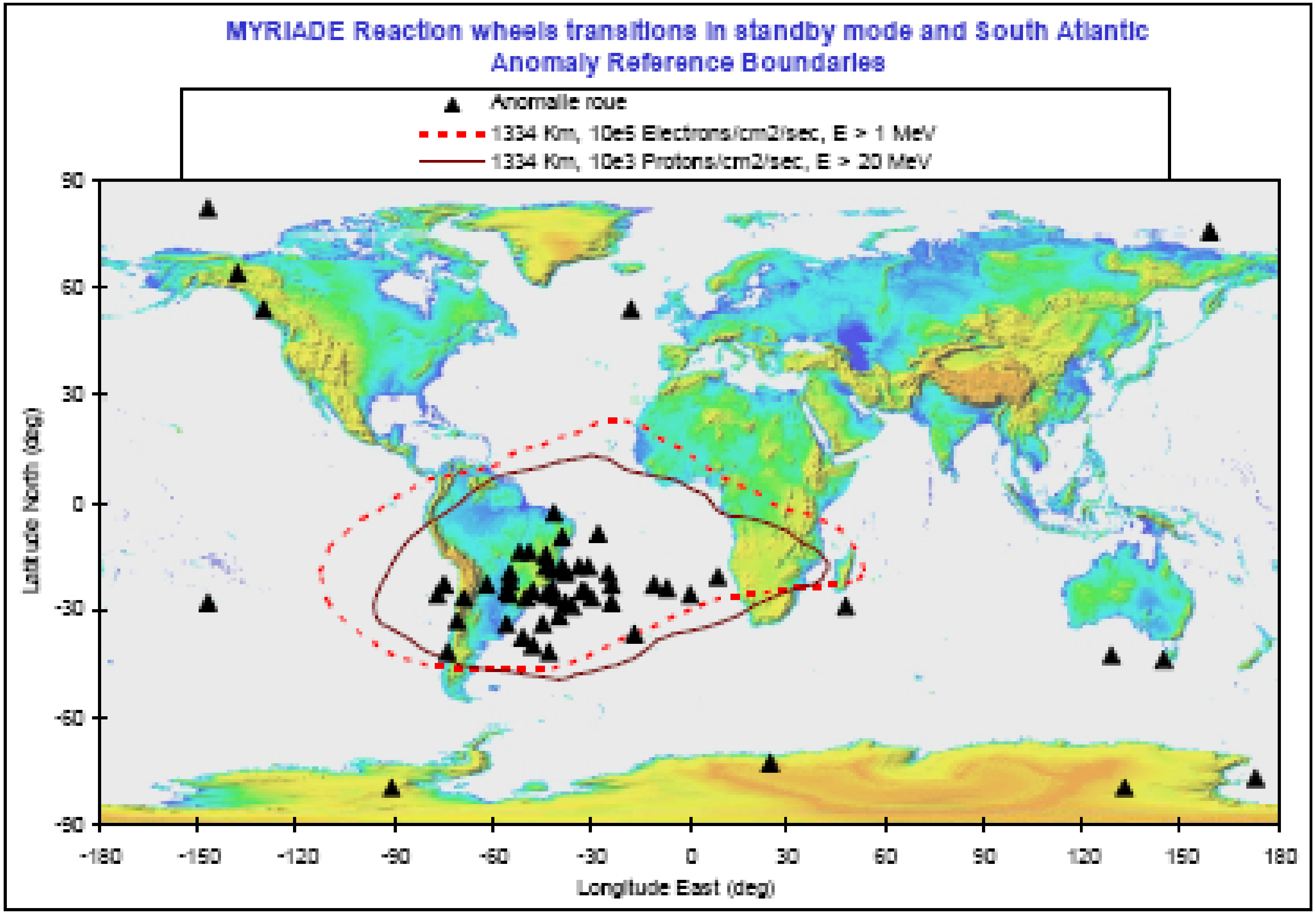
Trapped protons

DEMETER BANT DSP upsets



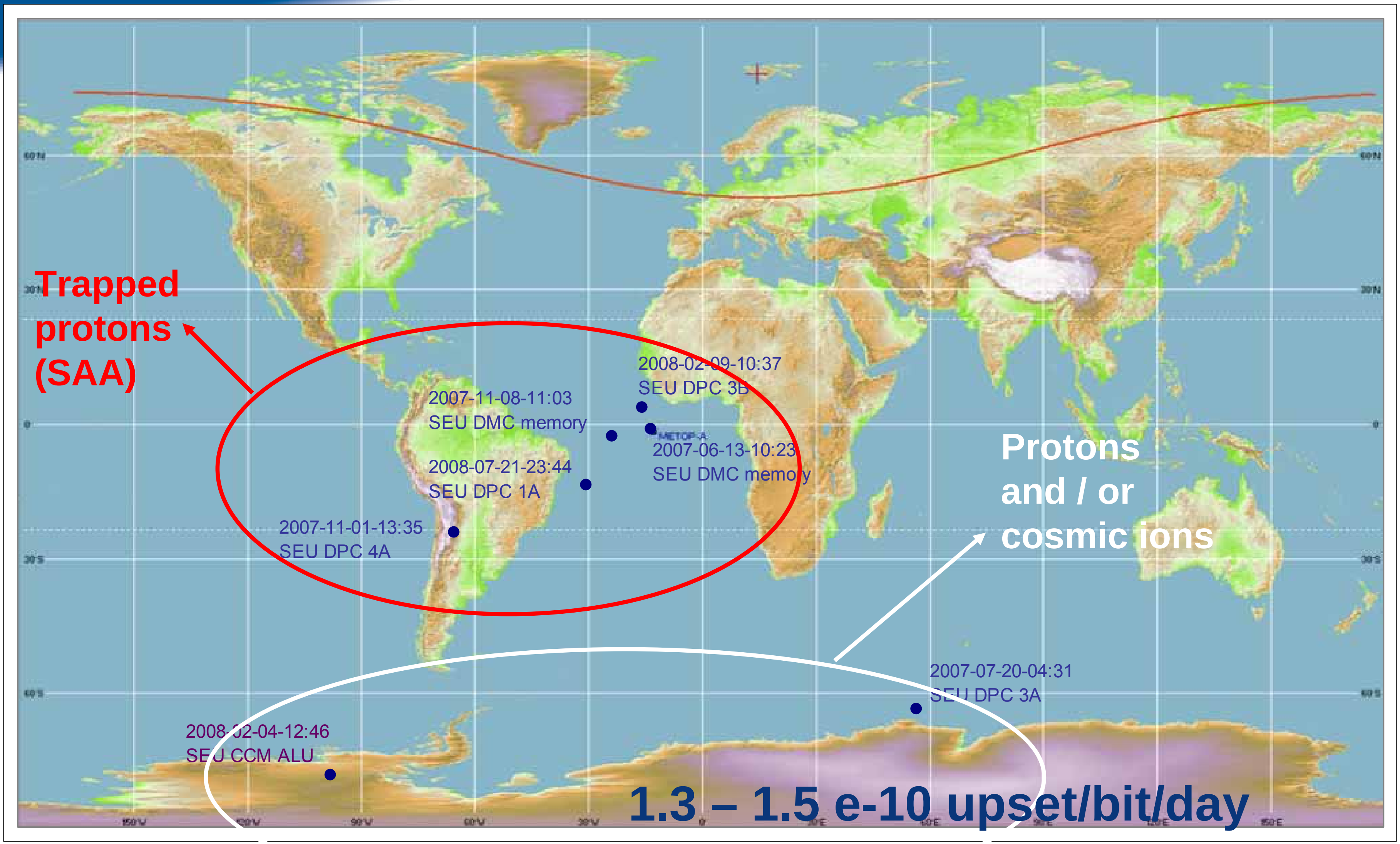
Trapped protons

MYRIADE reaction wheels resets



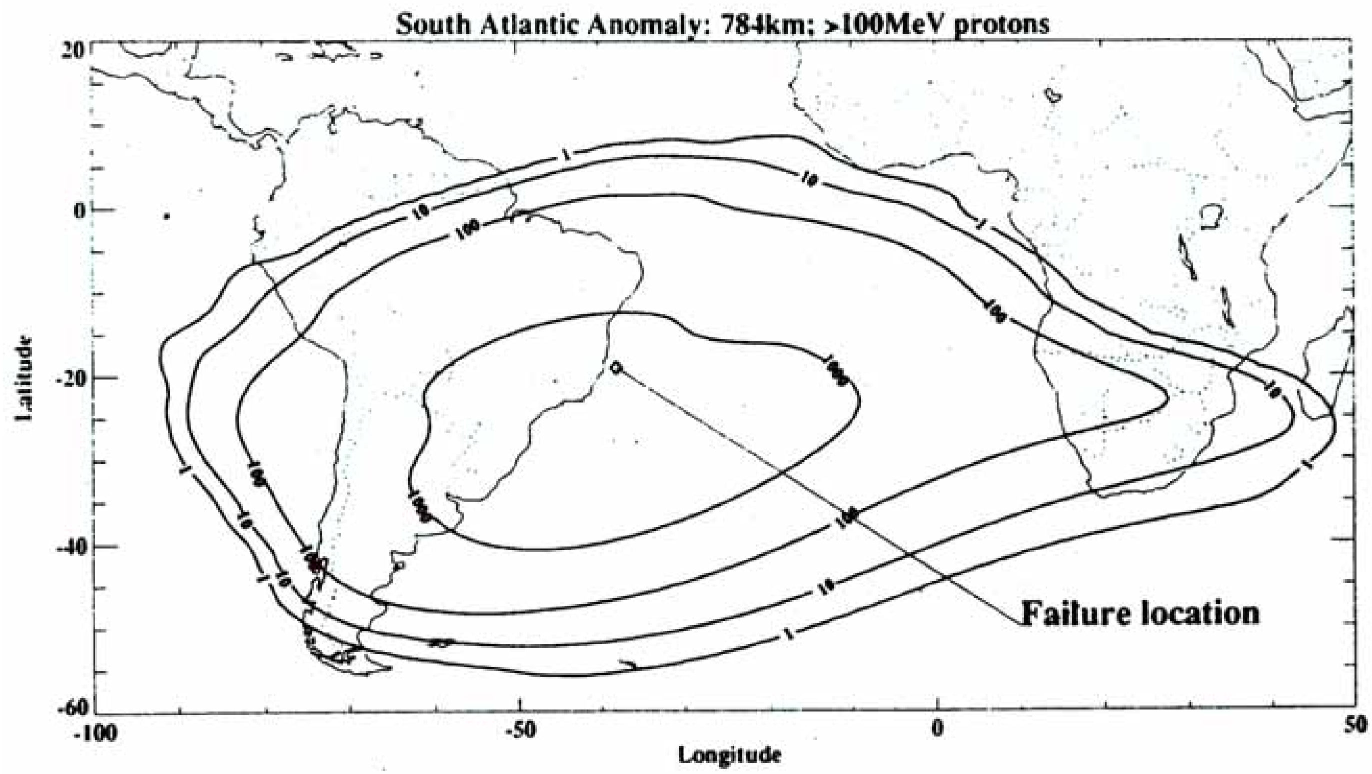
Trapped protons

IASI/METOP : SEUs on rad-hard memories



Trapped protons

PRARE / ERS-1 instrument loss (SSO)



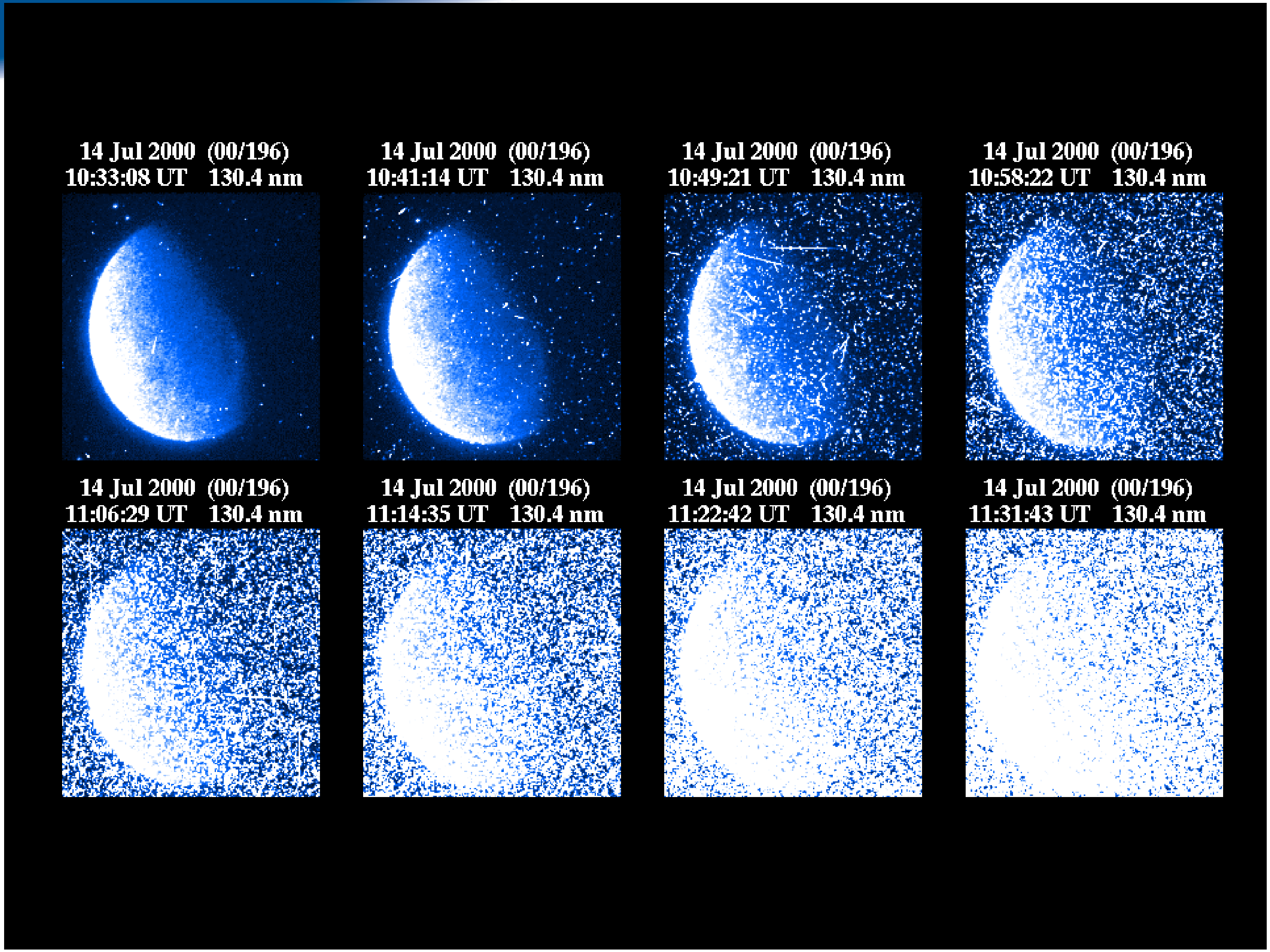
- **Latch-up on 64-kbit CMOS SRAM, after 5 days**
  9 W, 16 to 32s, instrument lost

The particular case of sensors

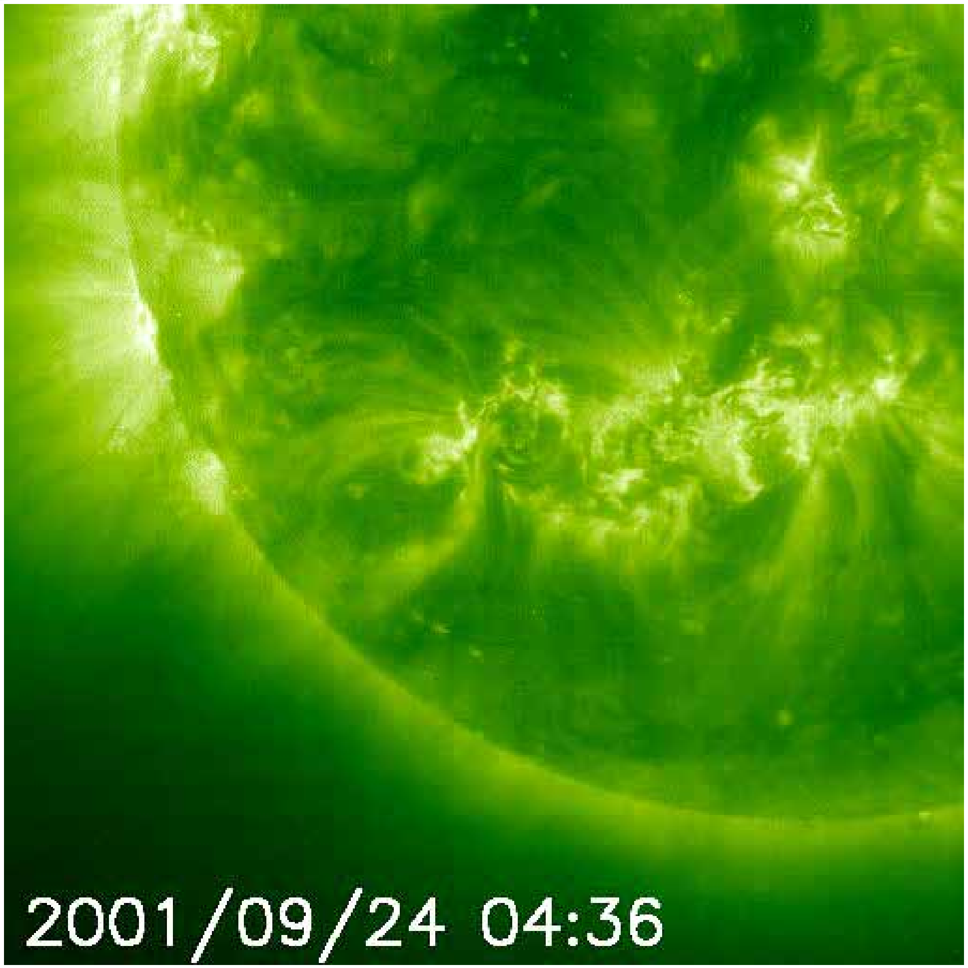
- External sensors are particularly exposed to radiation
  - By nature (charge collection devices), they are sensitive to radiation effects
  - Charge collection after a proton (or ion) impact
  - One or many pixels may be affected
  - On matrix detectors, tracks can appear

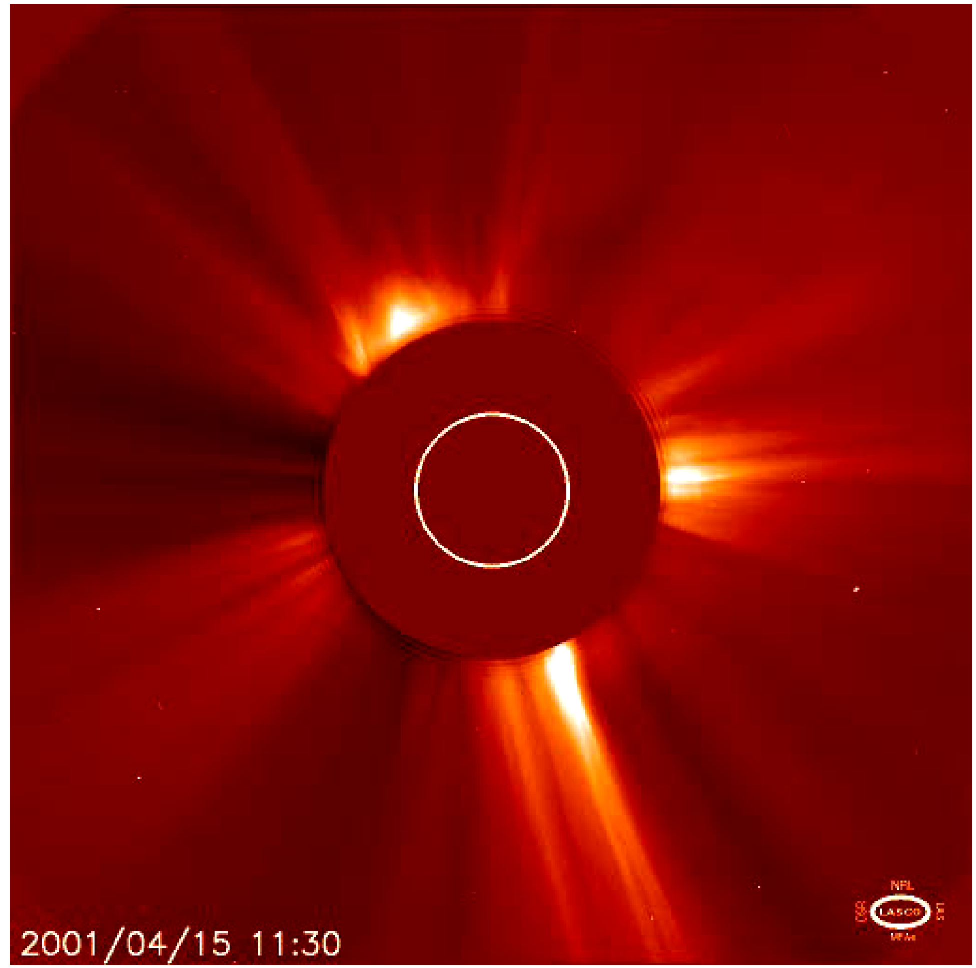
- Transient signals
- Permanent or semi-permanent damage

Blurring of VIS camera on NASA / POLAR



Solar protons "filmed" by SOHO





Galileo at Jupiter

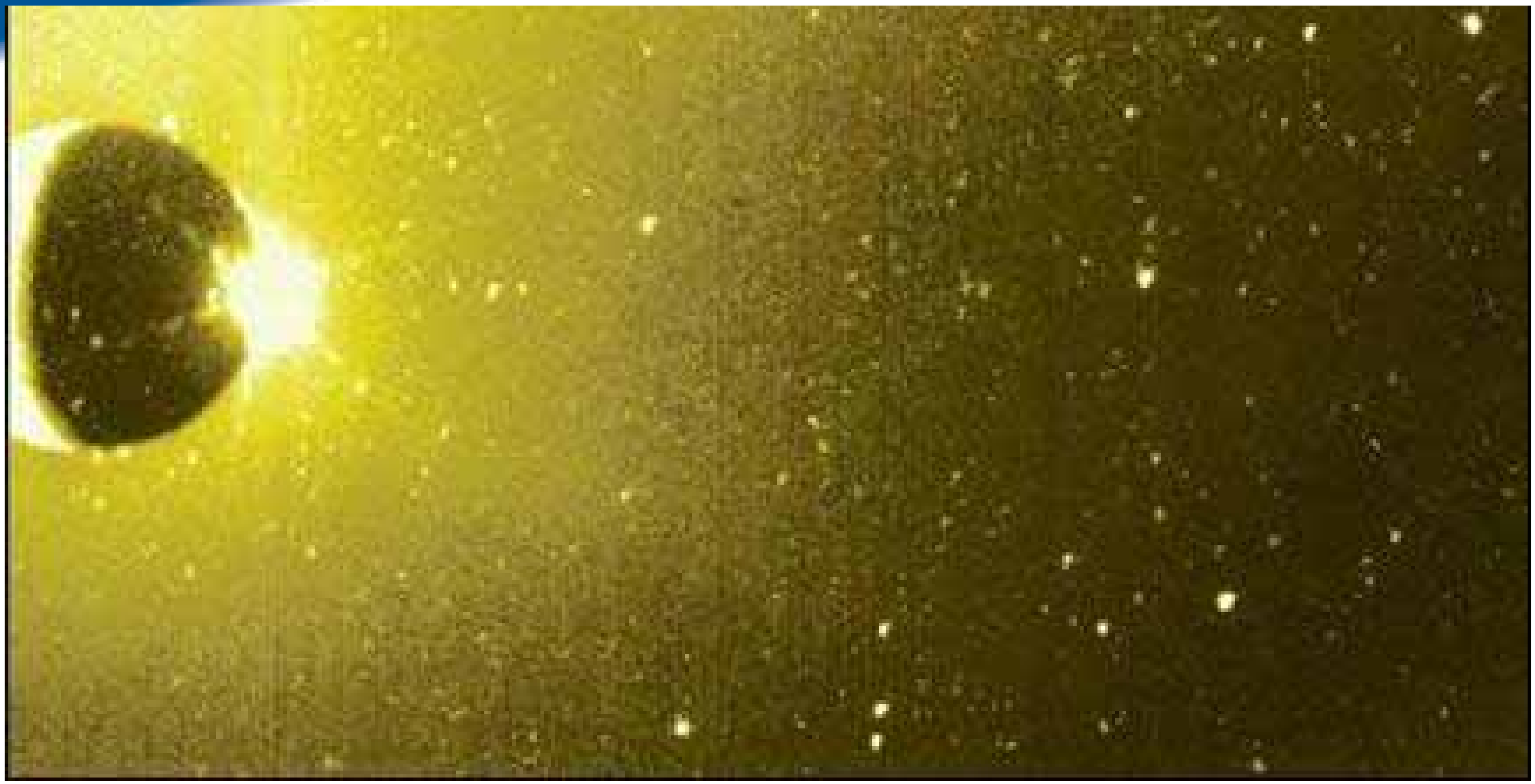
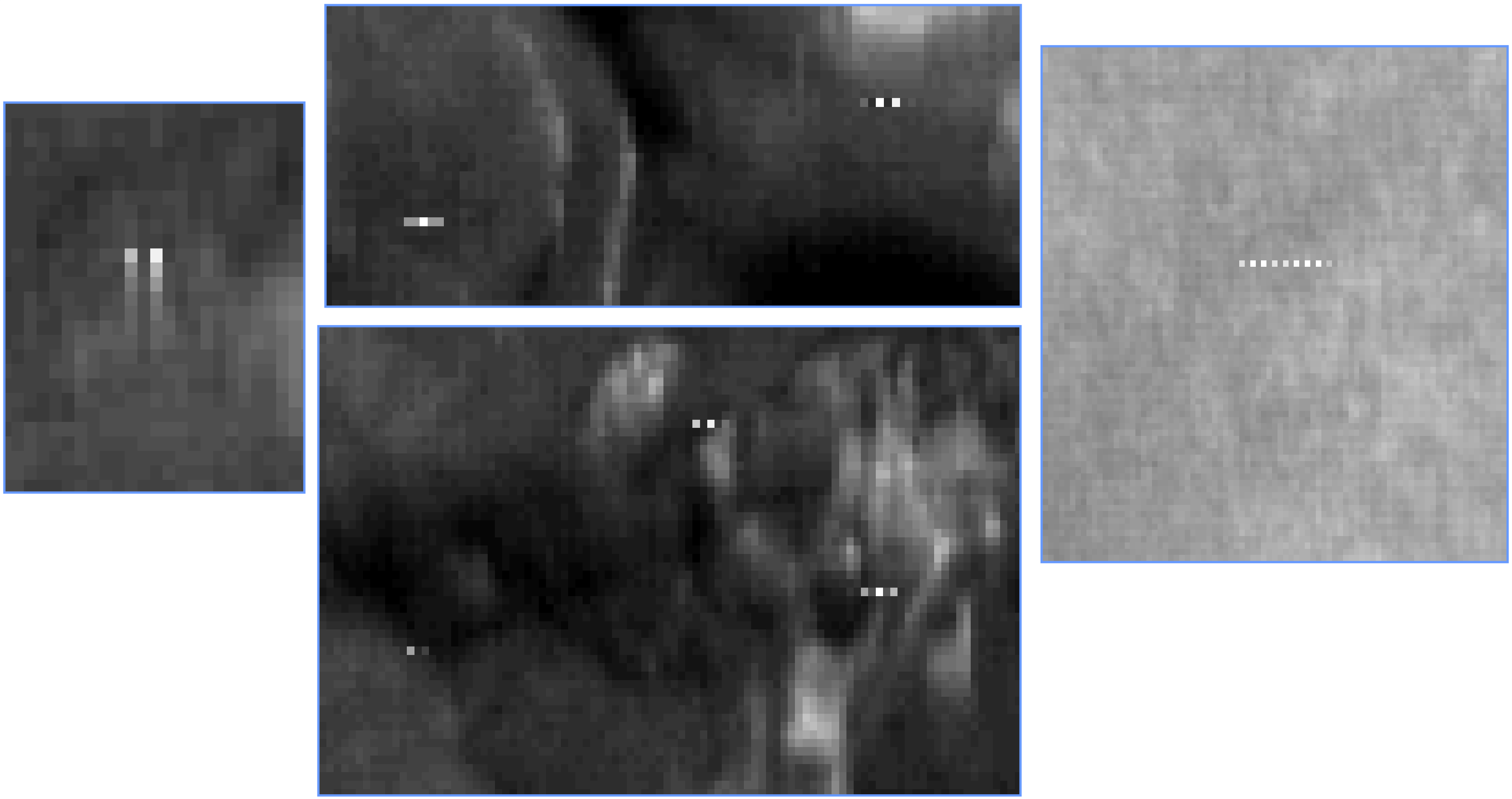
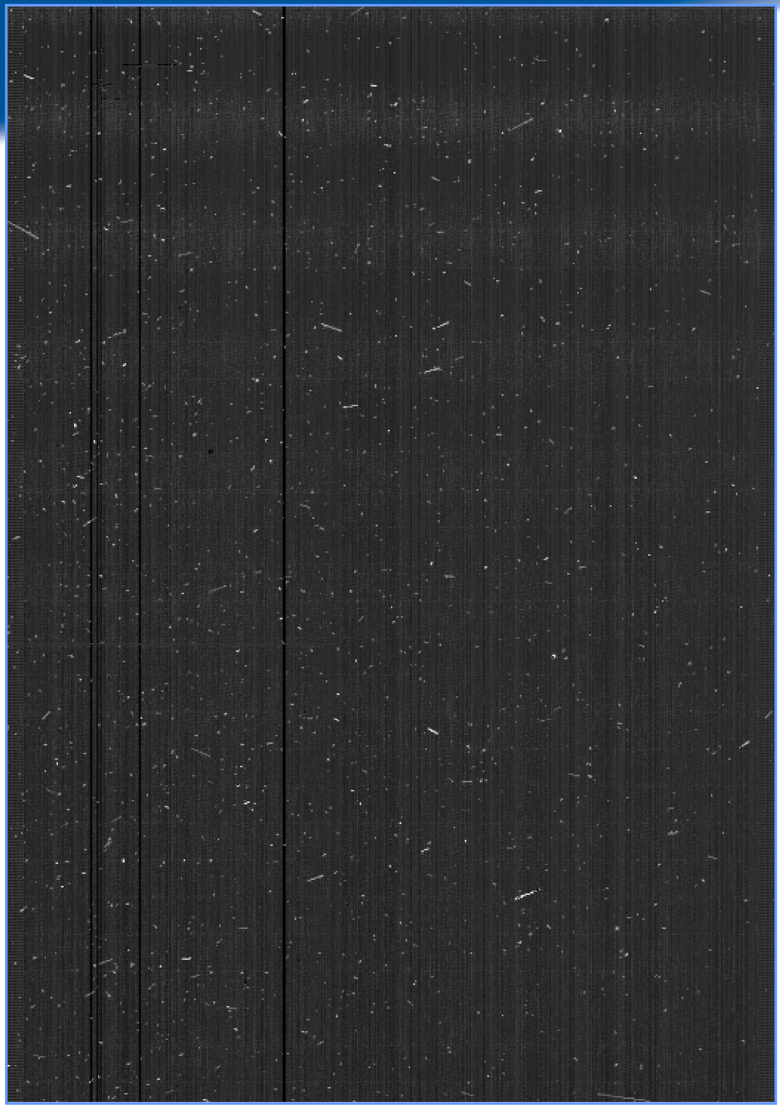


Image of a Sodium volcanic plume on the moon Io contaminated by speckles due to Jupiter radiation belts, JPL image

SPOT "UFOs"

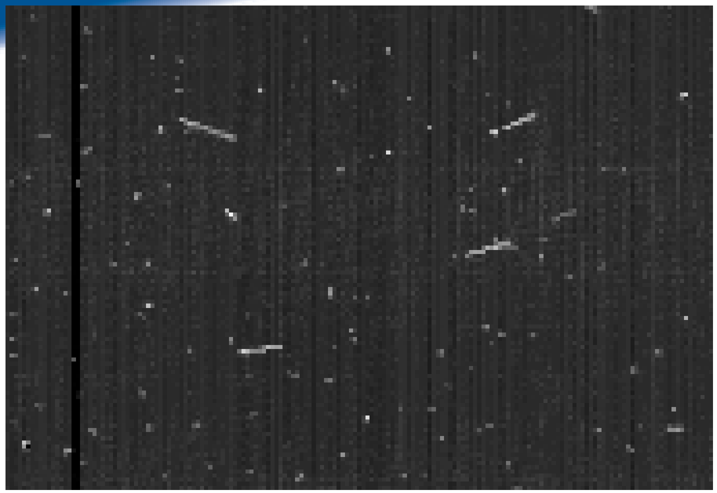


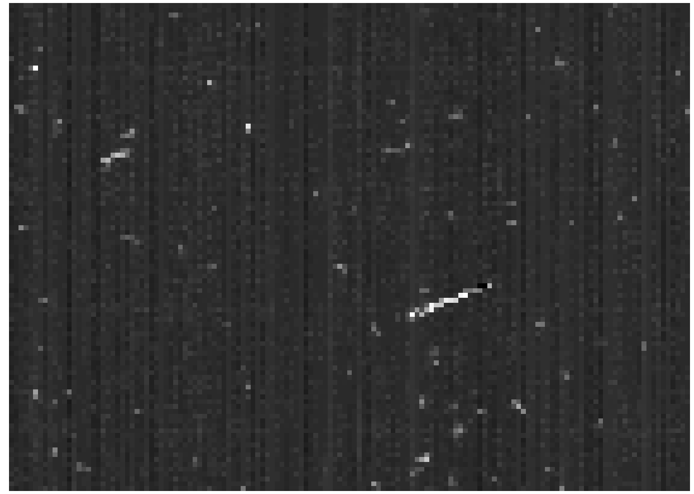
Jason-1 star tracker transients



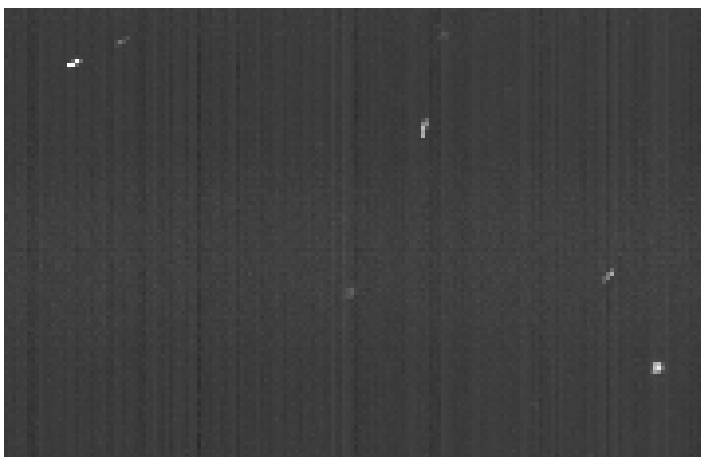
Proton tracks in SAA passes

Jason-1 star tracker transients





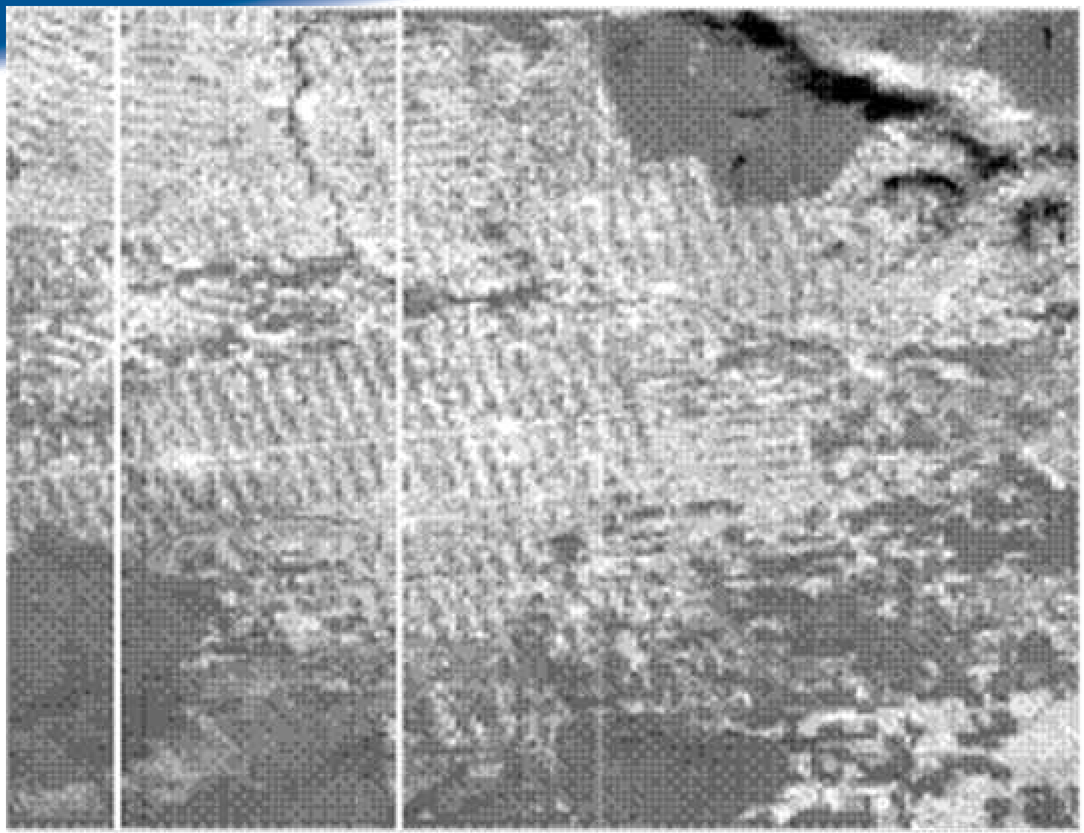
SAA passes

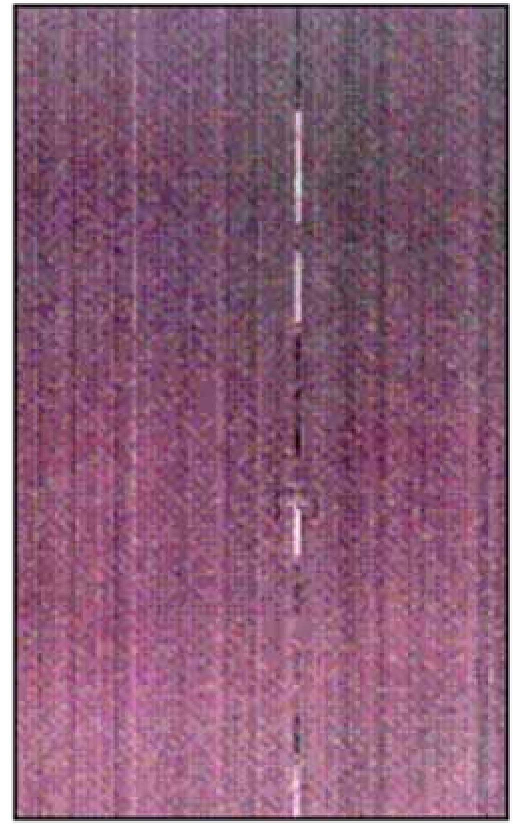


Clear star field

Same star tracker on JPL GENESIS probe was blinded 4 times during April 2002 SPE.

Permanent or semi-permanent damage





Hot pixels (left) and RTS (right) on SPOT-5 MIR detectors

Space weather action cases

NASA Lidar on CALIPSO

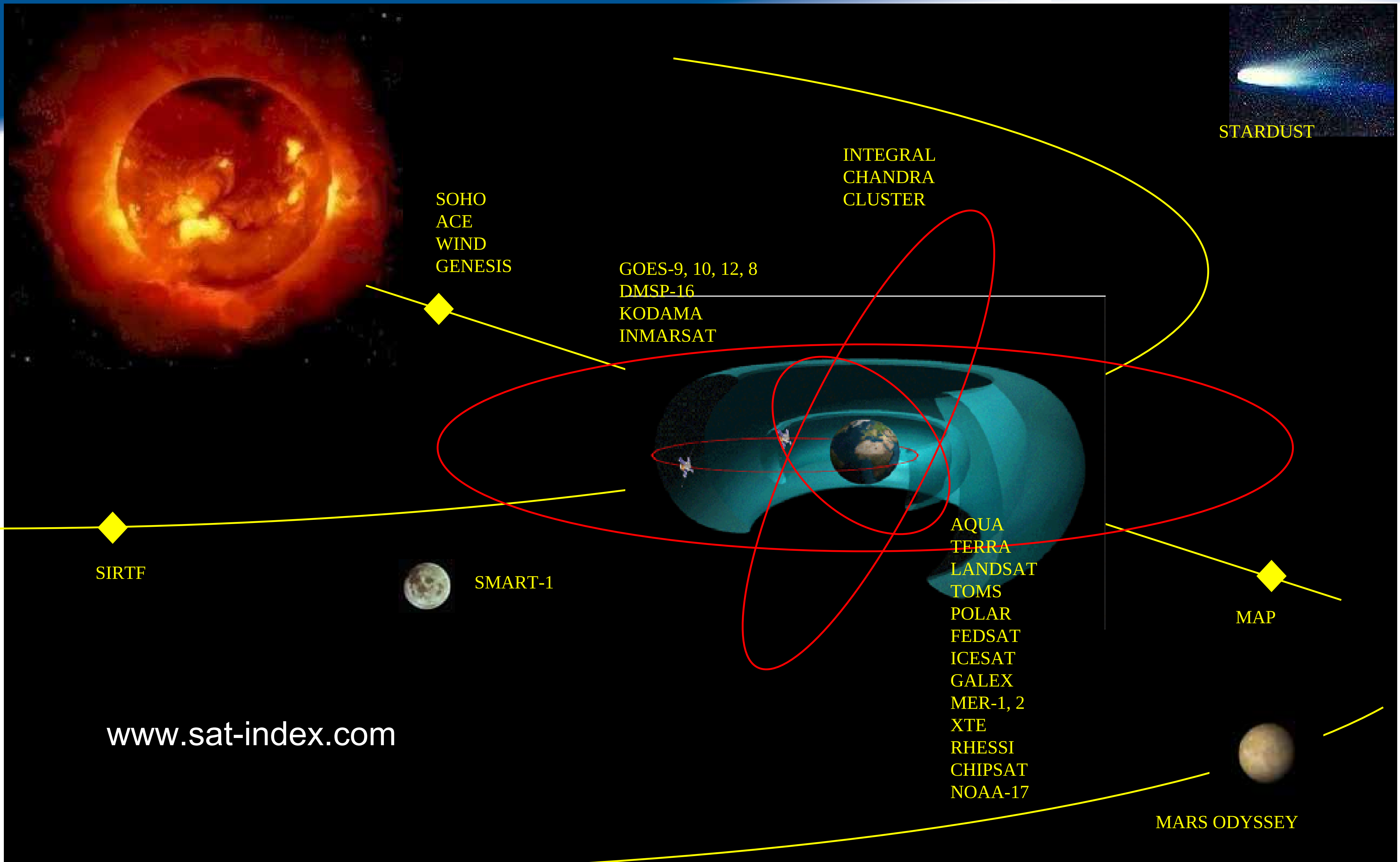
-An SEU on one of the Lidar components can lead to a constantly powered X-band emitter with a risk of burn-out if this lasts too long

-We switch-off this payload on NASA SW solar flare warning

Space Weather operation on CALIPSO

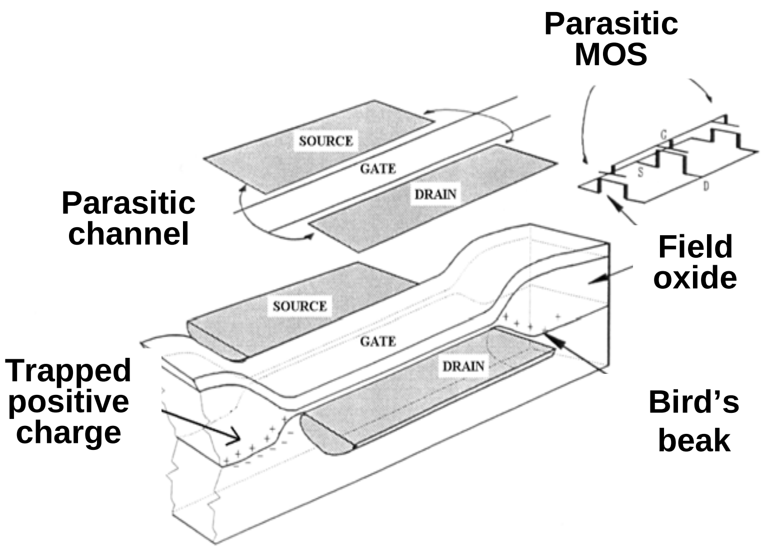
- **12.07.06**: We received notification of a space weather 100 MeV warning at 7:11 PM on Wednesday, 12.06.06. Because of this warning we have turned off the CALIPSO payload controller, and we expect that we won't resume operations before Monday, 12.11.06.
- **12.11.06**: The space weather forecast is improving and plans to resume CALIPSO operations are being finalized. Plans to resume operations follow:
  - December 12, 2006: Reactivate Payload Controller provided conditions remain less than 100 MeV
  - December 13, 2006: Apply power to laser system, Configure PL in Standby provided conditions are less than < 10 MeV. Resume data acquisition at earliest opportunity (late 12/13/2006 or early 12/14/2006).
- **12.12.06**: CALIPSO reactivation began today when the CALIPSO Payload Controller was successfully turned on at 12:14 UTC. A 10 MeV space weather alert remains in effect until 16:00 UTC today. The 10 MeV alert must be clear before further activation of the CALIPSO payload can be performed. We anticipate favorable conditions and plan to continue CALIPSO reactivation on December 13, 2006.
- **12.13.06**: Space weather conditions deteriorated overnight. The NOAA Space Environment Center issued 100 MeV and 10 MeV warnings and alerts at 03:00 UTC December 13, 2006. In response to these conditions, the payload controller was turned OFF at approximately 12:15 UTC 8:06 UTC December 13, 2006 as a precautionary measure. Space weather warnings at both the 10 MeV and 100 MeV levels remain in effect until 23:59 UTC December 13, 2006. It is possible that these warnings will be extended later today.
- **12.14.06**: Space weather conditions continue to be unfavorable for CALIPSO operation. Space weather 100 MeV and 10 MeV warnings remain in effect through at 01:00 UTC December 15, 2006 and we anticipate that these warnings will be extended later today. The solar activity forecast predicts at least a 75% chance of additional proton events through December 16, 2006 with NOAA sunspot Region 930 responsible for the elevated activity. Tentative plans are being developed to begin CALIPSO reactivation on Monday, December 18, 2006 and return to science operations with X-band data transmission on December 19, 2006. Correction (see change made below): The CALIPSO payload controller was powered OFF at 8:06 UTC on December 13, 2006 and not at approximately 12:15 UTC as initially reported.•
- **12.20.06**: CALIPSO resumed nominal data acquisition December 19, 2006 at 13:56 UTC. Payload performance is nominal based on a review of telemetry received last night and early this morning. CALIPSO will remain in nominal data acquisition until a planned drag make up orbit maneuver tentatively planned January 16, 2007.
- **01.12.07**: The CALIPSO payload will be out of service between 08:45 UTC on January 15, 2007 until 13:28 UTC on January 17, 2007. The down time is necessary so the CALIPSO satellite can perform a drag make up orbit maneuver to maintain its position in the A-train constellation and to perform a periodic check of the redundant CALIPSO laser system. The next scheduled outage will occur in support of an overall A-Train inclination manoeuver sequence with the first of three CALIPSO maneuvers tentatively scheduled on March 8, 2007.

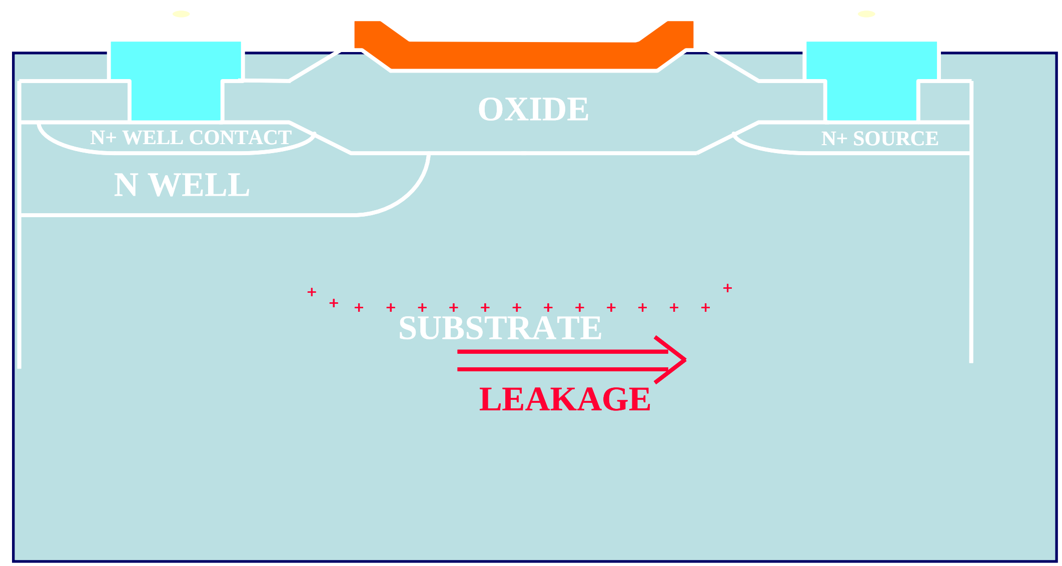
Effects of a major SW event (oct-nov 03)



Technological trends - dose

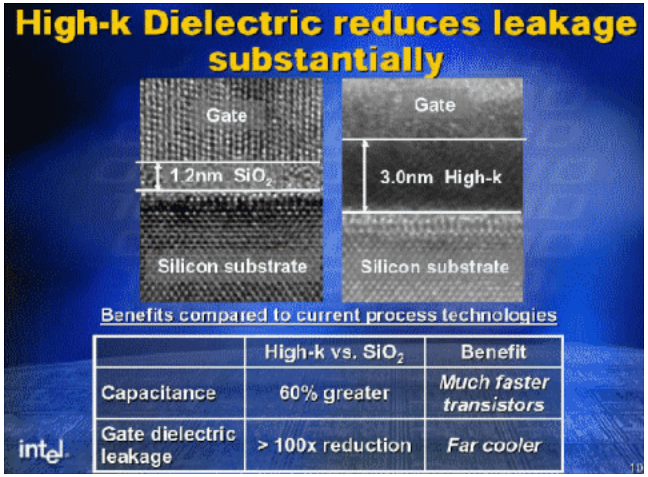
- In general, advanced technologies tend to have quite good TID figures
- Downscaling implies thinner gate oxides
  - favourable to better TID performance (less oxide traps)
  - lower gate leakage with dose
  - drawback : higher influence of interface states → rebound effects
- But reduction in spacing brings other mechanisms such as parasitic channel (source – drain leakage)



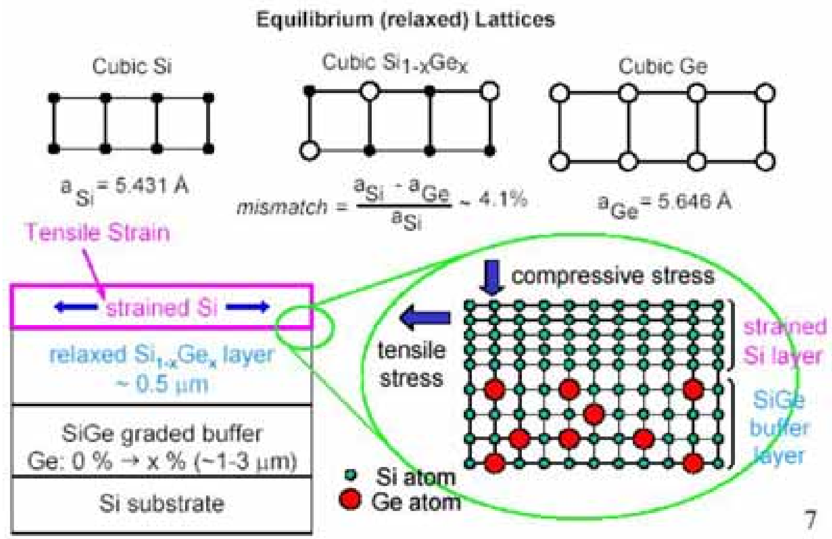


Technological trends - dose

- It has been observed that the use of nitride passivation has a strong negative impact on TID performance
  - mechanism still to be elucidated, probably related to H+ migration
- The (few) available results on high-k dieletric and strained silicon technologies do not show to date a negative impact of these features on TID performance



	High-k vs. SiO_2	Benefit
Capacitance	60% greater	Much faster transistors
Gate dielectric leakage	> 100x reduction	Far cooler



Technological trends - SEE

- Both VDD reduction and geometry downscaling lead to lower charges stored on the nodes Qnode=VDD x Cnode
- New generations have lower SEE threshold critical charges → higher SEU sensitivity
  - 1980's : heavy ions
  - 1990's : protons
  - 2000's : atmospheric and thermal neutrons

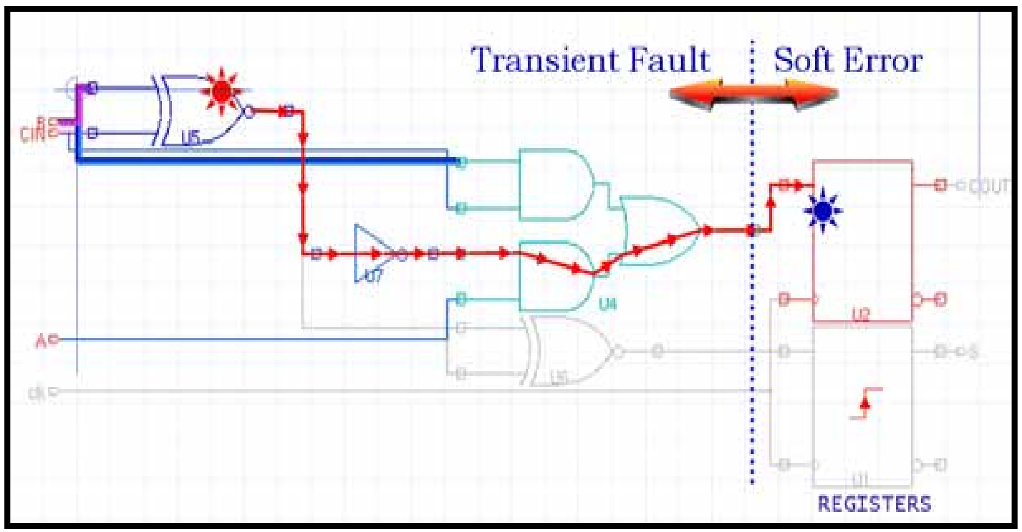
Conditions	FIT/Mb Neutrons	FIT/Mb alpha Am241	TOTAL
Sea level	1300	2200	3500
Alt.1500 m	3000	2200	5500

CMOS 0.13um, Los Alamos NSC

1000 FIT = 1 error per 114 years, for 128 Mbytes=> 1 error per 14 days at ground level

Technological trends - SEE

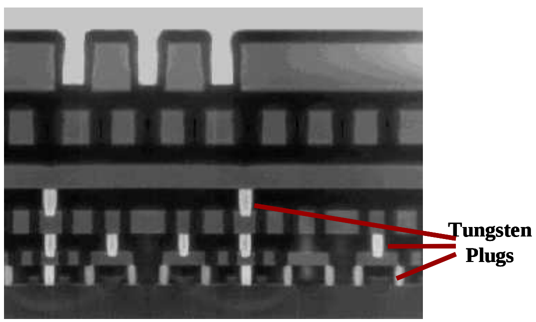
- More sensitive but harder to shoot at (smaller) targets
  - device SEU sensitivity more or less the same
  - i.e. for a sensitive memory, the surface of the die
- Transient pulses become larger than gate transition times and can propagate to outputs
- With frequency increase, probability of capture in latches increases



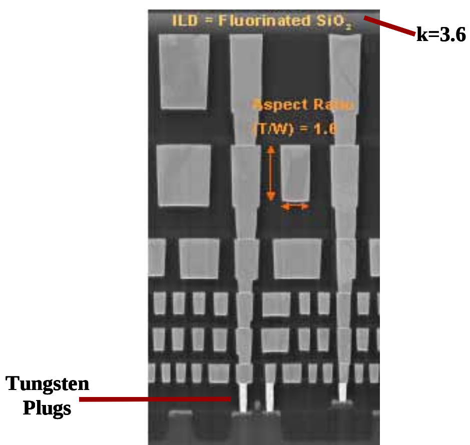
SER in combinatorial logic becomes comparable to SER in latches

Technological trends - SEE

- Good news :
  - crosstalk, substrate noise,… and atmospheric neutrons problems
  - brings interest of large manufacturers for SEU/SET mitigation
  - technology / internal coding or fault tolerant techniques
- Bad news (for rad-hard products)
  - use of tungsten interconnections
  - p+ / W interaction leads to high LET recoils
  - latent p+ SEU rate recently evidenced on some rad-hard devices
  - does not concern classical / commercial devices (already sensitive)



Intel 0.25µm Process (Al)
5 Layers - Tungsten Vias
Source: *Intel Technical Journal* 3Q98



Intel 0.13µm Process (Cu)
Source: *Intel Technical Journal* 2Q02

Dedicated instruments and experiments

- Space environment monitors
- Technology experiments

Space environment monitors

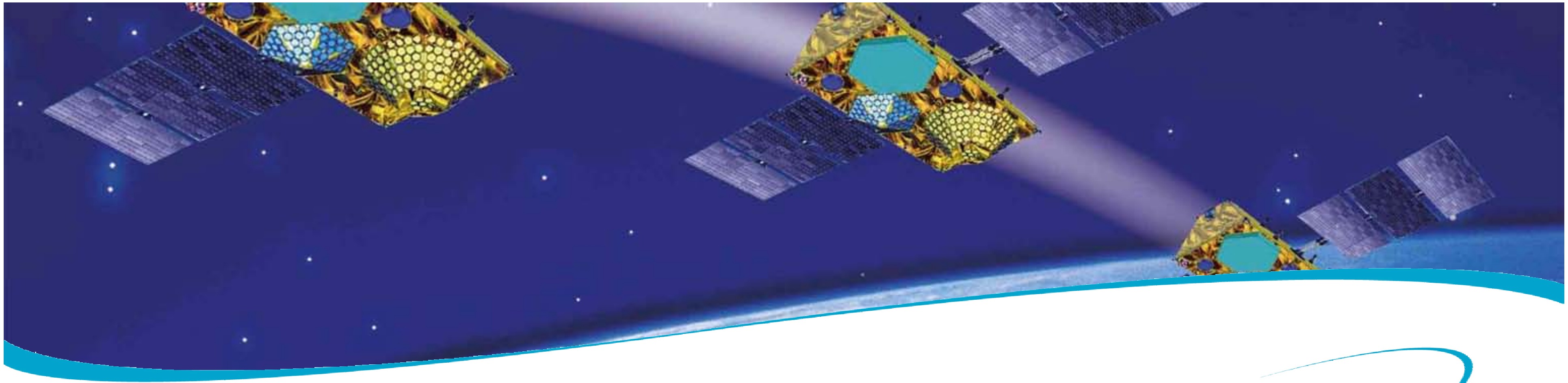
- Space environment monitors are of great help as witnesses of conditions during the anomaly
- Generic data from environment observatories (e.g. GOES, POES)
- Monitoring on the host satellite
  - “Black box” for future investigations
  - Particularly useful in GEO where conditions may vary with longitude

Technology experiments

- Technology experiments, e.g :
- SEE monitoring (SEU, SET, SEL, SEB,…) can give useful information
  - on the raw SEE rate on devices before system filtering
  - and thus give an idea of the raw level of perturbation
- Dosimetry and/or dose drift measurements can give information
  - on the actual dose level received and state of components
  - on remaining lifetime
  - provide anticipation on possible recovery techniques

Conclusions

- Radiation-induced spacecraft anomalies have been observed since the very beginning of the space era
- Radiation effects anomalies have their origin at the component level but the observed anomaly is a system response
- Radiation effects knowledge is a tremendous added value for engineering anomaly way-outs (e.g. JPL / Galileo)



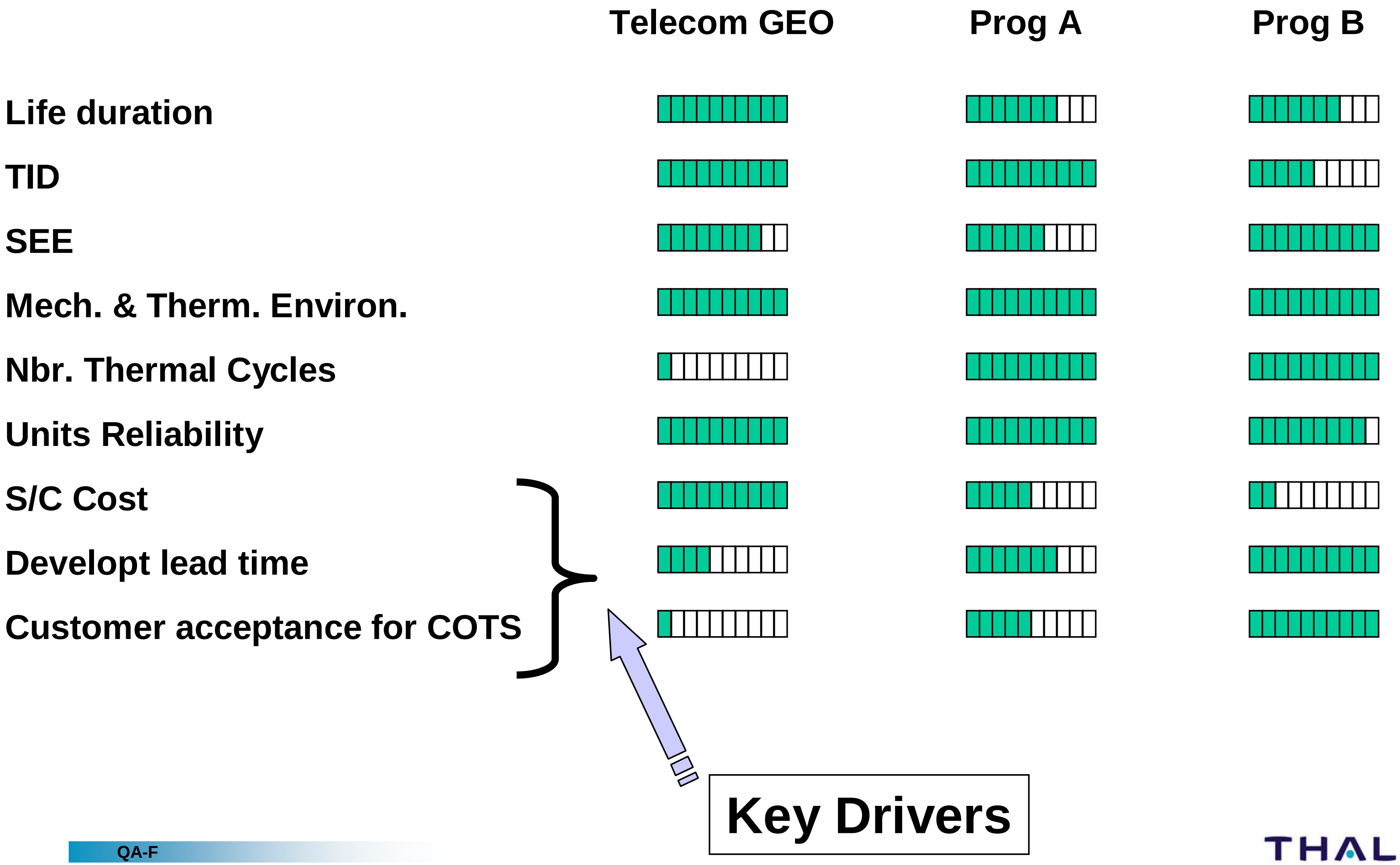
Challenges and Opportunities for EEE parts in Constellations,

O. Rémondière, Y. Folco – ESCCON 2011, 15-17/03/2011 @ ESTEC

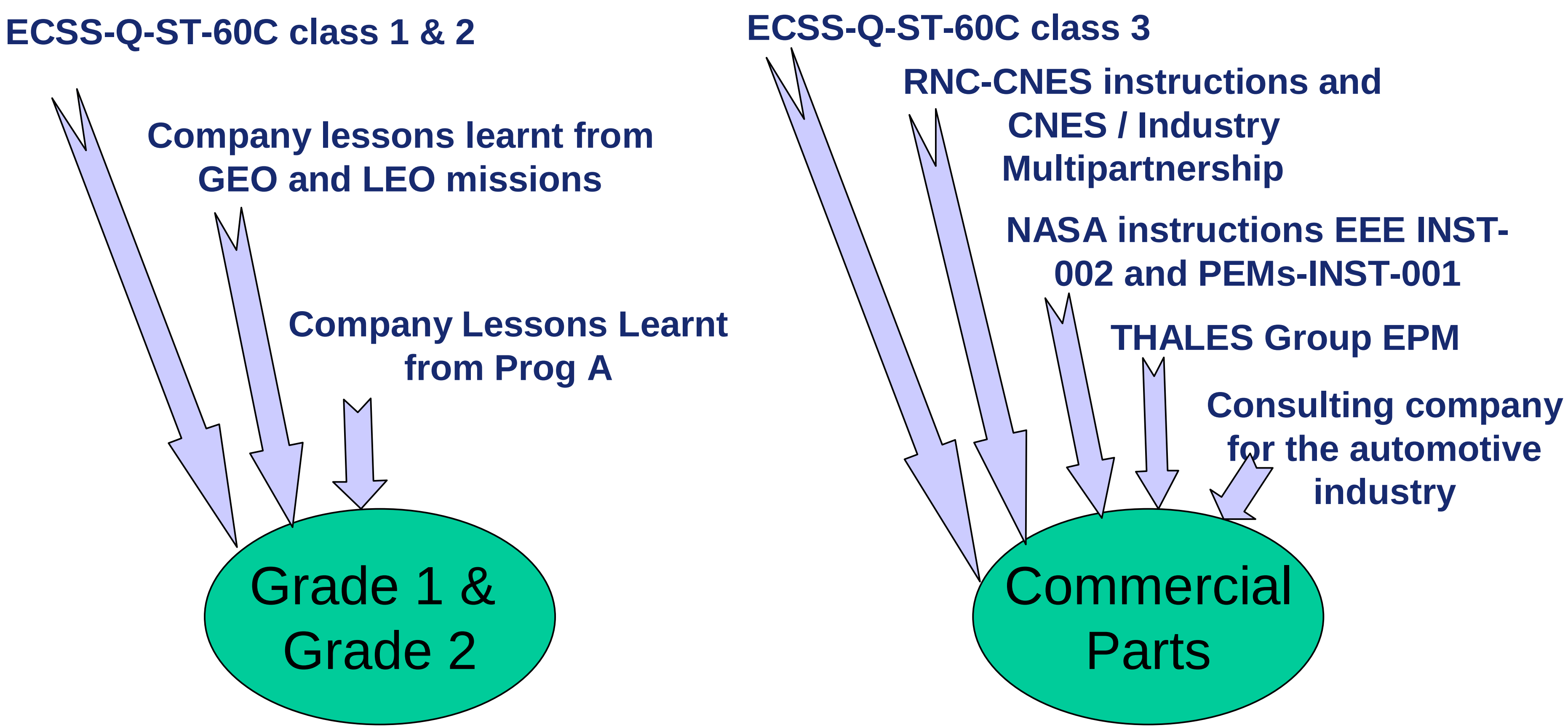
Template reference : 100181703F-EN

- Drivers for EEE parts policy
- ThalèsAleniaSpace EEE parts policy for Constellations
- Consequences
- Risks
- Conclusions

Drivers for EEE parts policy



Where is it coming from ?



TAS EEE parts Policy

Telecom GEO	PROG A	PROG B
Parts Management Process : Per ECSS-Q-60 class 1	Parts Management Process: Per ECSS-Q-60 class 1 & 2 equivalent	Parts Management Process per ECSS-Q-60 class 2 & 3 equivalent
Class 1 / Grade 1, mandatory for : ALL PARTS	Class 1 / Grade 1, Mandatory for : Crystal Oscillators, Crystals, Hybrids from non space qual line, EMI filters Electromagnetics Relays, Tantalum chips capacitors, Stacked ceramic chips capacitors, Cermet Fuses , Connectors at equipement interfaces	Class 1 / Grade 1, Mandatory for: Crystal Oscillators, Crystals, Hybrids from non space qual line, EMI filters, Electromagnetics Relays, Tantalum chips capacitors, Stacked ceramic chips capacitors,, Cermet Fuses, Connectors at equipement interfaces
Grade 2: NO PARTS	Grade 2 minimum : Microcircuits , RF active devices , Rectifier, Zener, Signal Diodes, Bipolar transistors, arrays, FET, JFET, Power MOSFET, Opto-couplers, Hybrids from MIL QPL, Some passive parts (Interesting for re-use of existing design , originally populated with Grade 1 parts)	Grade 2 minimum : Thermistors, Connectors and Contacts, passive parts, Hybrids from space qual lines (an all other functions if Interesting for re-use of existing design , originally populated with Grade 1 parts)
COTS: NO PARTS	COTS allowed on case by case basis (performance): Few Microcircuits and RF active devices	COTS allowed as general policy : PEMs and PEDs (all functions): Packaged Microcircuits including MMICs; Rectifier, Zener, Signal Diodes; Low power Bipolar, FET, JFET, transistors arrays, Commercial I.R power MOSFET, Opto-couplers

General Policy

- To offer the best compromise between Risks, Quality and Cost
- To consider alternative policies applied on similar programs from sub-contractors
- To allow the use of grade 1, grade 2 and COTS
- Proposals with key components preliminary Parts List , Parts heritage and contractor policy for COTS screening

Evaluation and Qualification Policy for PEMs and PEDs

- The requirements provide - in base line - a qualification test flow (adapted from NASA / CNES flow)
- Alternative approaches such as Manufacturer qualification data or Sub-contractor proposal based on Internal parts policies for similar programs are acceptable. In both cases, two first Go / No Go criteria for lot acceptability are:
  - Successful Radiation tests or data
  - Constructional analysis.

Screening Policy for COTS

- The requirements provide 3 options regarding youth defect parts elimination
  - 100% Screening. When feasible, Test flow and sensitive parameter tables are provided
  - Justification based on Manufacturer SPC data
  - Burn-In and/or Cycling tests at PCB assembly or at Equipment level
- Alternative proposals from sub-contractor for similar programs are acceptable

Pure Tin issues with COTS

- PEMs and PEDs comes from RoHs fabrication lines (Pure tin terminals)
  - Tin whiskers can develop and create short circuits
  - The Contractor shall propose mitigation strategies to prevent whiskers induced failures
  - The requirements provide Guide lines for Pure Tin risk mitigation

Commercial Parts Procurement and Obsolescence management

- The requirements provide cost oriented guide lines
  - Procurement in single lot preferably ➡ One test campaign
  - Procurement for the total needs of the program ➡ COTS life cycle is incompatible with the program duration
  - Huge quantities needed . (More than 40 000 for one PEM for example)

Consequences

Consistency of all PA requirements is key to enable the use of COTS

- **Reliability and Failure rate predictions have to be adapted to take benefit from COTS**
  - Unit and Parts life time demonstration is a matter of evaluation and qualification
  - Unit Failure Rate is a matter of prediction
    - Based preferably on TAS tailoring of MIL-HDBK-217 from Lessons Learnt
    - Or on Sub-Contractor proposed approach
- **Mounting processes Qualifications have to be adapted and complemented for PEMs**
  - Storage, mounting, rework and repair (IPC/JEDEC J-STD-020A)
  - Mounting process validation per Lot
  - Tin whiskers mitigation at PBA level
  - Demonstration of Inspection efficiency and / or Process Control for Grid Arrays
  - Specific validation for Glob Top technologies / 3D technologies

Risks	Mitigation
Lack of experience related to COTS selection and management	Support from Thales Group EPM . Thales PPL Access Mapping of COTS selection from contractors versus Thales PPL entries and current status (Qual, EOL, etc) Contractor heritage and running programs with COTS
Lack of Engineering support to review and approve Justification Files	To ensure enough resources at Prime and Contractors level early in the Program
Late « showstopper » during part validation wrt Unit developement	To approve very early the parts selection in order to allow early unique batch procurement and validation before freezing the design
Support from Manufacturers in case of problems	Early and full validation of the lots allowing back-up strategies in case of issues
COTS Obsolescence	Procurement for the entire program and improved storage conditions
Tin Whiskers	State-of-the art risk mitigation guidelines included in the requirements
100% reliable traceability	To procure as far as possible from OEM. To get from the supplier all the available traceability elements

Conclusion

Good feedback from the market during PROG B RFPs for Units

- Requirements are understood
- Positive Feed-back from equipment manufacturers involved on previous constellations program
- 95% of proposals received with key components preliminary parts lists.
- When COTS are proposed, their management are fitting with expectations
- Generally, proposals are taking benefits from the requirements to offer high performance at low cost

EUROPEAN SPACE COMPONENT CONFERENCE

ESCCON 2011

THE EXPERIENCE OF COMMERCIAL COMPONENTS

INSERTION IN PEM (GAIA PROGRAM)

P. Peres / A. Gomez – 16 March 2011

WHY COMMERCIAL COMPONENTS ?

- The demanding performances of the GAIA-PEM (Proximity Electronic Module) made necessary the use of commercial components for several critical functions.

- Driving requirements for GAIA-PEM design are :
  - In first place, electrical performances :
    - Low noise
    - Power dissipation stability
    - Limitations in power dissipation
    - Very tight timing uncertainty
  - Limited volume and weight
  - Minimum interconnections

HOW COMMERCIAL COMPONENTS HAVE BEEN SELECTED ?

- The selection of these components has been made along the different R&D activities.
- During these studies it has been analysed many alternatives for each function looking for a radiation tolerant, at least evaluated or used in previous missions.
- The most relevant components have been included in different design alternatives, assembled and characterised with respect to their main relevant parameters influencing the PEM performances.
- No space or military qualified component has been identified to meet the PEM performances.

WHAT WE DID ?

- Collaboration within Astrium (Spain & France) for the selection, procurement and use of commercial components.

- Selection process based on procedures commonly built by the French multi-partnership :
  - Guidelines on the use of parts out of manufacturers specified temperature range (up rating) : RNC-CNES-Q-60-511
  - Selection procedure for electrical, electronics and electromechanical (EEE) commercial components intended to be used in space applications : RNC-CNES-Q-60-514

- Components selection :
  - Identification of commercial candidates (including back up)
  - Preliminary assessment
  - Risk analysis
  - Proposed commercial components baselines

WHAT TYPES OF COMMERCIAL COMPONENTS HAVE BEEN ANALYZED ?

- More than 60 video operational amplifiers, rail to rail and single supply voltage, providing very low noise and low input offset voltage and input bias current.

  Identified candidate : AD 8028

- More than 50 ADC's providing 16 bit or better resolution, preferably SAR architecture with no pipeline delay and with conversion time faster that 1,2 us.

  Identified candidate : AD 7621

- More than 15 analog switches, providing low R_{on}, fast switching time, and low and single supply voltage.

  Identified candidate : MAX 313, 1st back up candidate : ADG 451, 2nd back up candidate : SWI ISL43110

- Several fast clock drivers.

  Identified candidate : EL 7457

- Multiple, preferable octal or larger, 8-bits DACs.

  Identified candidate : MAX 521 (back up candidate : AD 7228)

GENERIC POLICY FOR COMMERCIAL COMPONENTS APPROVAL (1)

1) TO COMPLETE A JUSTIFICATION DOCUMENT (JD)

- To collect available data on the commercial components (general information, literature, supporting data on previous lots, data sheet)
- To define an evaluation plan (including radiation tests)
- To define the screening flow of the FM lot.

2) TO PROCURE THE FM LOT

- The FM lot is procured, according to manufacturer data sheet.

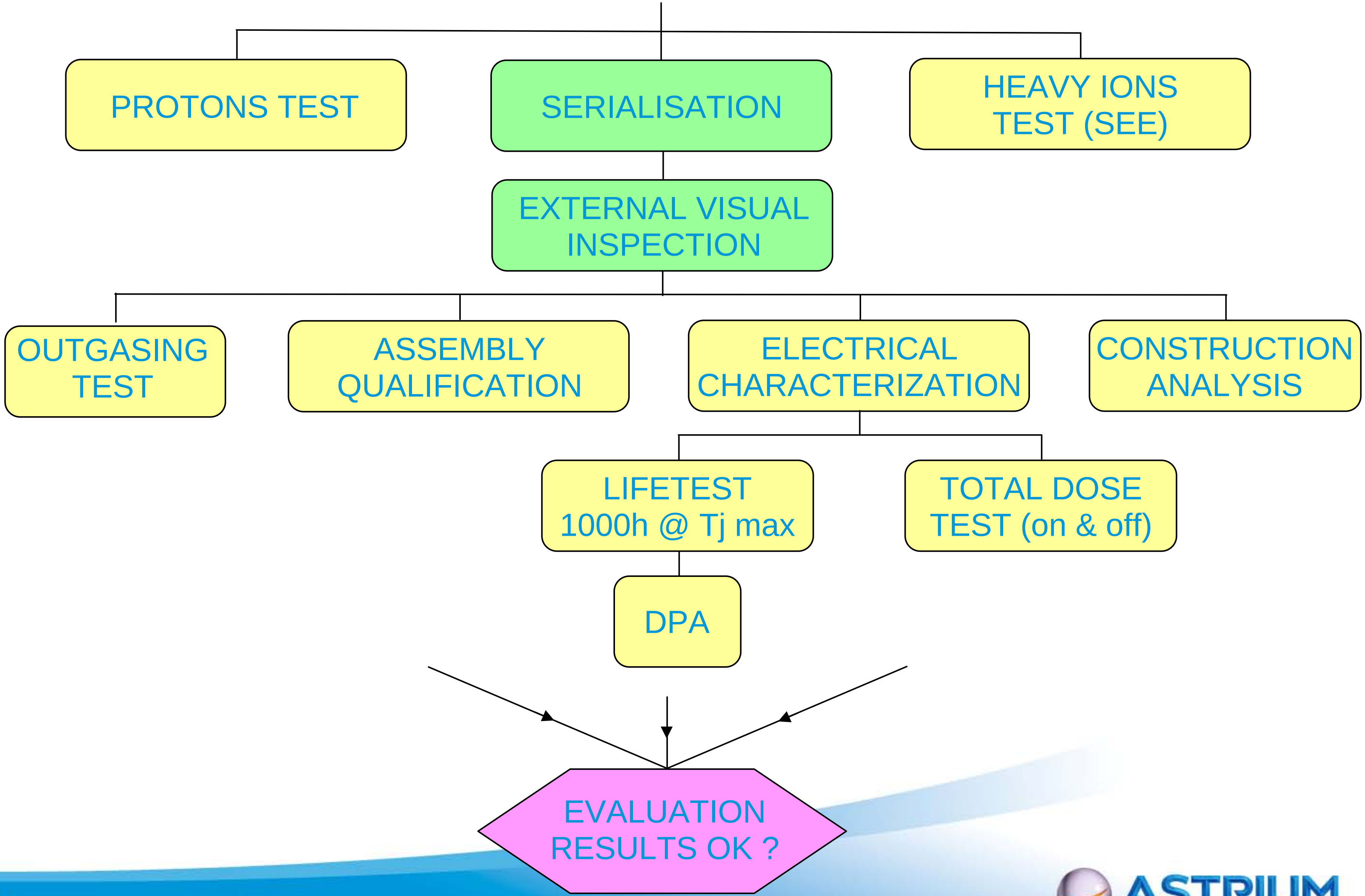
3) TO PERFORM AN EVALUATION OF THE FM LOT

- The evaluation of the FM lot is performed, according to the JD plan and to the risk analysis raised to identify the most urgent tests to be done (SEE, constructional analysis, life test, out gassing…).

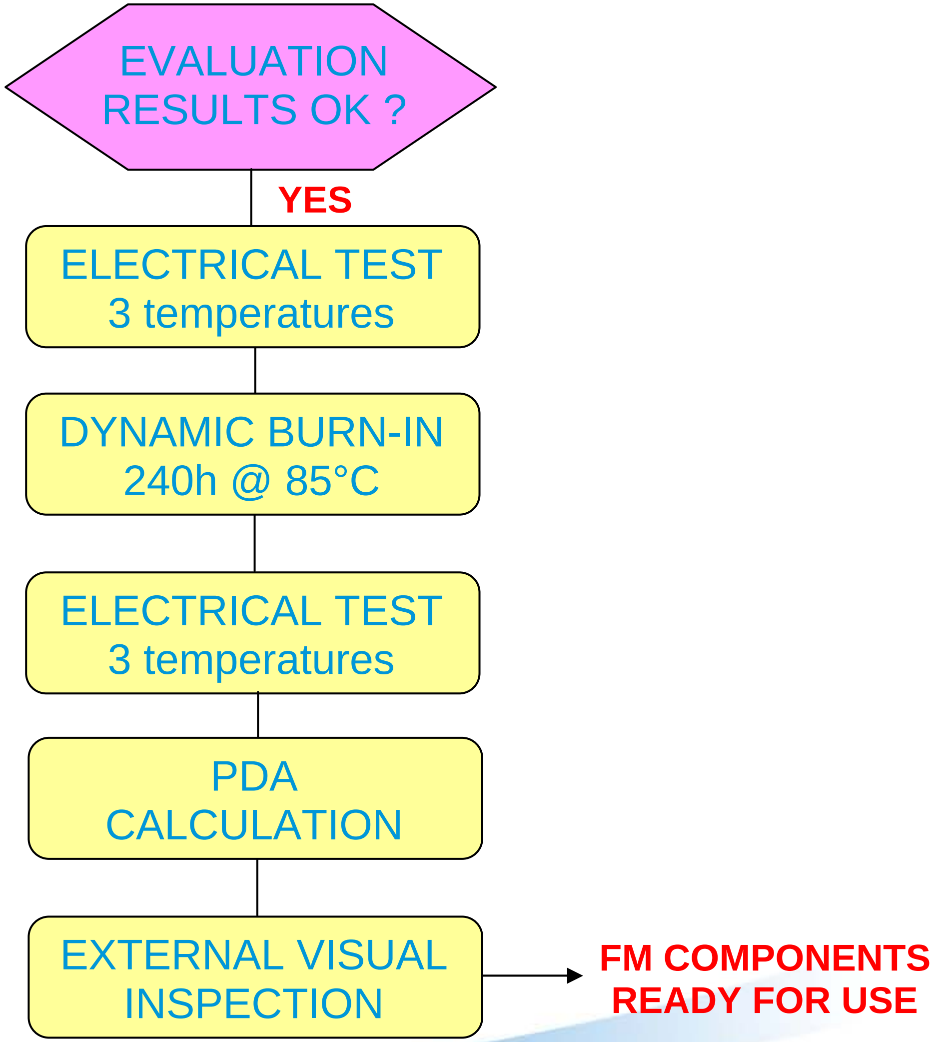
4) TO SCREEN THE WHOLE FM LOT

- The FM lot is screened by the user (based on the evaluation results)
- Since evaluation is done on the FM lot, no additional LAT is requested

GENERIC EVALUATION FLOW CHART



GENERIC SCREENING FLOW CHART (BY USER)



JUSTIFICATION DOCUMENTS
RESULTS OF THE SELECTION

FUNCTION	TYPE	MNFCT	CASE	TEMP RANGE	RISK ANALYSIS CONCLUSIONS
VIDEO AMPLIFIER	**AD8028AR**	AD / US	SOIC 8	-40°C/+125°C	- AD major manufacturer = no risk for front / back end - Transient sensitivity
ANALOG SWITCH	**MAX313L**	MAX / US	SOIC 24	-40°C/+85°C	MAXIM = risky manufacturer => CA to be anticipated
ANALOG SWITCH (Back up)	**ADG451BR**	AD / US	SOIC 16	-40°C/+85°C	- AD major manufacturer = no risk for front / back end - TID (at VLDR) - Transient sensitivity
CLOCK DRIVER	**EL7457CS**	INT / US	SOIC 16	-40°C/+85°C	Urgent CA to identify mask reference for SEL test
ADC	**AD7621AST**	AD / US	LQFP 48	-40°C/+85°C	AD major manufacturer = no risk for front or back end
DAC	**MAX521 BEWG**	MAX / US	SOIC 24	-40°C/+85°C	MAXIM = risky manufacturer => CA to be anticipated

EVALUATION RESULTS
DIE & PACKAGE

TYPE	PROCURED LOT	CONSTRUC-TION ANALYSIS	OUT GASSING	ASSY QUALIF	EVAL. RESULTS
AD 8028	One DC	OK	OK	OK	OK
MAX 313	One DC	FAILED	Not done	Not done	REJECTED
ADG 451	One DC	ACCEPTABLE	OK	OK	OK
EL 7457	One DC	OK	OK	OK	OK
AD 7621	One DC	OK	OK	OK	OK
MAX 521	One DC	OK	OK	OK	OK

EVALUATION RESULTS
ELECTRICAL & ENDURANCE

TYPE	ELECT. CHARACT. @ -40°C, 25°C, 85°C,125°C	DYNAMIC LIFE TEST	ELECT. TESTS AFTER LT @ -40°C, 25°C, 85°C,125°C
AD 8028	Acceptable	1000H @ 125°C	0 reject
ADG 451	Acceptable	1000H @ 125°C	0 reject
EL 7457	Acceptable	1000H @ 105°C	0 reject
AD 7621	Acceptable	1000H @ 115°C	0 reject
MAX 521	Acceptable	1000H @ 125°C	0 reject

EVALUATION RESULTS
TOTAL DOSE (RVT)

		DOSE RATE	TID RESULTS
VIDEO AMPLIFIER	**AD 8028 AR**	140 Rad(Si) / h	OK up to 30 Krad
ANALOG SWITCH	**ADG 451 BR**	LDR = 40 Rad(Si) / h VLDR = 3.3 Rad(Si) / h	LDR: Is (OFF) < 0.6 Krad VLDR: Is (OFF) < 0.3 Krad
CLOCK DRIVER	**EL 7457 CS**	40 Rad(Si) / h	OK up to 30 Krad
ADC	**AD 7621 AST**	140 Rad(Si) / h	OK up to 30 Krad
DAC	**MAX 521 BEWG**	40 Rad(Si) / h	OK up to 30 Krad

EVALUATION RESULTS
HEAVY IONS & PROTONS

	SEL or SEB/SEGR	SEU	SET	PROTONS
AD 8028	SEL Insensitive	Insensitive	Sensitive	Insensitive up to 190 MeV
ADG 451	SEL Insensitive	Insensitive	Sensitive	NA
EL 7457	SEB sensitive SEGR Sensitive	Insensitive	Sensitive	NA
AD 7621	SEL Insensitive	SEU sensitive SEFI sensitive	Insensitive	Insensitive up to 190 MeV
MAX 521	SEL Insensitive	Sensitive	Sensitive	NA

SCREENING RESULTS

	ELECTRICAL TESTS BEFORE BI @ 3 T°	DYNAMIC BURN IN	ELECTRICAL TESTS AFTER BI @ 3 T°
AD 8028	OK (1 reject)	240H @ 85°C	OK (0 reject)
ADG 451	OK (0 reject)	240H @ 85°C	OK (0 reject)
EL 7457	OK (1 reject)	240H @ 85°C	OK (0 reject)
AD 7621	OK (11 rejects)	240H @ 85°C	OK (7 rejects)
MAX 521	OK (0 reject)	240H @ 85°C	OK (0 reject)

SYNTHESIS OF EVALUATION AND SCREENING RESULTS

		PROC LOT	EVALUATION RESULTS	RVT	SEL or SEB/SEGR	SEU	SET	SCREENING
VIDEO AMPLI	AD8028	One DC	OK	OK up to 30 Krad	SEL Insensitive	Insensitive	Sensitive	OK
ANALOG SWITCH	MAX313	One DC	LOT REJECTED (MAVERICK LOT)					
ANALOG SWITCH	ADG451	One DC	OK	Sensitive (VLDR)	SEL Insensitive	Insensitive	Sensitive	OK
CLOCK DRIVER	EL7457	One DC	OK	OK up to 30 Krad	SEB/SEGR Sensitive	Insensitive	Sensitive	OK
ADC	AD7621	One DC	OK	OK up to 30 Krad	SEL Insensitive	SEU + SEFI sensitive	Insensitive	OK
DAC	MAX521	One DC	OK	OK up to 30 Krad	SEL Insensitive	Sensitive	Sensitive	OK

EXPERIENCE AFTER EQUIPMENTS MANUFACTURING

1) 110 FM Proximity Electronic Modules (PEM) manufactured
2) 96 FM PEMs already tested
3) Feed back after components mounting :
   - No problem during mounting
4) PEM electrical performances
   - PEM qualification : successful
   - No application temperature highest than Tmax :
     - +60ºC during qualification (QM)
     - +55ºC during acceptance (FM).
   - Electrical tests at PEM level showed no drift and a good reproducibility of performances

CONCLUSION - COST SYNTHESIS

- Cost of components selection : (Initial engineering activities, data collection, results analysis, Justification Document completion)	350 K€	(27%)
- Cost of components procurement : *8 types & 8900 components procured* *5 types & 2688 available components for FM*	50 K€	(4%)
- Cost of tests activities : (Evaluation, screening, radiations, …)	900 K€	(69%)
TOTAL AMOUNT (cost of ownership)	1300 K€	

CONCLUSION - OVERALL EXPERIENCE (1)

- The selection of commercial components has been done for performance reasons (access to high capacity or speed) results in higher performing, reduced size and lighter equipments with less interconnections.
- Successful approach by combining evaluation and lot acceptance test on the FM lot :

  => It reduces the risk of quick evolution of mask & technology between evaluation and procurement of flight components.
- In 5 of 6 cases => the lot qualification results have been successful.
- Successful management of traceability w.r.t. radiation.
- The use of commercial components induces a lot of engineering activities (selection, JD, evaluation, …) generating very high non recurring cost :

  => **don't use commercial components for cost saving !**

CONCLUSION - OVERALL EXPERIENCE (2)

The non-availability of high performing and high reliability EEE components for the GAIA mission imposed the use of commercial components.

This has been positively proven on a few types.

Strength	Weakness
▪ Electrical performances incomparable vs HI REL components ▪ Low mass and small packages ⇒ SMALLEST & LIGHTEST EQUIPMENTS	▪ Many products on the market ⇒LONG PRELIMINARY SELECTION ▪ Unknown reliability and radiation behaviour ⇒ BACKUP SOLUTIONS REQUESTED ⇒ HARD AND RISKY EVALUATION TO BE DONE ⇒ HIGH FINAL COST ⇒ SCHEDULE / DESIGN IMPACTS WHEN EVAL. FAILS ▪ Components storage (Nitrogen) ▪ Preliminary cost evaluation

DON'T BE AFRAID TO USE COMMERCIAL EEE COMPONENTS IN CASE YOU NEED HIGH PERFORMANCES

BUT

DON'T BELIEVE YOU WILL SAVE MONEY BY USING COMMERCIAL EEE COMPONENTS

THANK YOU FOR YOUR ATTENTION

ESCCON 2011

ESCC Evaluation and Qualification Programmes

J. Howley, Enterprise Ireland
G. Joormann, DLR Köln
J. Wong, ESA ESTEC

ESCC Evaluation and Qualification Programmes- The ESCC System

European space programmes need stable sources and supply of components

- **The ESCC System is centrally positioned to address this need**
  an international system for the specification, qualification and procurement of EEE components for use in Space programs

- **ESCC Specification System**
  - **the technical specification of EEE components**
  - **methodologies for component evaluation and qualification**
  - **testing methods / quality assurance / operational provisions**

It offers a degree of autonomy for its component technology requirements and forms a basis for development and growth

All ESCC Specifications are freely available from the ESCIES web site. The web address is *https://escies.org*.

ESCIES
European Space Components Information Exchange System

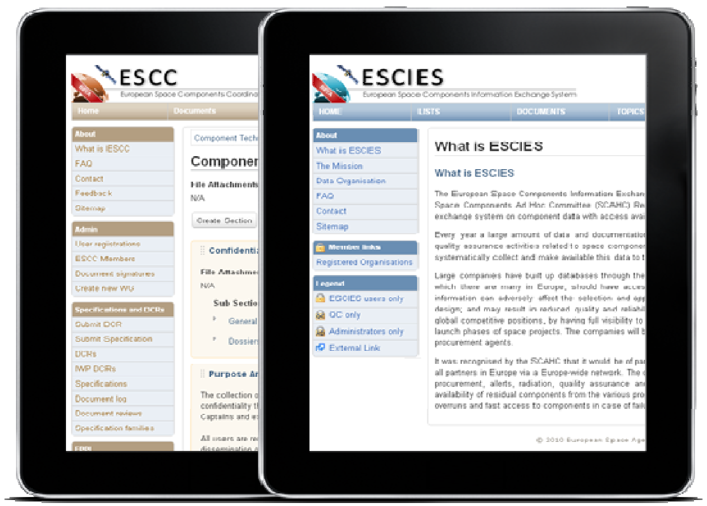
ESCC Evaluation and Qualification Programmes- The ESCC System

Sole purpose of the ESCC System is to provide components for space applications.

- A key objective is to improve the availability of strategically important EEE components

- It prefers European sources offering competitive performance and costs

- Key Products include:
  - ESCC specification system
  - Quality assurance infrastructure
  - Qualified Parts List
  - Qualified Manufacturers List
  - European Preferred Parts List
  - ESCIES and Spacecomponents.org

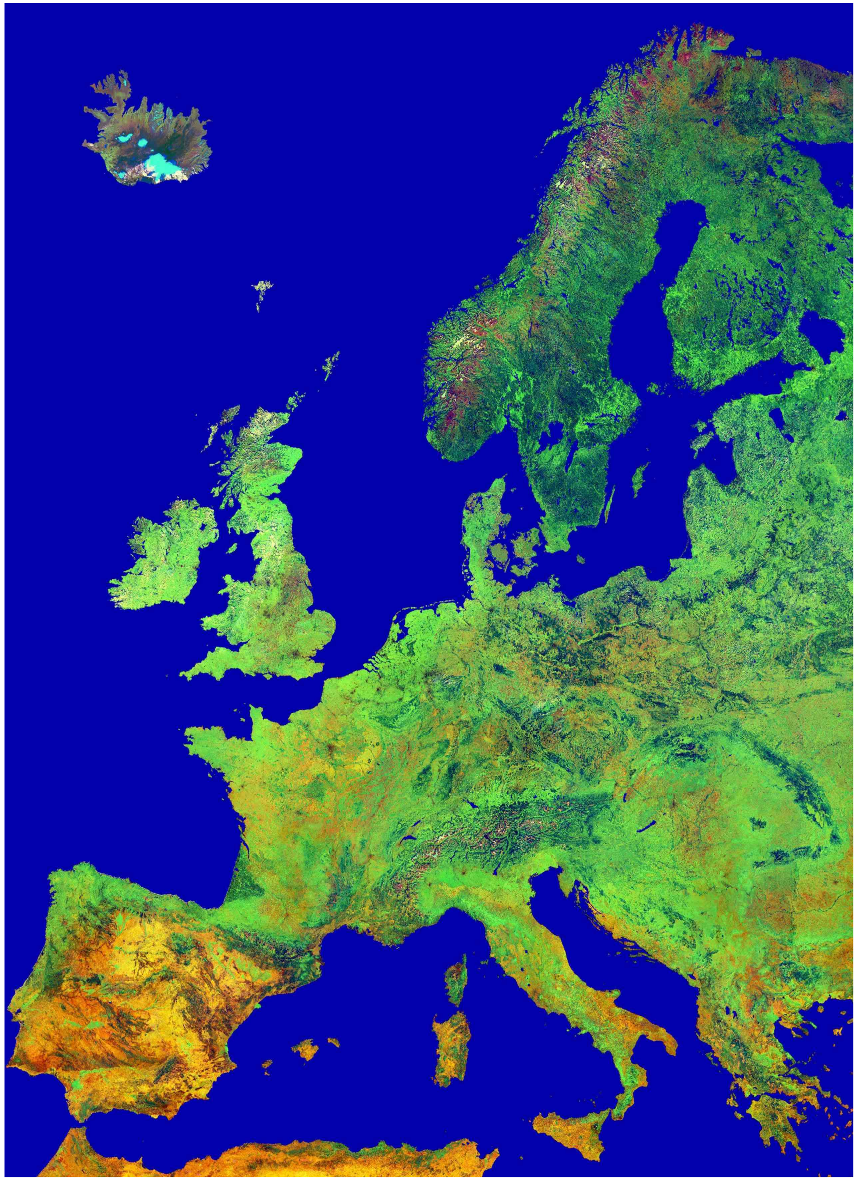


ESCC Evaluation and Qualification Programmes- The ESCC System

ESCC is a unified and single European system for space component specifications and the corresponding qualification and certification activities.

➢ The System is supported by the signatories to its Charter and its partners contribute resources with their own funding

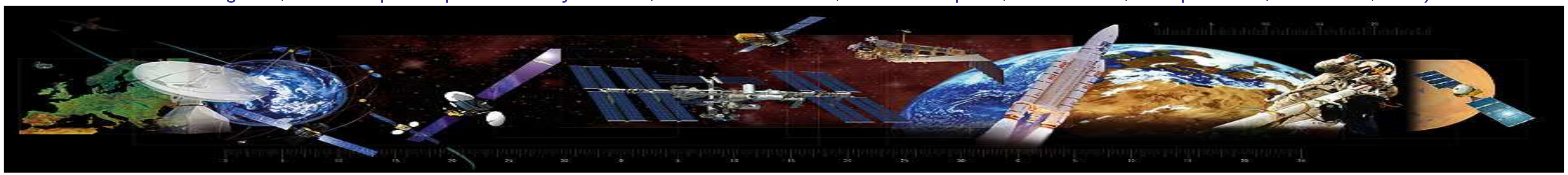
➢ The Space Components Steering Board (SCSB) is the penultimate body to contribute and supervise the resources to achieve its stated objectives



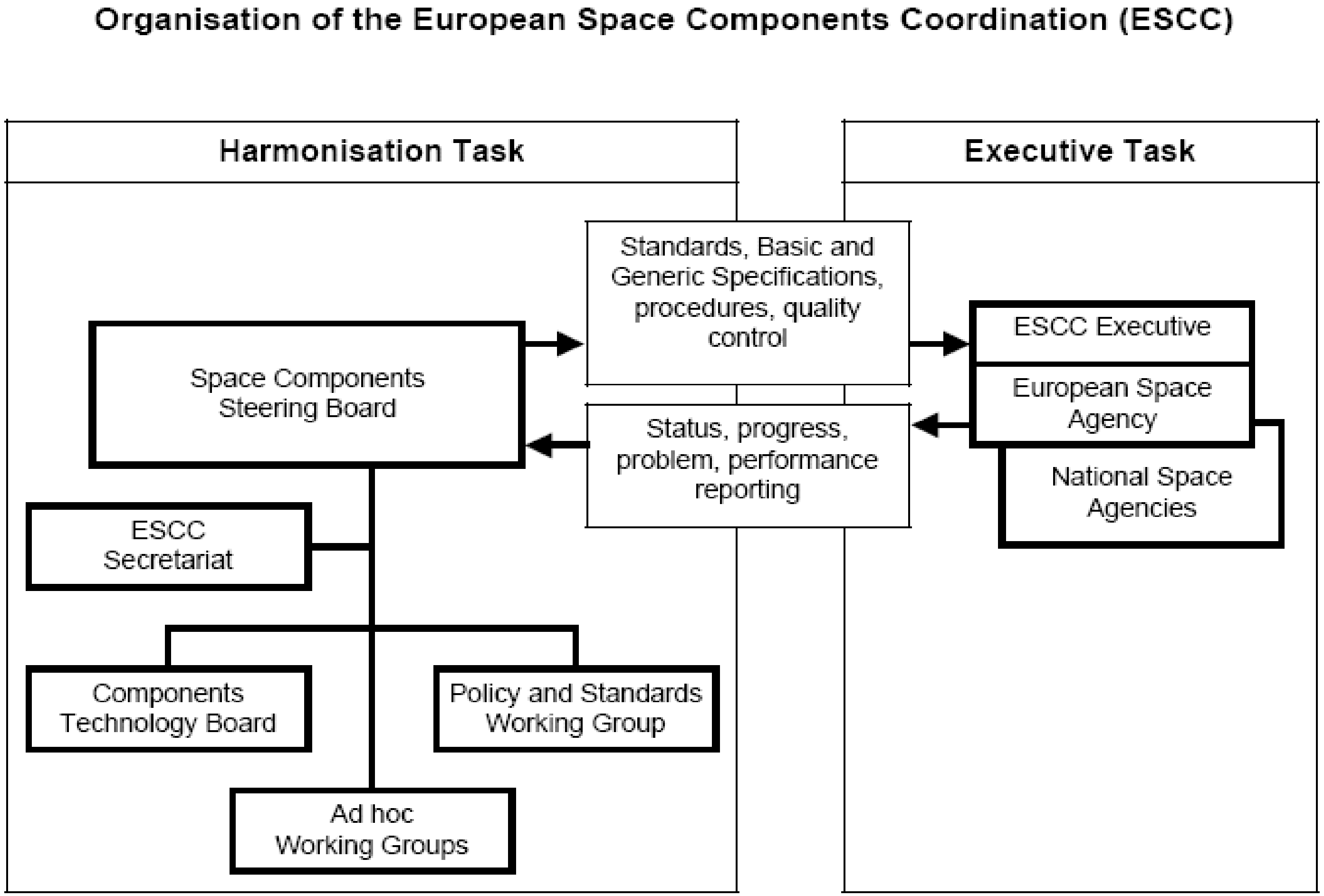
ESCC Evaluation and Qualification Programmes- The Perspective

Segment	Programmes	No. of Companies	M€/year	Export, %	ESA %
Total			5,359	49.9[2]	
Satellite Applications		118	3,081	36.8	21.1
	Telecomm.		1,940	49.9	7.1
	Earth Obs.		938	16.9	36.8
	Navigation		204	-	82.9
Launchers		26	1,069	2.0	-
Science			821	6.5	81.4
	Science		443	-	70.4
	Human Space		342	-	93.6
	Microgravity		36	-	Mainly ESA
Ground Segment		48	387	9.8	-
	EGSE/MGSE		46	28.3	15.2
	Ground Stations		246	8.9	31.7
	Services		95	3.2	-
ESCC System					
	European Space Components	**45 (1180 employees)**	**Est. > 240**	N/A	N/A

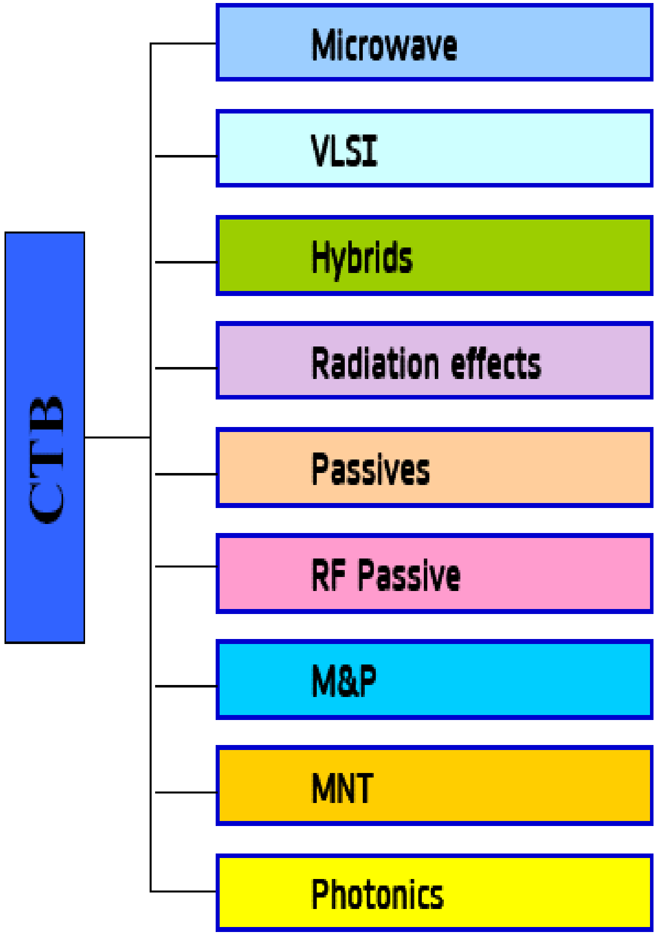
Facts and Figures, The European space industry in 2009, Public Issue No. 1, ASD-Eurospace, 2010-06-18, except ESCC, L. Bonora, ESA)



ESCC Evaluation and Qualification Programmes- The ESCC



ESCC Evaluation and Qualification Programmes- CTB



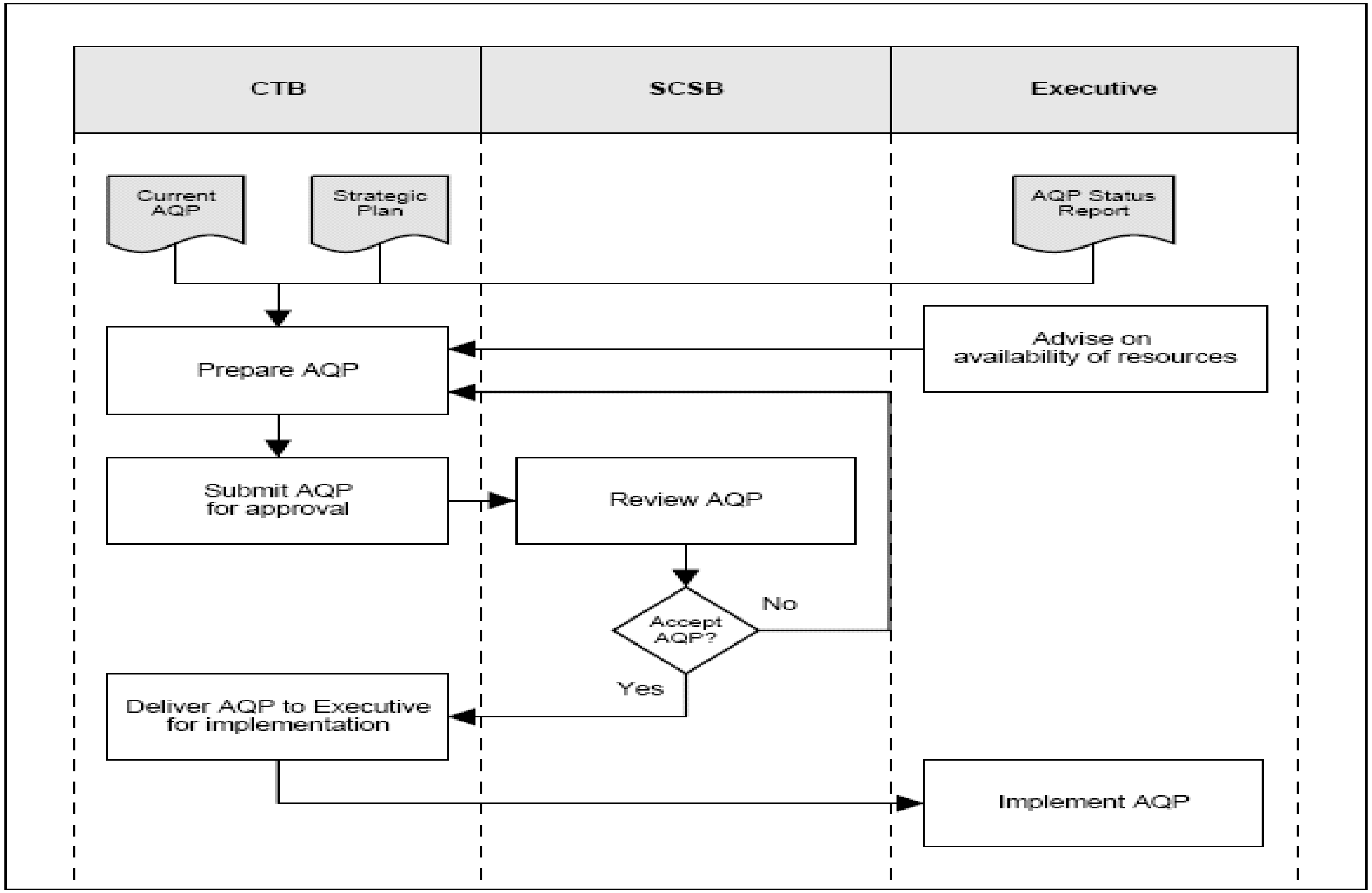
Formulates Programmes for Research and Development of EEE Components,
e.g., in the areas of:

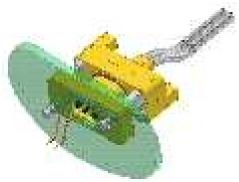
- o VLSI and Silicon Technologies
- o Hybrids and Packaging
- o Microwave Technologies
- o Micro-Nano Technologies
- o Materials and Processes
- o Photonics
- o Radiation Effects and Engineering Tools
- o Passive Technologies
- o RF Passive Technologies

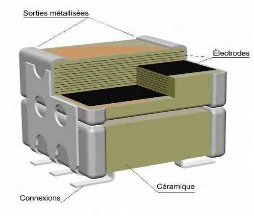
➢Leads to formulation of the Annual Qualification Programme (AQP)

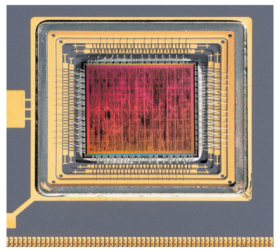
➢Based on technology specific dossiers

ESCC Evaluation and Qualification Programmes- Formulation









ESCC Evaluation and Qualification Programmes- Executive

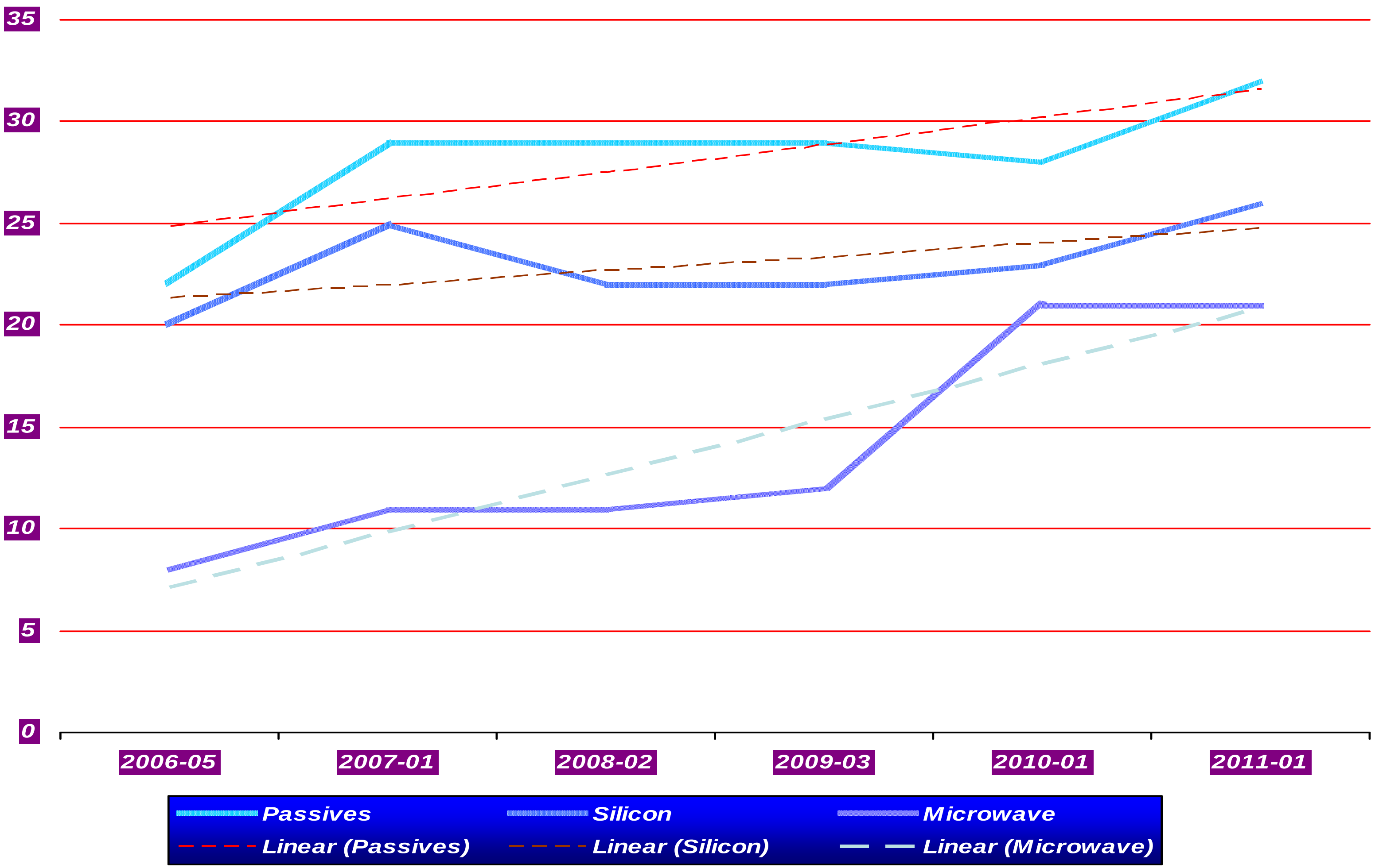
The CTB combines the collective participation and needs of European industry, manufacturers capabilities and space agencies for electrical, electronic and electromagnetic (EEE) components in one organization.

It establishes a coherent set of plans that aim to secure standard and strategic components through R & D programs, technology roadmaps and strategic dossiers, including

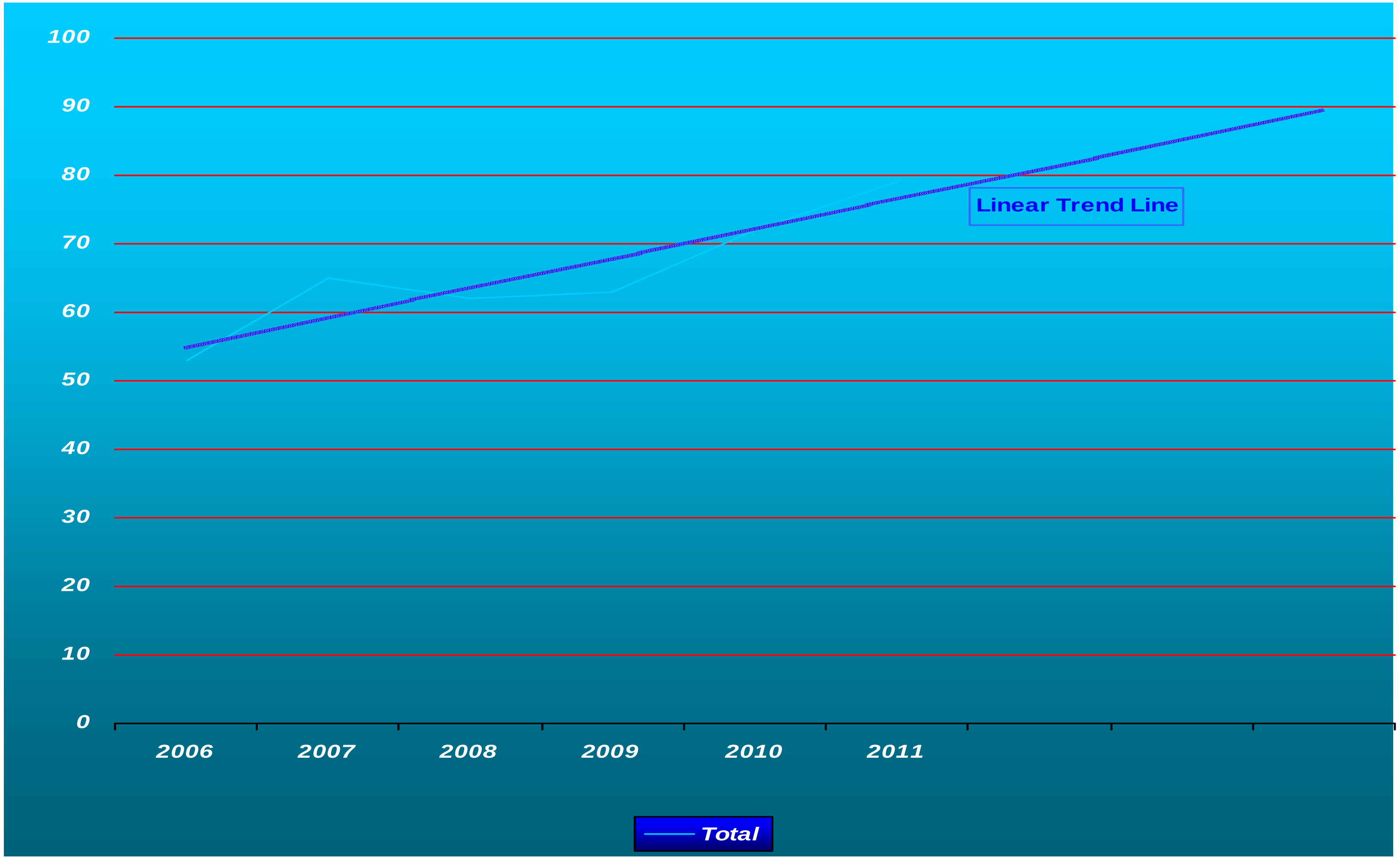
- an Annual Qualification Program (AQP)

The Executive provides the resources to implement the AQP.

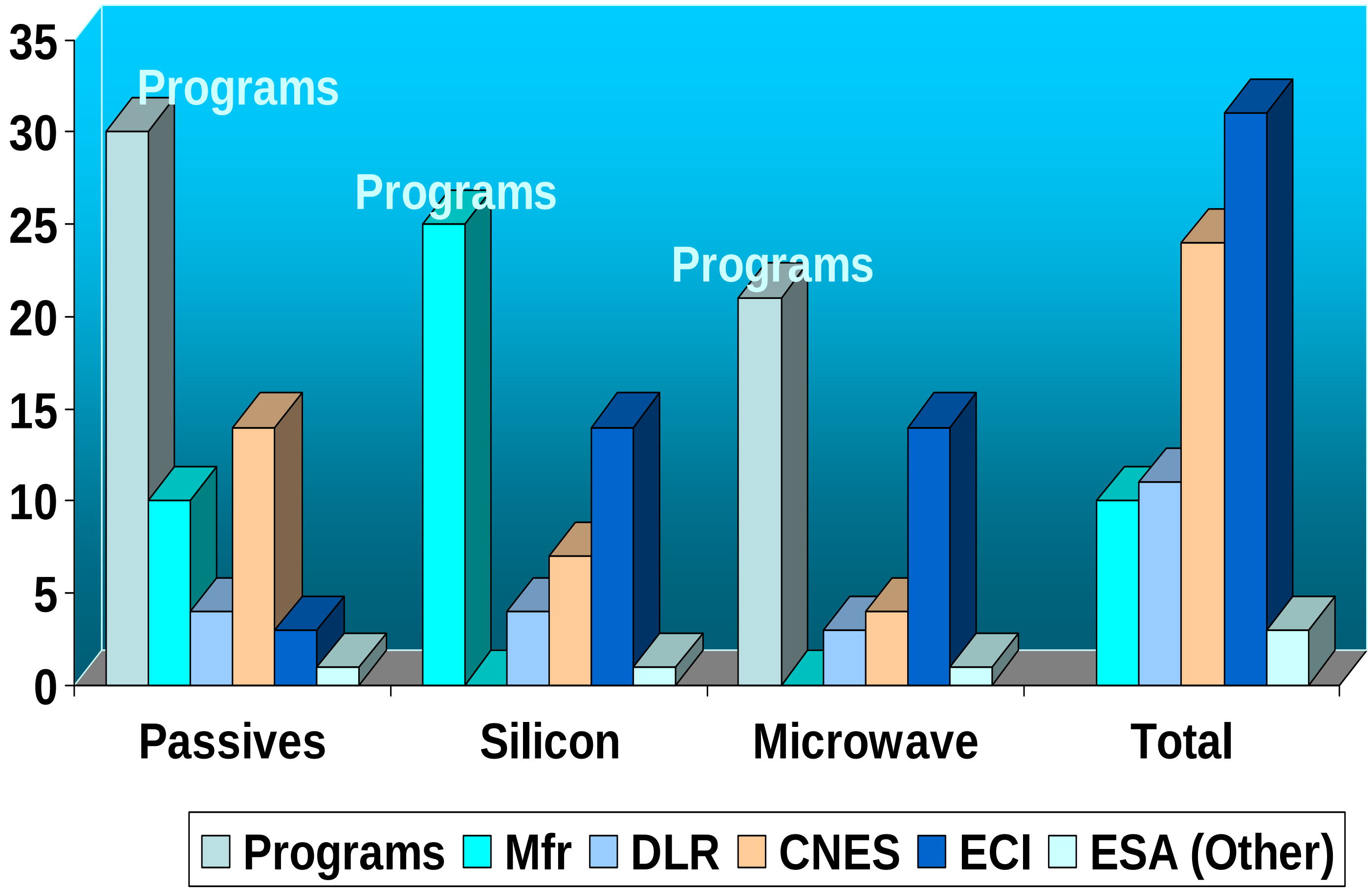
ESCC Evaluation and Qualification Programmes – Running Totals



ESCC Evaluation and Qualification Programme- 10 Year Trend Line



ESCC Evaluation and Qualification Programmes- Funding Profile



ESCC Qualification programme

– ESCC qualification is a general and long term authorisation for use in space.

– is based on a 2 step qualification approach:

Evaluation phase + Qualification Testing phase.

- is supervised by the ESCC Executive.

ESCC Evaluation Phase

Elements necessary at the beginning of / early in the Evaluation phase:

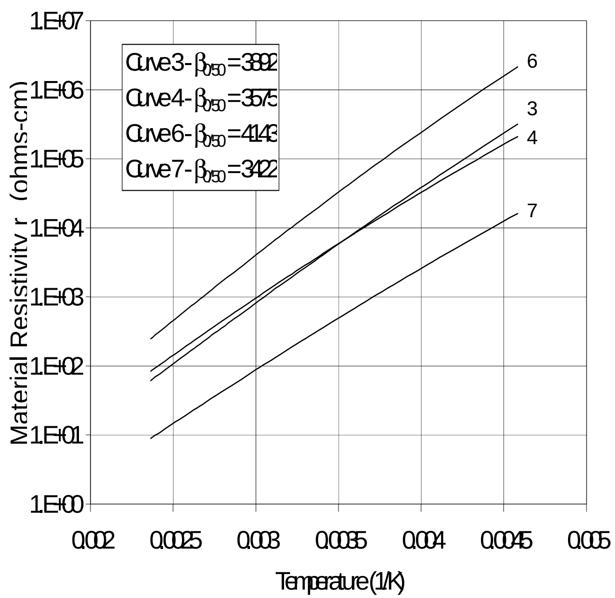
- Existing relevant test results and standard reliability data.
- Draft Detail Specification, if not already existing.
- Construction Analysis results.
- Draft Process Identification Document (PID).
- Domain and Test Vehicles description for Capability Approval/Technology Flow.

ESCC Evaluation Phase

Existing relevant characterization results, test results and standard reliability data:

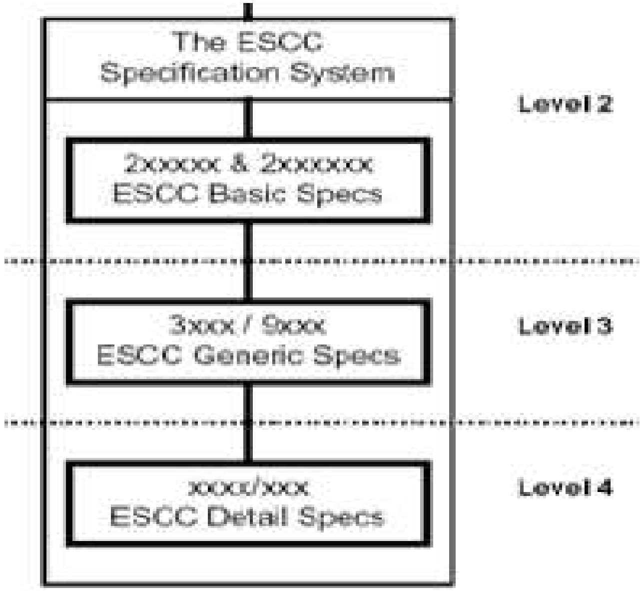
1 Very few EEE parts are specifically designed for space applications due to the low volume and sporadic purchasing/manufacturing requirements.

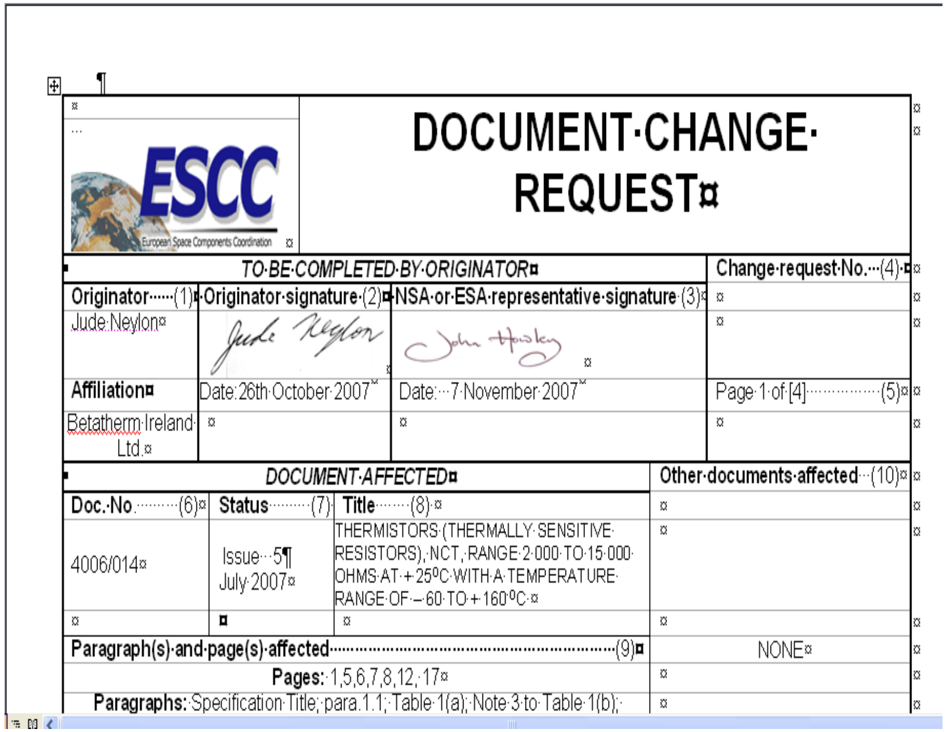
2 It is critical that all aspects of reliability and relevant known failure modes and mechanisms be addressed.



ESCC Evaluation Phase

Draft Detail Specification, if not already existing :





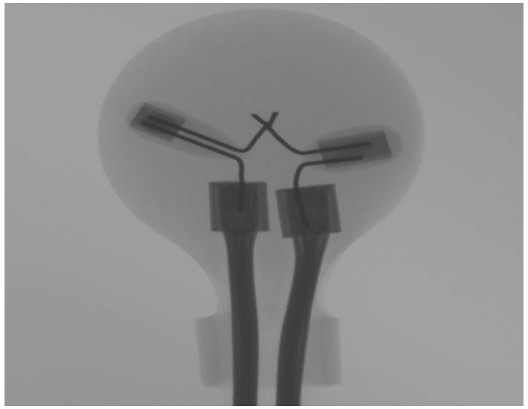
DOCUMENT CHANGE REQUEST

TO BE COMPLETED BY ORIGINATOR			Change request No. (4)
Originator (1)	Originator signature (2)	NSA or ESA representative signature (3)	
Jude Neylon			
Affiliation	Date: 26th October 2007	Date: 7 November 2007	Page 1 of [4] (5)
Betatherm Ireland Ltd.			

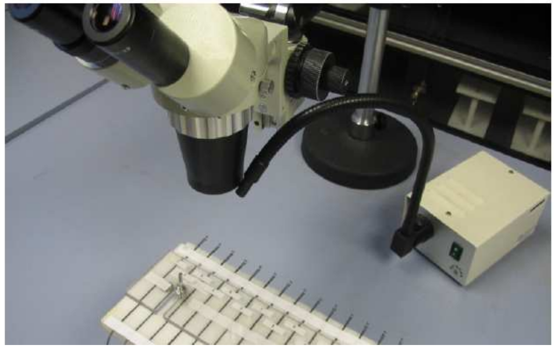
DOCUMENT AFFECTED			Other documents affected (10)
Doc. No (6)	Status (7)	Title (8)	
4006/014	Issue 5 July 2007	THERMISTORS (THERMALLY SENSITIVE RESISTORS), NCT, RANGE 2 000 TO 15 000 OHMS AT +25ºC WITH A TEMPERATURE RANGE OF –60 TO +160ºC	
Paragraph(s) and page(s) affected (9)			NONE
Pages: 1,5,6,7,8,12, 17			
Paragraphs: Specification Title; para 1.1; Table 1(a); Note 3 to Table 1(b);			

ESCC Evaluation Phase

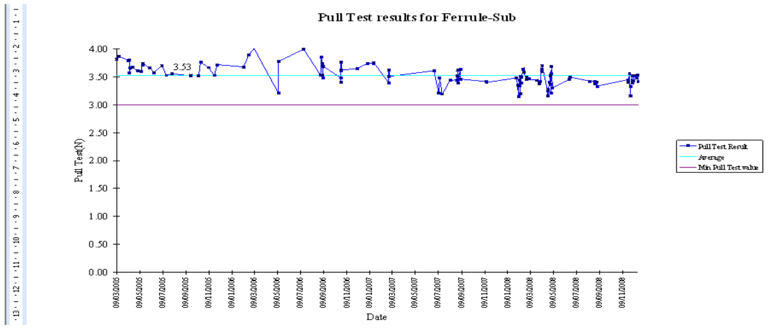
Construction Analysis results, for example:



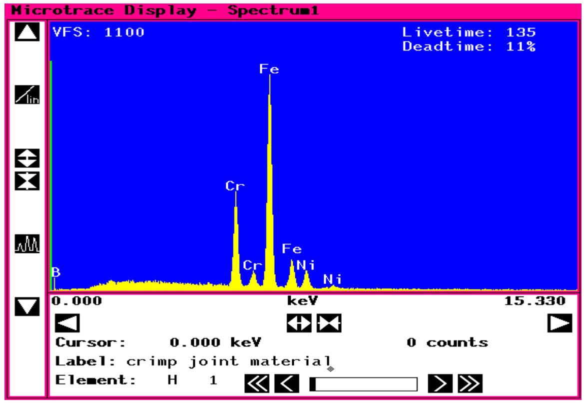
Radiography Analysis



Visual Analysis Results



Mechanical Analysis Results



SEM/EDX Element Analysis

ESCC Evaluation Phase

Draft Process Identification Document (PID)

The PID is an instantaneous and accurate picture of the actual manufacturing flow and practices.

The PID includes; amongst others:
- specimen of the travellers/route sheets used
- detailed flow chart with related manufacturing specifications
- list of piece parts and materials used
- a list of test equipment and test/inspection procedures
- a list of subcontractors and suppliers

ESCC Evaluation Phase

Domain and Test Vehicles description for Capability Approval / Technology Flow

The Capability Approval problem - Some components have design features that are tailored to a particular customer requirement, and may be required for a short time and often in small quantities.

Capability Approval solution – Define and evaluate a capability domain, and its boundaries, that will enable both the provision of standard devices and the ability to satisfy specialised needs.

Technology Flow (ESCC QML) issues – require to instil Quality Management (QM) within the manufacturing environment, using Statistical Process Control (SPC) and Process Technology Certification to accelerate the insertion cycle of high quality and reliable component types with emphasis on continuous improvement led by the manufacturer.

ESCC
European Space Components Coordination

ESCC Evaluation Phase

Component Selection

ESCC Executive will review existing data and verify that the proposed component is appropriate for evaluation.

If the results are promising, random samples, taken from current production, shall be subjected to a Construction Analysis (CA).

esa *Components Division Laboratory Support Group* *Report Number : CA0503 Page Number 1 of 22*

Components Division
Laboratory Support Group

ANALYSIS REPORT
NUMBER
CA 0503

After Construction Analysis, if the decision is to proceed, a Detail Specification will be required at this point.

ESCC
European Space Components Coordination

Pages 1 to 15

THERMISTORS (THERMALLY SENSITIVE RESISTORS), NTC,
RANGE 2000 TO 100000 OHMS AT +25°C WITH A
TEMPERATURE RANGE OF -60 TO +160°C

BASED ON TYPE G15K4D489, G10K4D453, G2K7D411, G4K7D421, G100K6D487,
G15K4D589

ESCC Detail Specification No. 4006/014

ESCC Evaluation Phase

Component Selection

- EVALUATION TEST PROGRAMME (ETP):

- Components and technologies are extensively characterized and tested; to destruction wherever possible!

- Tests are designed to:
  - Gauge reliability and lifetime
  - Provide stresses that simulate thermal, mechanical, electrical, vacuum and radiation environments
  - Address intrinsic and extrinsic failure modes
  - Determine the margins for these failure mechanisms (these are used in the ECSS-Q-ST-30 derating standard as well as for ESCC Detail Specification parameter derating).

ESCC European Space Components Coordination

ESCC Evaluation Phase

Component Selection

- EVALUATION TEST PROGRAMME (ETP):

• Established in conjunction with the Manufacturer / ESCC Executive
• On a sample representative of the component family – unscreened parts (no Burn-In)
• In order to determine failure modes and margins, it includes:
  - A review of existing reliability data
  - Endurance tests (HTRB, Extended Burn-in, Life Test)
  - Destructive tests (Step-stress, radiation, Environmental/Mechanical/Assembly…)

• Ancillary specifications ESCC 226xxxx describe the procedure and requirements to create and perform an ETP

ESCC Evaluation Phase

EVALUATION OF A MANUFACTURER

- A survey of the Manufacturer’s production, inspection and testing facilities is carried out under control of the ESCC Executive, particular attention being given to the existence and adequacy of formal updated documentation and control procedures relating to the component to be evaluated.

- this survey is performed as a formal audit in accordance with the requirements of ESCC Basic Specification No. 20200.

5 DEFINITIONS

In this report, the following definitions are employed:

FINDING - Objective evidence that a control feature of the quality programme or manufacturing process is not implemented in accordance with the requirements.

OBSERVATION - An observed control feature of the quality programme or manufacturing process, which is a cause for concern. A condition that may become a Finding.

COMMENT - A comment to an observed control feature of the quality programme or manufacturing process, which is neither a Finding nor Observation.

A Finding requires a corrective action and an Observation requires consideration by the manufacturer.

ESCC Evaluation Phase

EVALUATION OF A MANUFACTURER

Outputs of the Evaluation Phase are:

- Evaluation report
- Applicable Detail Specification(s)
- Final PID
- Final definition of the Domain (if applicable)
- A Generic Specification, if not existing
- Audit report + evidence of completed Corrective Actions

Resulting in:

Certification of the Evaluation by ESCC Executive

ESCC Qualification Phase

- Components required for qualification testing must be produced strictly in accordance with the PID.
- Qualification testing of the component must be in accordance with the requirements of the relevant ESCC Generic & Detail Specification.
- Successful completion of the testing phase results in listing on ESCC-QPL.
- A Qualification, once established, is valid up to 2 years.

ESCC Qualification Phase

Requirement for Qualification Approval

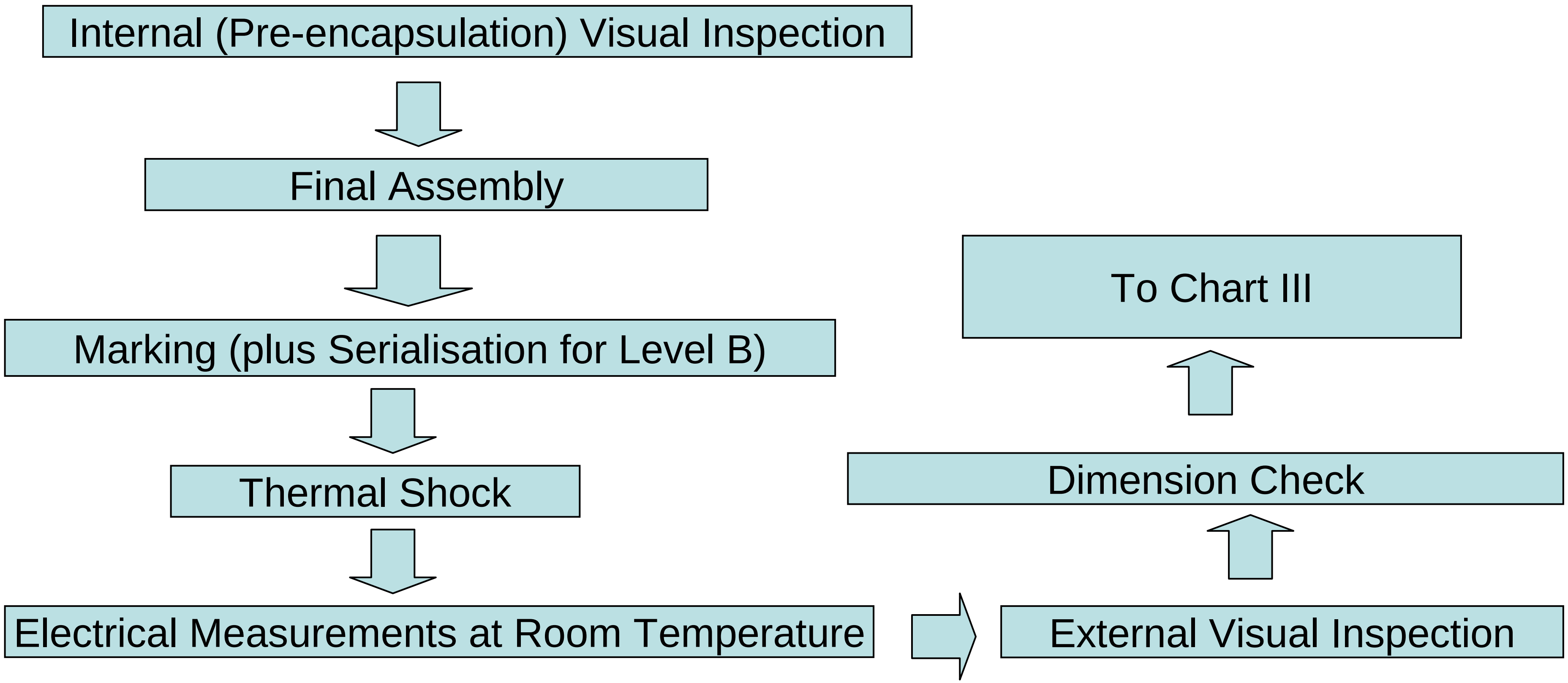
Chart II/F2:	Final Production Tests
Chart III/F3:	Burn-in & electrical measurements
Chart IV/F4:	Qualification tests

→ Test, Record and Report

ESCC Qualification Phase

ESCC Generic Specification No. 4006 - Thermistors

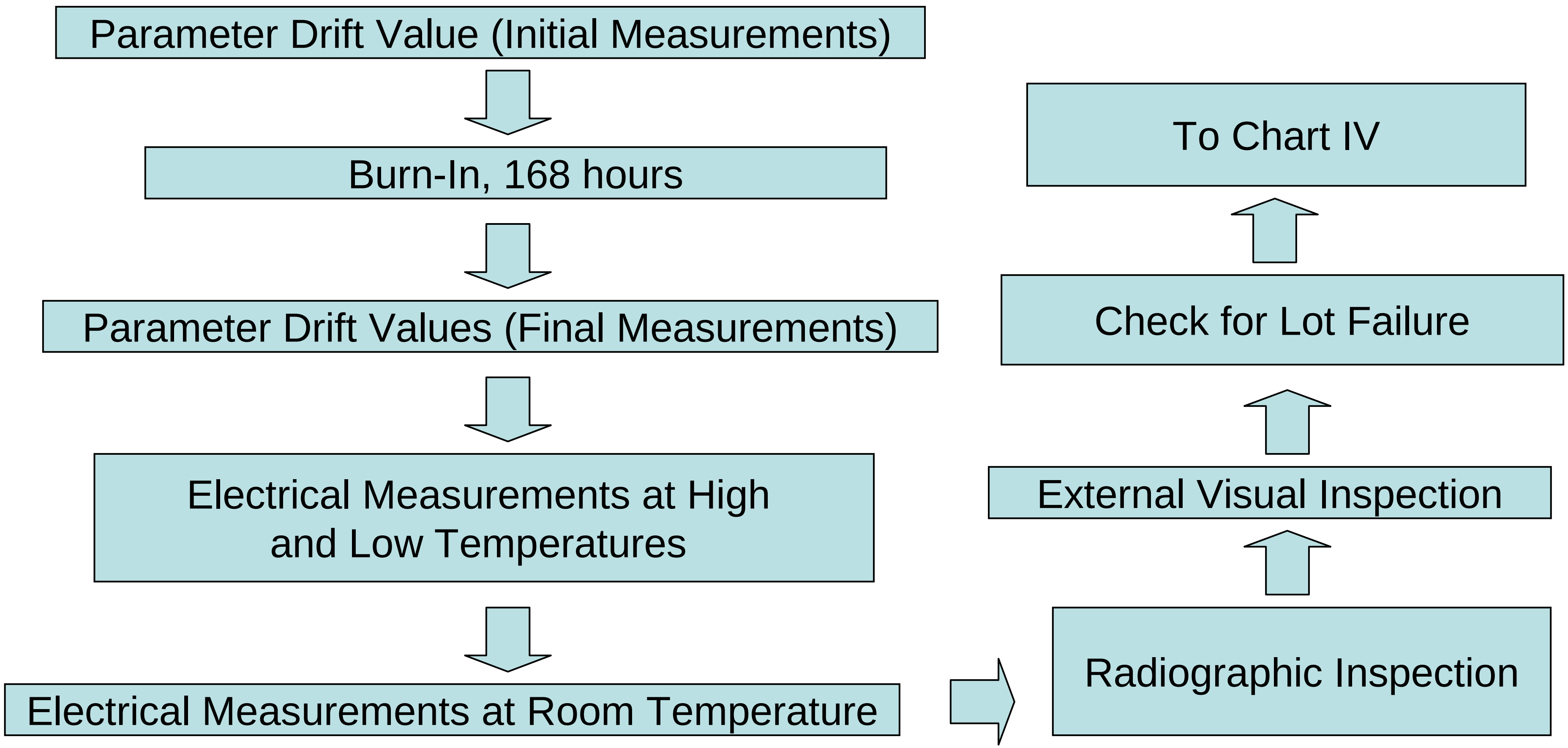
Chart II – Final Production Tests



ESCC Qualification Phase

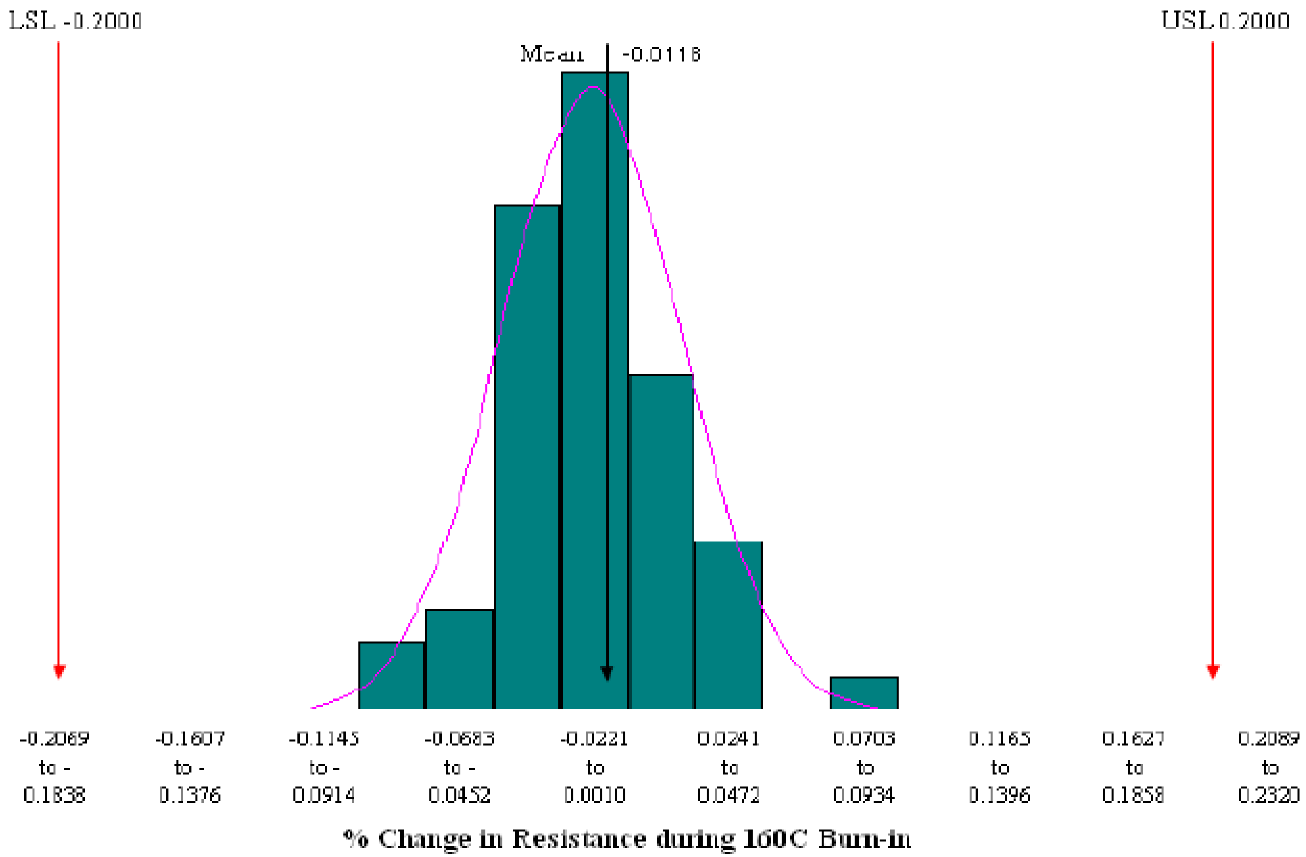
ESCC Generic Specification No. 4006 - Thermistors

Chart III – Burn-In and Electrical Measurements



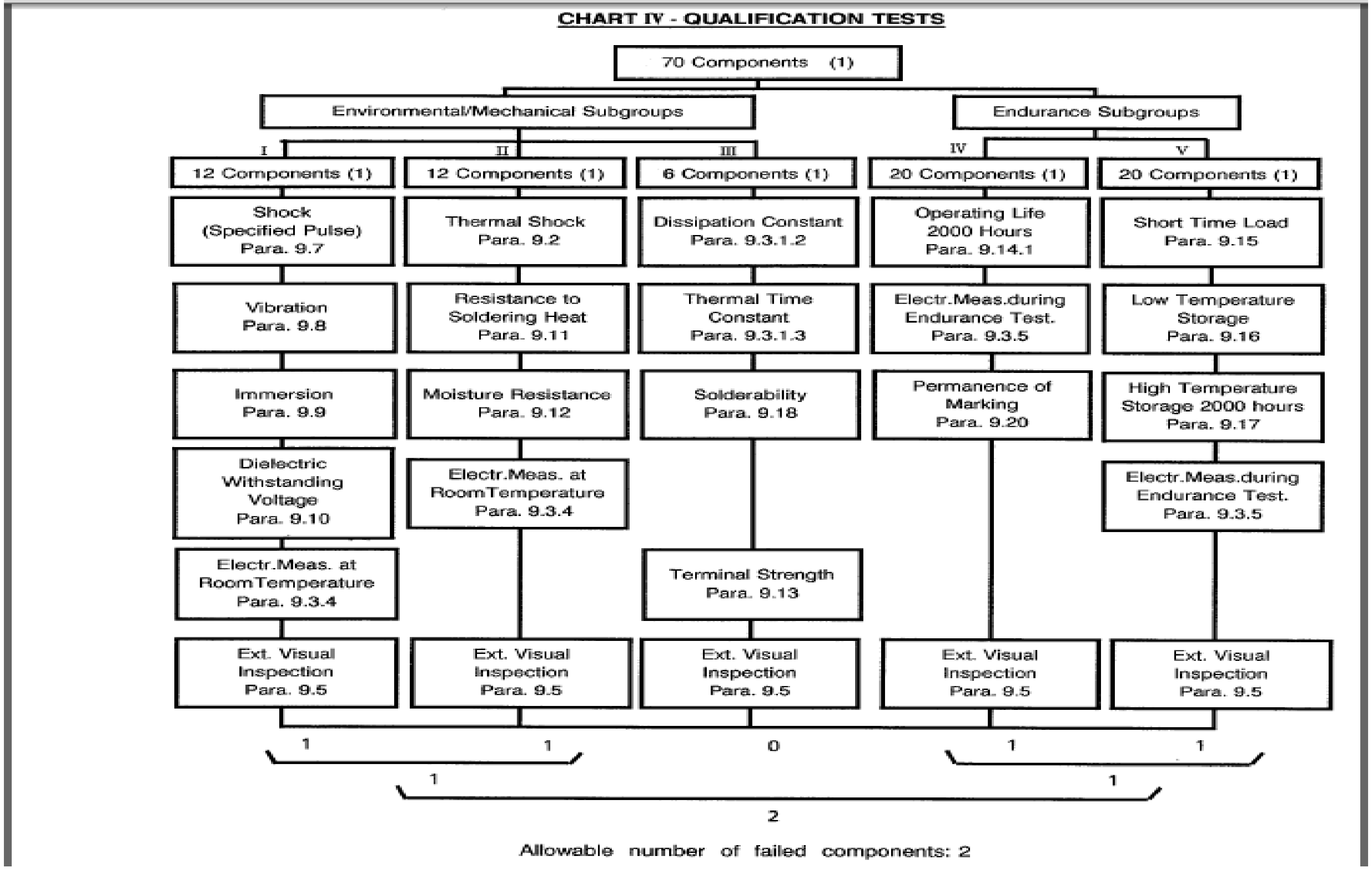
ESCC Qualification Phase

Parameter Drift Data - Results



ESCC
European Space Components Coordination

ESCC Qualification Phase



ESCC Qualification Phase

- Qualification testing of the component is documented and certified by the manufacturer.
- Non-conformances, failure analysis and DPA results when applicable are closed.
- A Qualification Report is accepted by the ESCC Executive.
- Components meeting the qualification requirements are certified by ESA.
- An ESA logo is applied by the manufacturer to each component meeting all the inspection and test requirements!

ESCC Qualification Phase

The expected result!!

Types covered by similarity:

Remarks: Refer to variants table 1(a) in the Detail Specifications for resistance to temperature characteristics

Procurement Specifications	Manufacturer
Generic ESCC 4006 Detail ESCC 4006/013 4006/014	MEAS Ireland (Betatherm) Galway Ireland

Characteristics:

4006/013: Variants 01 to 05 and 07 are qualified.

4006/014: Variants 08, 09, 12 and 13 are qualified.

Operating Temperature Range, (°C): $^{-}55$ to $^{+}115$ for 4006/013 variants 04, 05 and 06, $^{-}60$ to $^{+}160$ for 4006/014 variants 08, 09 and 13

Nature of Approval	Supervising Authority	Date
Qualification	ESTEC	Jul 2001
Extension	ESTEC	Jan 2002
Extension	ESTEC	Sep 2004
Extension	ESTEC	Nov 2006
Extension	Enterprise Ireland	Nov 2008
Extension	Enterprise Ireland	Nov 2009

THERMISTORS,
(THERMALLY SENSITIVE RESISTORS), NTC,
BASED ON TYPES G15K4D489 AND *K3A35*

Current Validity of Qualification		Page
Certificate	Valid Until	11-01
266 E	November 2011	001

Evaluation & Qualification Programs in Germany

Jürgen Tetzlaff (juergen.tetzlaff@dlr.de),
Guido Joormann (guido.joormann@dlr.de)

ESCCON, Noordwijk, 15. - 17. March 2011

Deutsches Zentrum
für Luft- und Raumfahrt e.V.
in der Helmholtz-Gemeinschaft

DLR EEE Parts Projects

Activity	Term	Status
PPH15-Process Evaluation	2003 - 2006	finished
Evaluation and Qualification of Thin Film Chip Resistors	2004 - 2008	finished
Evaluation and Qualification of Cables	2005 - 2009	finished
Qualification of Quartzes and Oscillators	2005 - 2010	in progress
Qualification of Microwave Connectors	2005 - 2011	in progress
Certification of an Assembly and Test House	2006 - 2011	in progress
Qualification of MMIC Local Oscillator	2007 - 2011	in progress
Development and Qualification of PowerMOSFETs	2008 - 2011	in progress
Qualification of Diodes and RF-Transistors	2008 - 2011	in progress
Evaluation of the UMS PPH15x Process	2008 - 2011	in progress
Development of a GaN 1000V Switching Transistor	2007 - 2011	in progress
Capability Approval of L-Foundry	2010 - 2013	In progress
Qualification of RF-Circulators / Isolators	2011 - 2013	planned
Capability Approval of IHP‘s SG13 Technology	2011 - 2013	planned
Qualification of a fully automatic LTCC Line	2011 - 2013	planned
Feasibility Study of the SiC Diodes Technology	2011 - NN	planned

All projects under : www.dlr.de/qp/en/desktopdefault.aspx/tabid-3091/4699_read-6881/

Evaluation and Qualification of RF-Connectors

This project shall improve the components availability for the European space users in the area of high frequency connectors. The request for qualified RF-connectors arose from the German manufacturers for space equipment, since connectors are required in lot of space equipment.

Info : www.rosenberger.de/

Qualification of Diodes and RF-Transistors

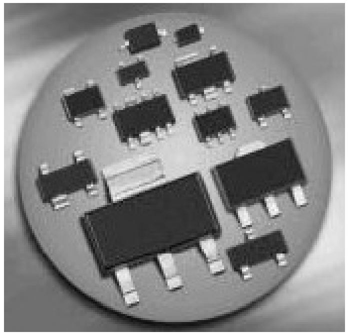
For automotive und wireless applications, Infineon provides high-quality diodes and microwave transistor chips. On request of German users they shall be packaged in suitable housings and an ESCC qualification of these parts is in progress.

Diodes: BAY6642 (1N6642)

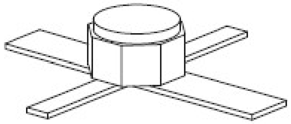
RF-Transistors: BFY640, BFY640B, BFY650B, BFY740B.

Info : www.infineon.com/cms/en/

=> discretes



Diodes

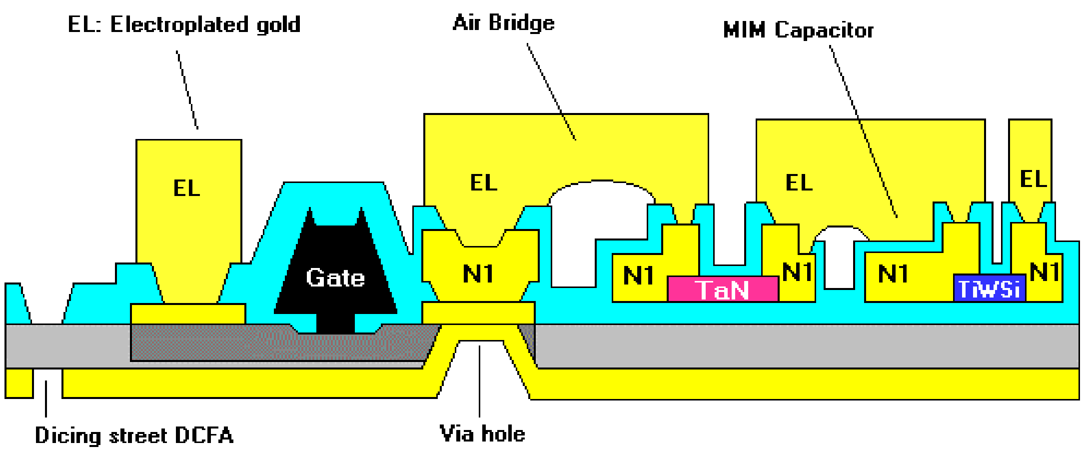


RF-Transistor, Micro-X Package

Evaluation of the UMS PPH15x Process

In this program, a delta evaluation of the PPH15x MMIC process will be performed. PPH15x stands for Power PHEMT (Pseudomorphic High Electron Mobility Transistor), a GaAs based technology with 0,15 Micron gate length, the x for a power enhancement of the PPH15 process, which was already evaluated. Life time and reliability tests have been performed. Space evaluation has started.

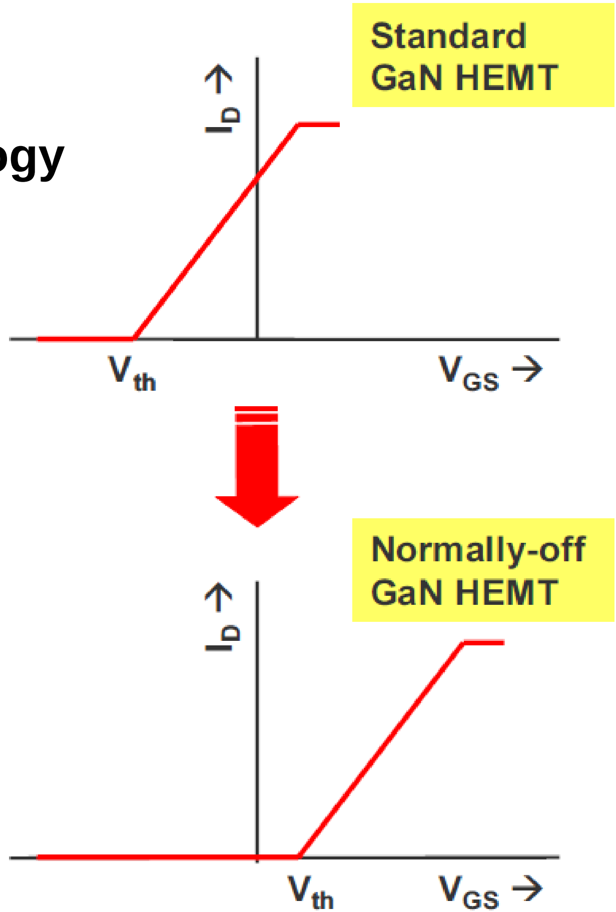
Info : www.ums-gaas.com/



Development of a GaN 1000V Switching Transistor (1)

Targets

- **Normally-off GaN transistor technology for space borne power conditioning**
- **Requirements**
  - low on-state resistance
  - high breakdown voltage (up to 1000 V)
  - Threshold voltage Vth > + 1 V
  - Large gate swing > 3 V
  - Low leakage currents
  - Reproducible process
  - Radiation hardness
  - High Reliability



Development of a GaN 1000V Switching Transistor (2)

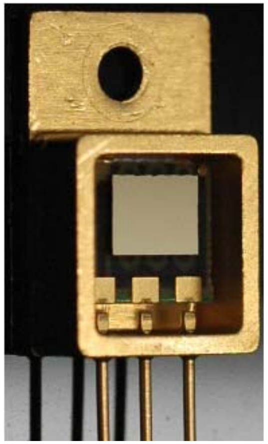
Actual Results

- Stable 3” GaN process
- Positive threshold voltage (+ 1.2 V)
- Large gate voltage swing (5 V)
- High IDS-max (0.5 A/mm) ➔ good trade-off to normally-on devices)
- Low leakage:
  - off-state drain leakage 10 µA/mm @ VGS = 0 V
  - on-state gate leakage 10 µA/mm @ VGS = + 5 V

- Good saturation properties
- Transistor-channel conductive if operated in reverse direction
  - 3rd quadrant operation
  - May be used for “self protection” when switching inductive loads

- Safe transistor operation up to 200°C ambient
  - IDS decreases with T _ CT = -1.3 mA/(mm K)
  - RON increases with T _ CT = 43 mWmm/K
  - Vth constant with T _ CT = -0.24 mV/K

➔ **No thermal run-away situation in p-GaN gate power transistors**

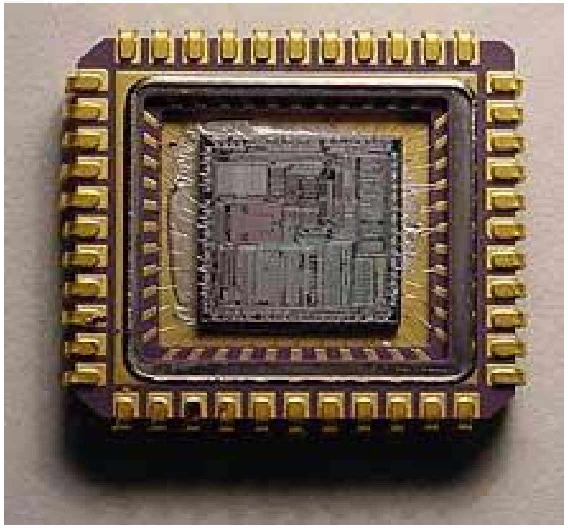


50 A device flip-chip mounted in TO 220 package

Capability Approval of L-Foundry

For space applications, less and less semiconductor foundries are available. Recently, the widely used MG2RTP CMOS process from Atmel became obsolete, too.

In preliminary investigations, L-Foundry (Landshut) was determined as suitable foundry. Meanwhile L-Foundry has bought Atmel's foundry at Rousset (F), too.



In a first test step, the suitability of commercial library elements for a radhard design will be verified.

In case of a positive result, an ESCC capability approval will be carried out.

Info : www.lfoundry.com/

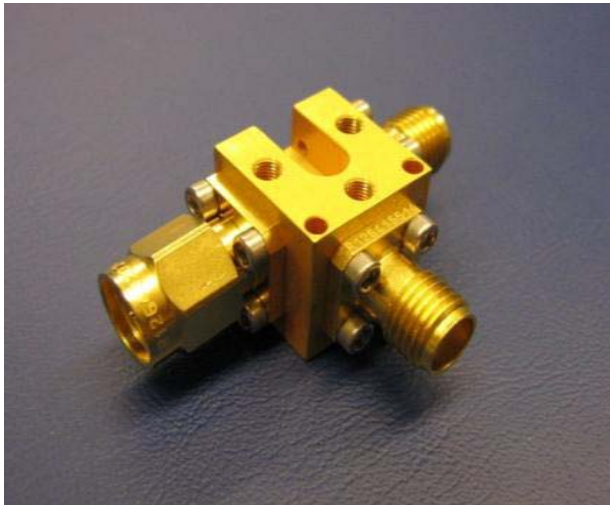
Qualification of RF-Circulators / Isolators

There are only two not qualified suppliers in Europe (Chelton [F] and Trak [GB]), who can deliver RF-Circulators / Isolators with required properties :

- High Reliability
- Low Insertion Loss
- High Isolation.

On the other side a German supplier fabricates excellent RF-Circulators / Isolators for their own use.

Therefore, German users asked for the ESCC qualification.

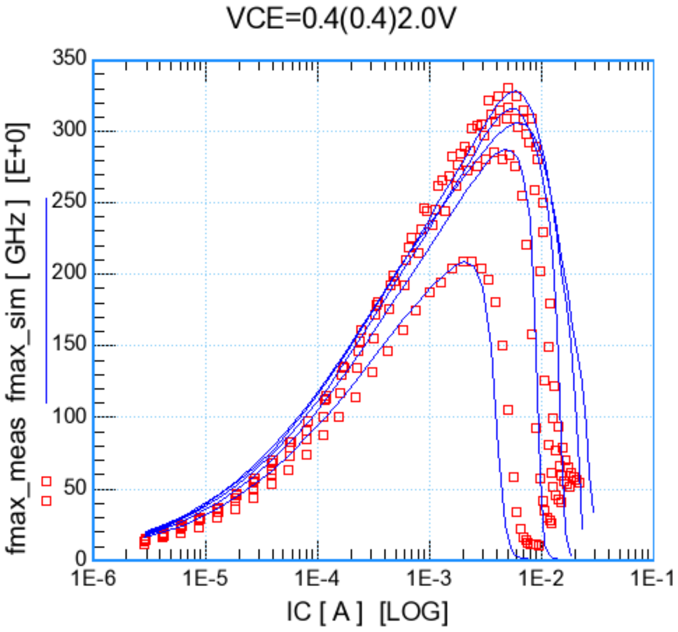


Capability Approval of a SG13 BiCMOS Technology

The SG13 BiCMOS technology is a mixed signal 0.13 µm technology with the focus on high frequencies (up to 140 GHz) and low power CMOS transistors.

In a first step several suitability tests will be performed, prior to developing a radhard library and test circuits for this technology.

Thus a further process for space use will be established in addition to an existing 0.25 µm technology, which is applicable for frequencies to 20 GHz and is already in the ESCC capability approval.



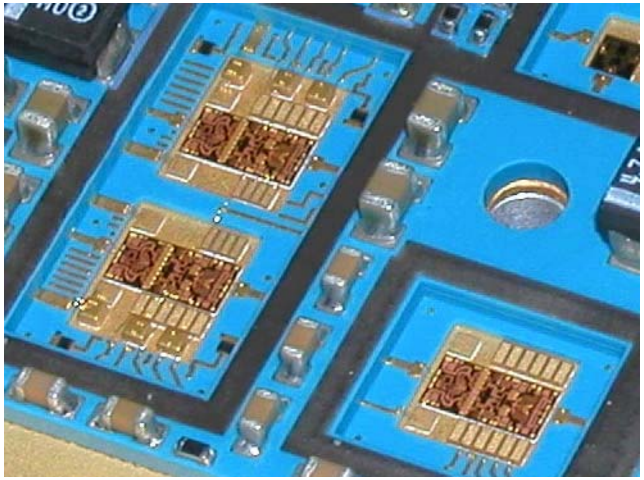
SiGe HBT f_{Max} versus $I_{collector}$ measured and modeled

Qualification of a fully automatic LTCC Line

A German supplier operates a fully automatic LTCC (Low Temperature Cofired Ceramics) line, which was used up to now for commercial applications.

This line shall be extended for space modules manufacturing and an ESCC capability approval shall be performed. By the extremely high degree of automation of this line, a very small error rate (First-pass yield > 95 %) will be achieved.

Due to the high process reliability of the line, a cost-effective fabrication of small and lightweight MMICs (e.g. up- and down converters or channel amplifiers) will be possible.



Feasibility Study of the SiC Diodes Technology (1)

Why Silicon carbide ?

- Space applications need robust and heat resistant components.
- Silicon power semi conductors are more and more reaching their physical limits (higher junction temperature, higher loss), which can lead to the damage of the parts.
- SiC offers excellent material properties and allows components with outstanding electrical characteristics and high junction temperatures.

➔ **A feasibility study shall examine the use for Space application.**

Feasibility Study of the SiC Diodes Technology (2)

Comparison Si ↔SiC

Characteristics	Si	SiC
Band Gap (eV)	1.1	3.2
Electron Mobility (cm^2/Vs)	1400	900
Disruptive Field Strength (kV/cm)	250	> 2000
Thermal Conductivity (W/cmK)	1,5	4.9
Advantages	Less Defects Higher Yield Lower Price	High Temperature Strength High Ampacity Chemical Resistance Radiation Hardness Material Hardness
Drawbacks	High Switching Loss at High Temperature At Performance Limit	High Increase of Crystal Defects Processes difficult to control Costly Bulk Material

Thank you for your attention!

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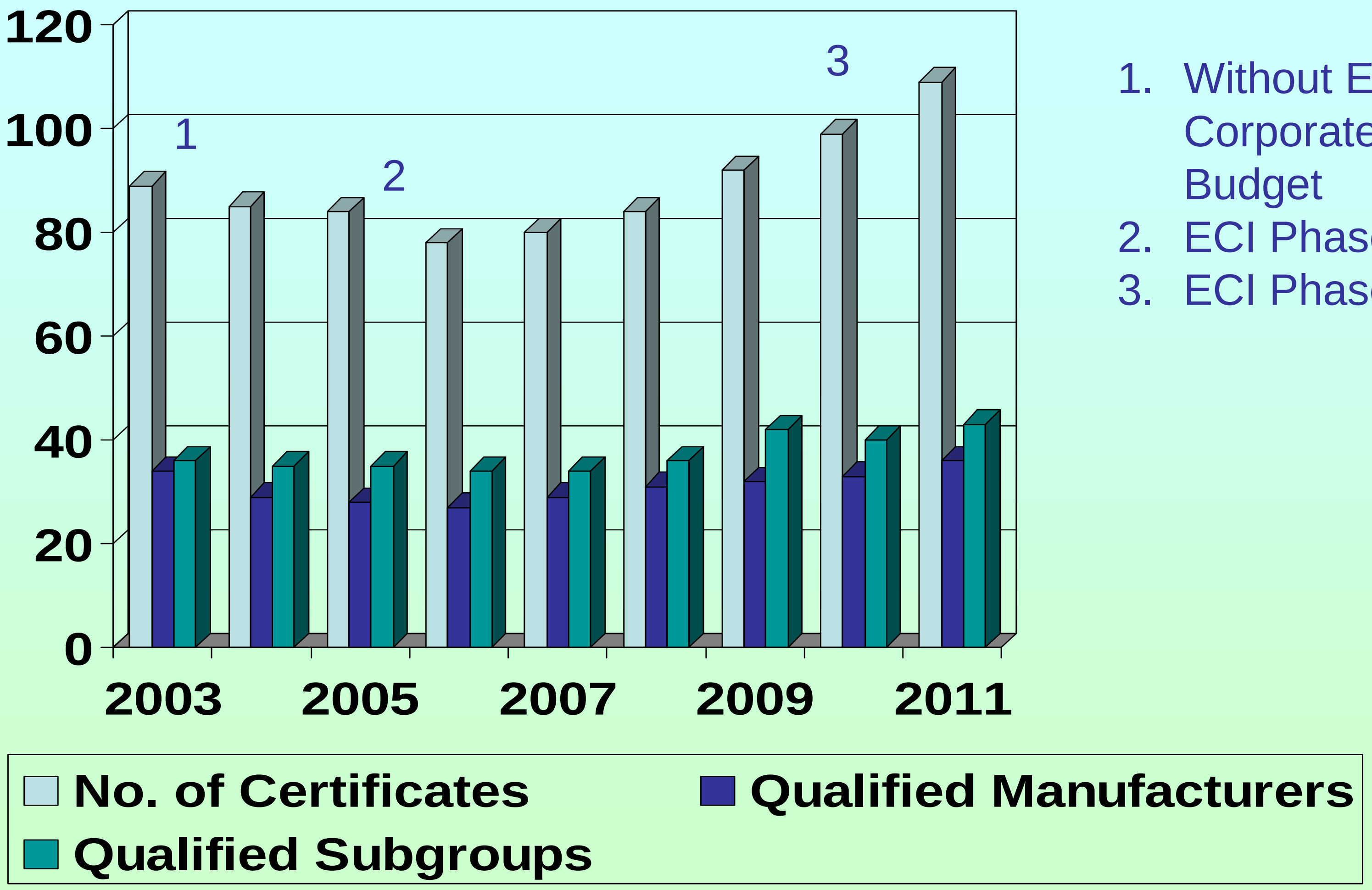
ESCC Evaluation and Qualification Programmes: Certificates



1. Without ESA Corporate Budget
2. ECI Phase 1
3. ECI Phase 2

ESCC Evaluation and Qualification Programmes: Benefits

The ESCC products constitute a pillar of product assurance through standardization of EEE components in space programs.

By applying standardization and type reduction space programs benefit in a number of ways:

- Components used in designs are applied properly with margin supported by available test data
- Components are evaluated or qualified to established criteria prior to use
- Quality and reliability of each component is established
- Components are compatible with equipment manufacturing processes
- Evolution of component quality and significant parameters are under configuration control
- Provides for component obsolescence management
- Component data is collected and stored for retrieval and analysis.

ESCC Evaluation and Qualification Programmes: Benefits

Key Results:

ECI stimulus funding from CNES, DLR and ESA has reinitiated AQP investment

AQP Programs managed by the ESCC Executive since 2005 up by 50%

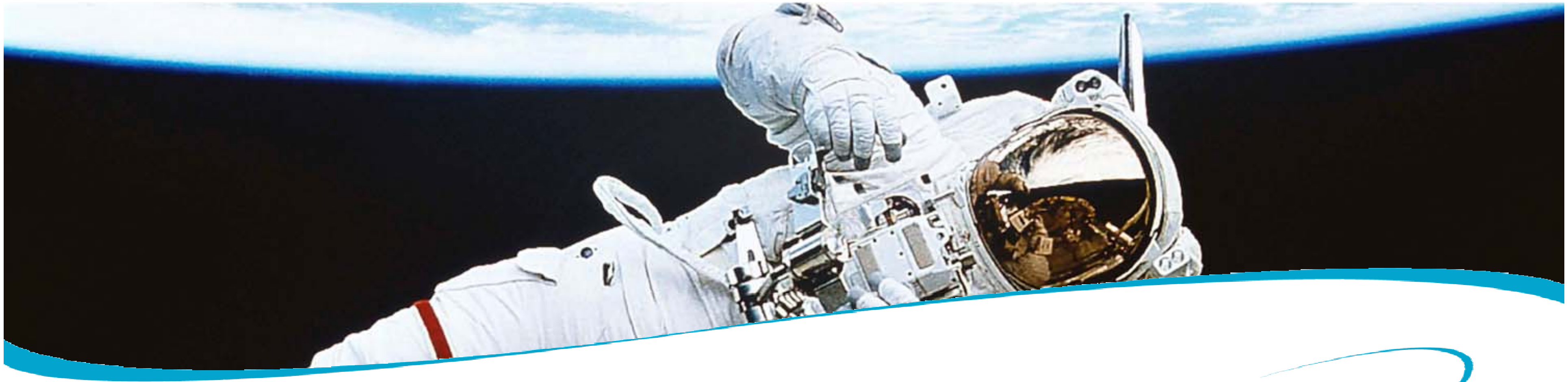
Number of ESCC qualification certificates since the low of 2006 up by 40%

12.7 % of AQP Programs are self funding

European space component manufacturers 2010 turnover > 240 M€

1200 employees of European manufacturers dedicated to space components


ESCCON 2011
Thank You for Your Attention
J. Howley, Enterprise Ireland
G. Joormann, DLR Köln
J. Wong, ESA ESTEC



Optoelectronics: risk management of problems encountered

A. Bensoussan

Thales Alenia Space, France

e-mail : alain.bensoussan@thalesaleniaspace.com

ESCCON 2011, NOORDWIJK, NETHERLANDS

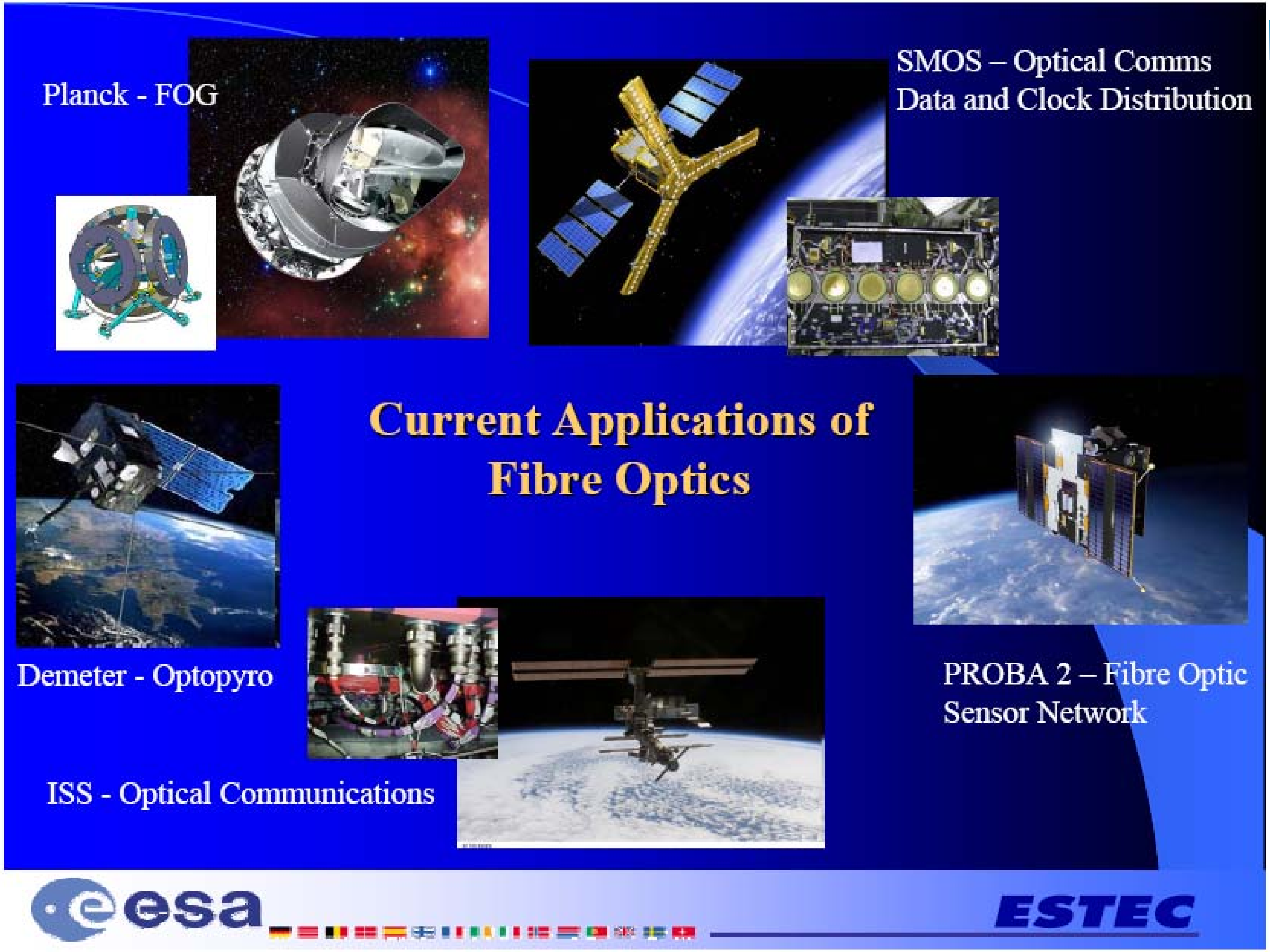
March 15th-17th 2011

CCEL

Content

- **Optical Links in Space Application**
- **Industrialization and Quality concerns vs Risk management**
- **Optoelectronic vs Reliability**
- **Conclusion**

Optical Links in Space Application

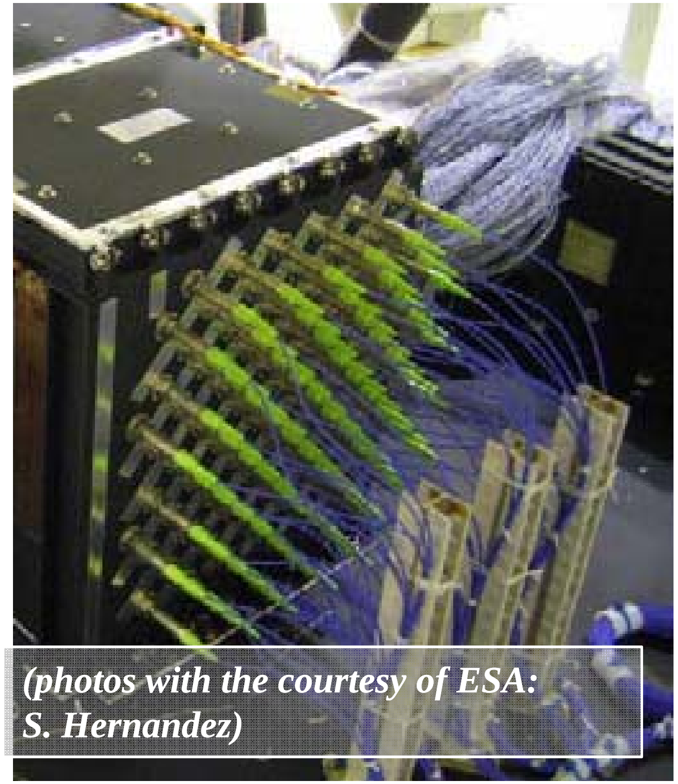


(courtesy of ESA : Iain Mckenzie and Nikos Karafolas)

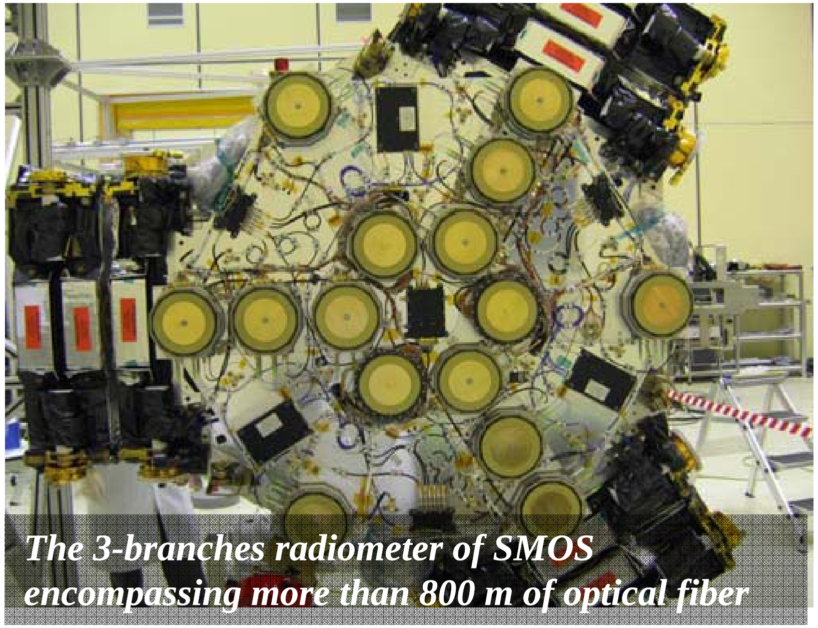
Optical Links in Space Application

• COTS Fibre Optic Components in SMOS/MOHA (ESA)

ESA's Soil Moisture and Ocean Salinity (SMOS) earth observation satellite using fibre optics.



(photos with the courtesy of ESA: S. Hernandez)

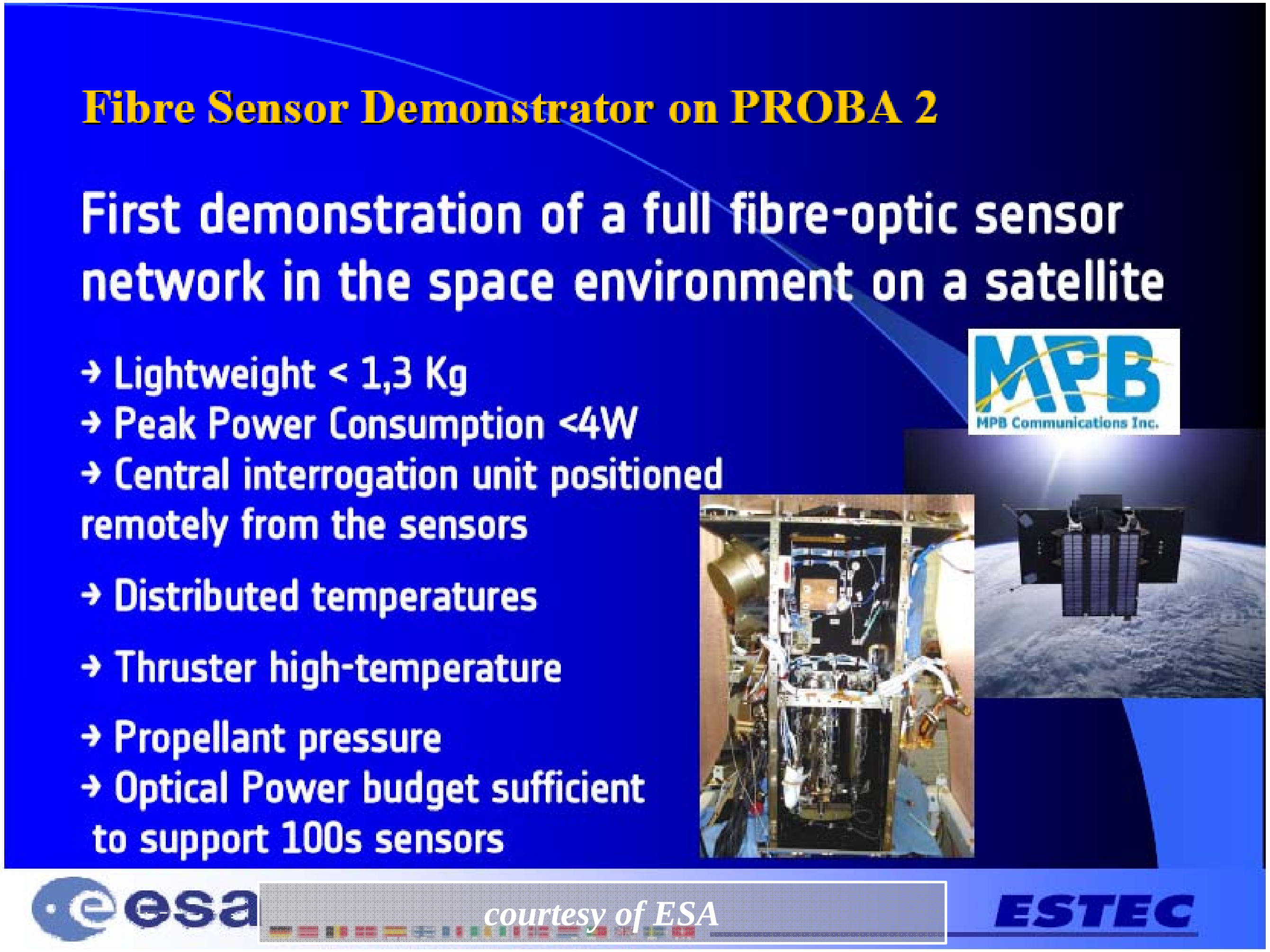


The 3-branches radiometer of SMOS encompassing more than 800 m of optical fiber

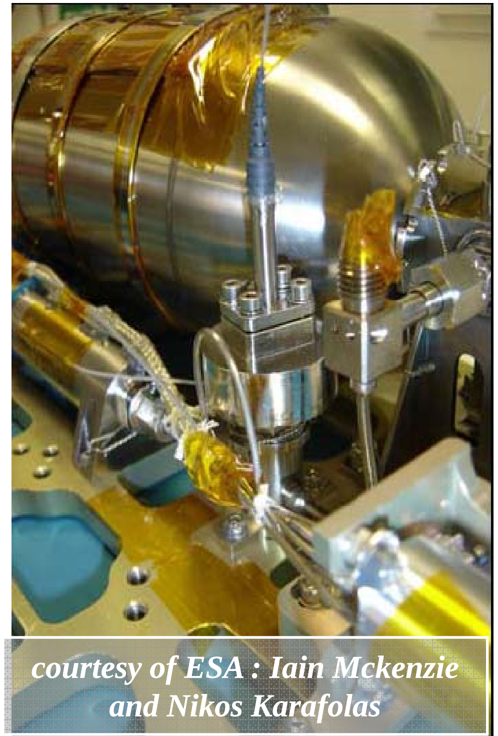
The optical fibre is used to communicate with the 72 detectors spread over the three arms of the satellite, conveying an optical clock to the detectors and returning a digital optical data signal to the digital correlator.

Optical Links in Space Application

- **Fiber-Optic Sensor System Demonstrator for Proba-2 (ESA)**



courtesy of ESA

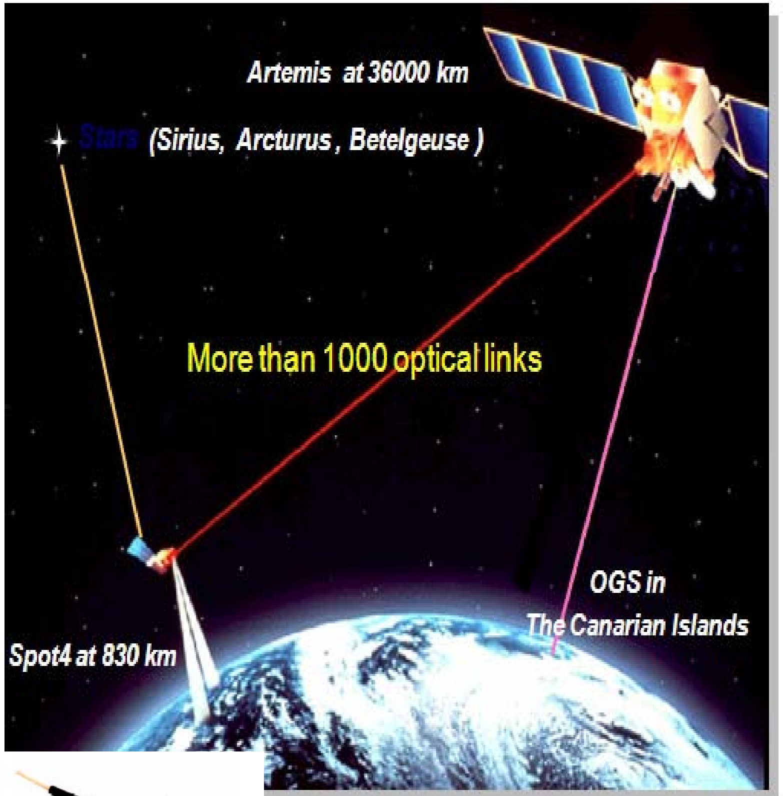

courtesy of ESA : Iain Mckenzie and Nikos Karafolas

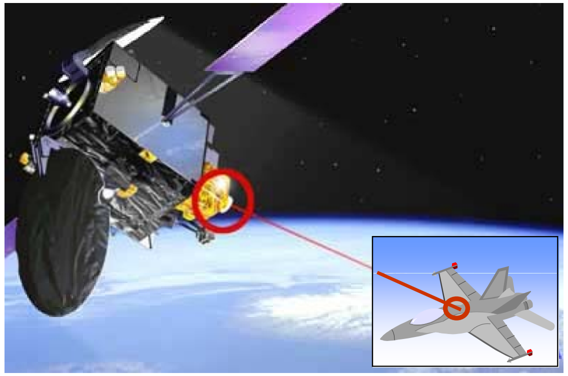
Attachment of FOS in the tank and pipes of the Propulsion Subsystem of ESA's PROBA II satellite.

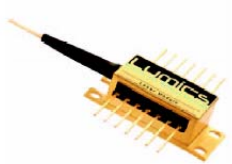
Optical Links in Space Application

- **High Bandwidth 0,85 µm laser Free Space Communication on ARTEMIS SILEX (EADS) and LOLA application (EADS, TAS)**

View SILEX Free Space Communications (courtesy EADS Astrium)





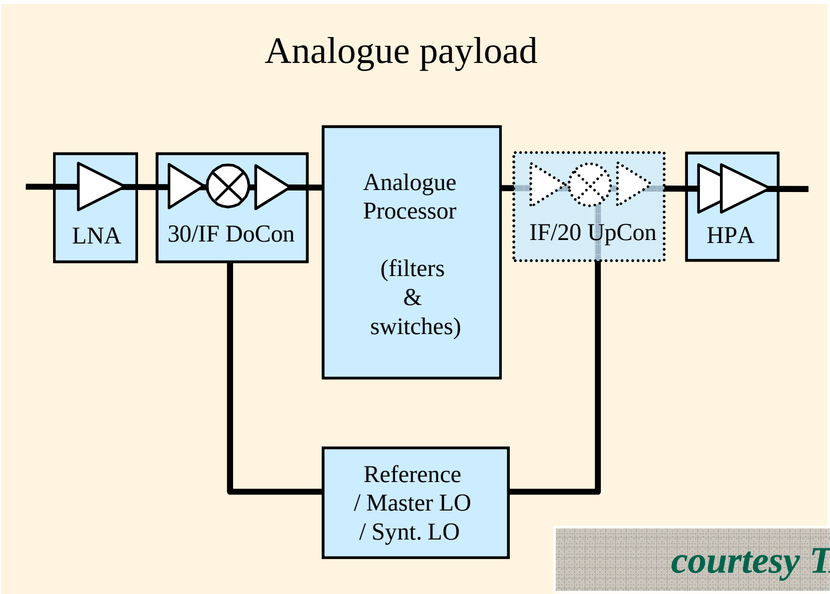


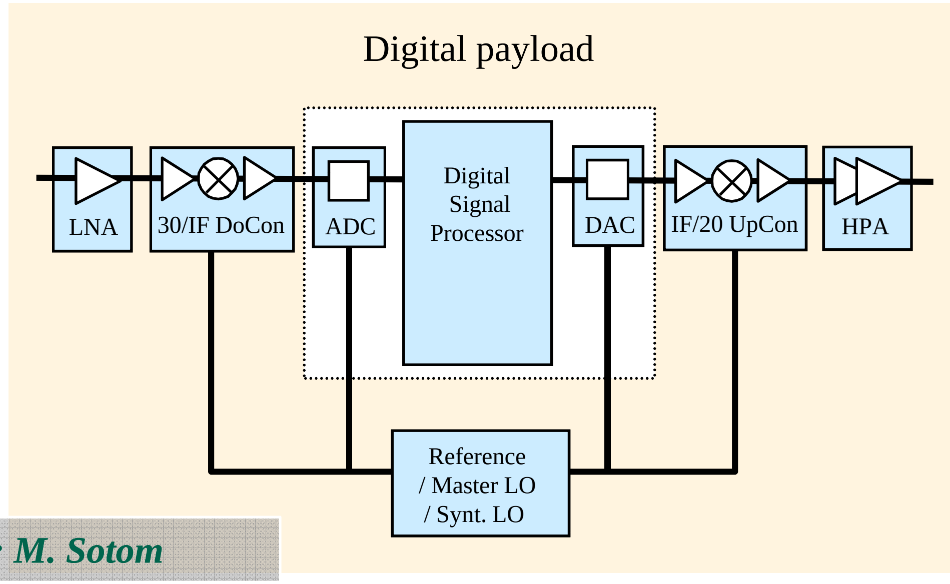
LOLA demonstrator laser diode : Operating conditions: 320 mW p-p, OOK, 50 Mbps

Advanced Photonic for Flexible Telecom payloads

Telecom satellite & payloads - Future Broadband Solutions (TAS)

- flexible complex payloads : coverage, connectivity, frequency plan, bandwidth allocation …
- > 100 RF channels (10’s of MHz) over 10’s of antenna beams
- critical requirements in terms of mass, volume & power consumption
- future-proof solutions = transparent payloads (analogue or digital)





courtesy TAS : M. Sotom

THALES

Advanced Photonic for Flexible Telecom payloads

• Microwave photonic repeater sub-systems (TAS)

Microwave photonic repeater concept

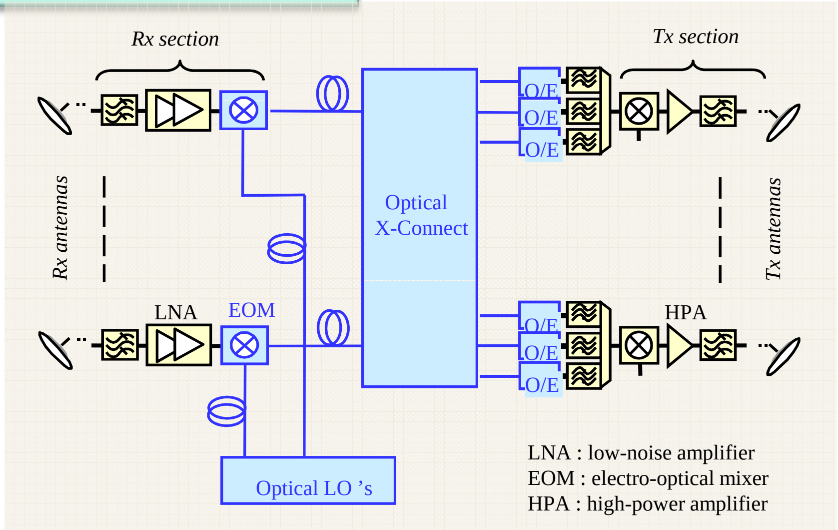
- optical generation & distribution of LO's
- optical frequency-mixing
- optical cross-connection of µ-wave signals

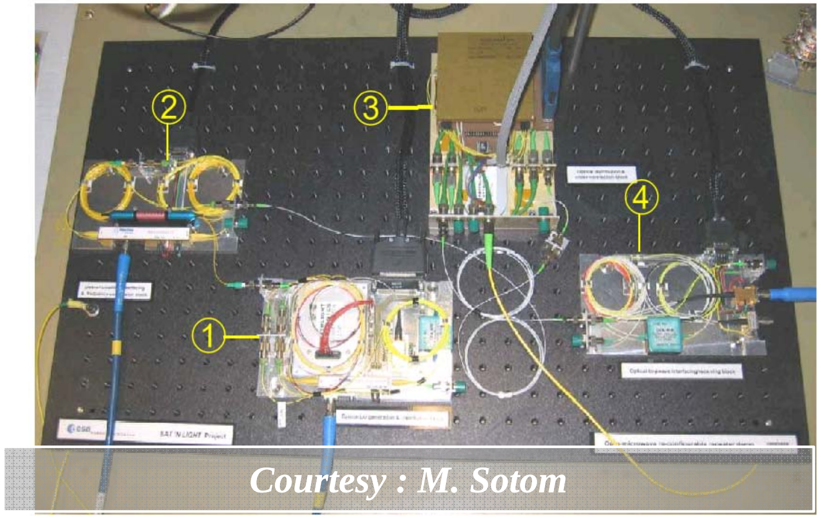
Applications : flexible analogue repeater

- Frequency-independent (C/Ku/Ka), broadband design : cost and planning advantages
- Flexible connectivity : in-orbit reconfiguration

Major achievements

- ESA *SAT 'N LIGHT* study, repeater concept & architectures
- BB demo
  - Ka-band LO distribution
  - Optical Ka/C down-conversion
  - RF channel cross-connection (by MOEMS)
- Validation of concept & performance



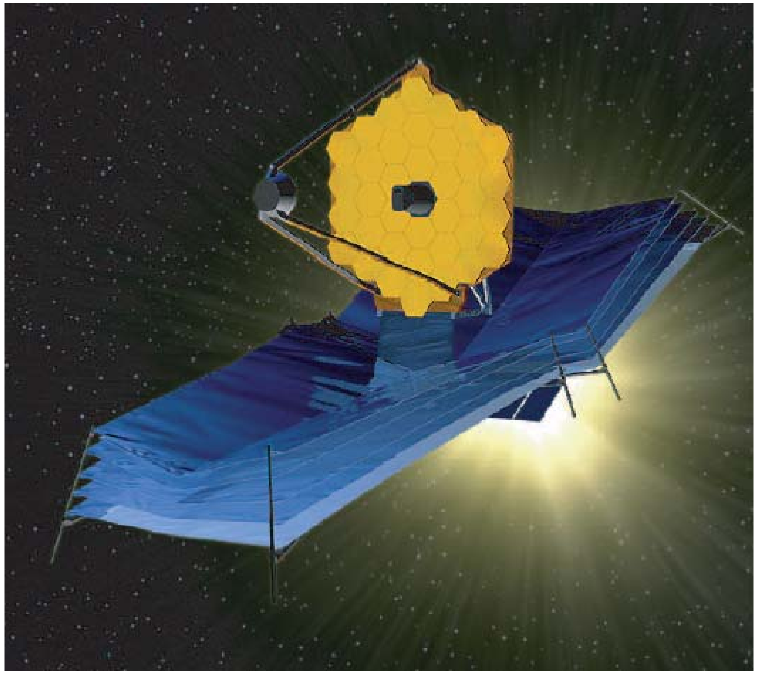


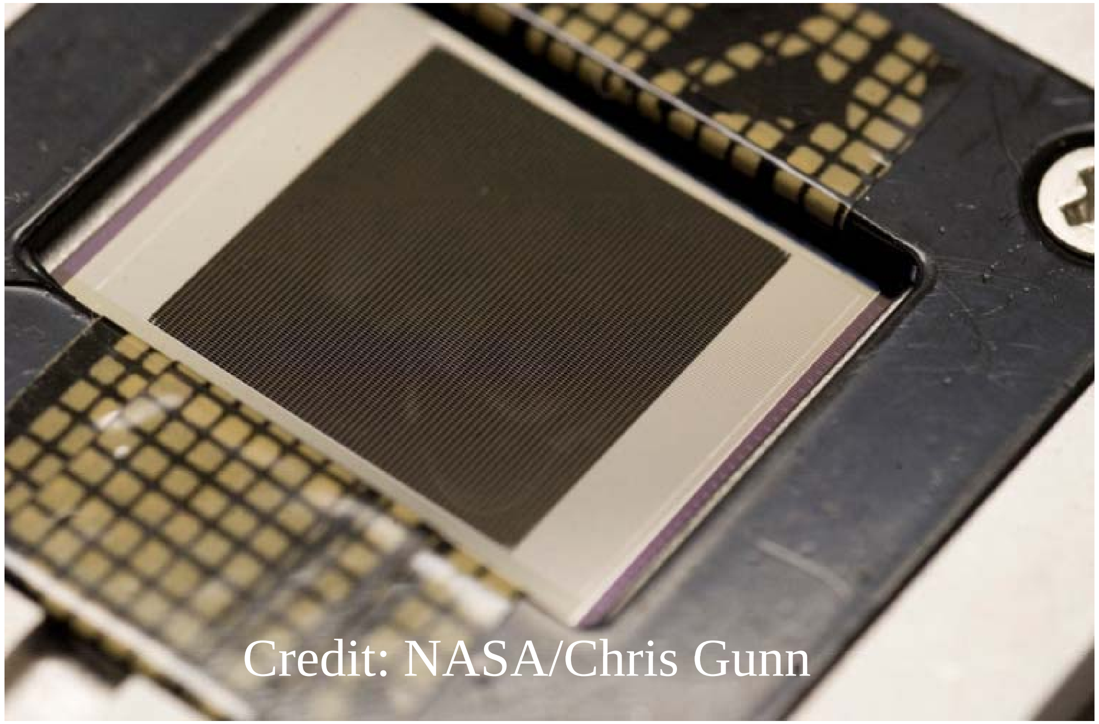
THALES

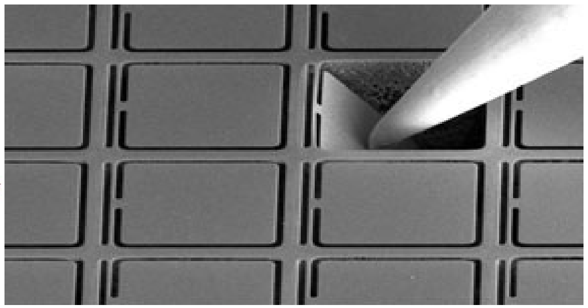
Optical Links in Space Application

In USA

- **JWST (NASA) and Smart technologies and MOEMS for Extremely Large Telescope (ELT) instruments (NASA).**







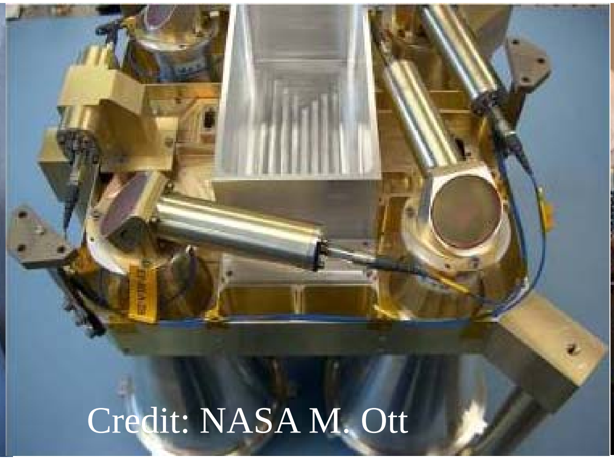
Micro-shutters manufactured by NASA/GSFC

http://www.nasa.gov/topics/technology/features/micro shutters.html

Optical Links in Space Application

NASA Lunar Reconnaissance Orbiter (NASA GSFC)

Series of missions towards the exploration of the Moon and Mars for the purpose of providing remote human habitat bases for planetary study



The Mercury Laser Altimeter consisted of four telescopes with fiber coupled from each to four individual detectors

Lunar Orbiter Laser Altimeter (LOLA) and Laser Ranging

Photos from paper M. Ott : Fiber free Space Optics.

LR Operations Overview

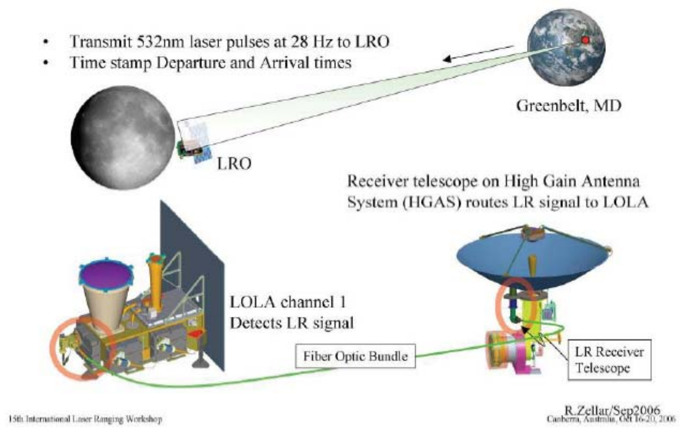
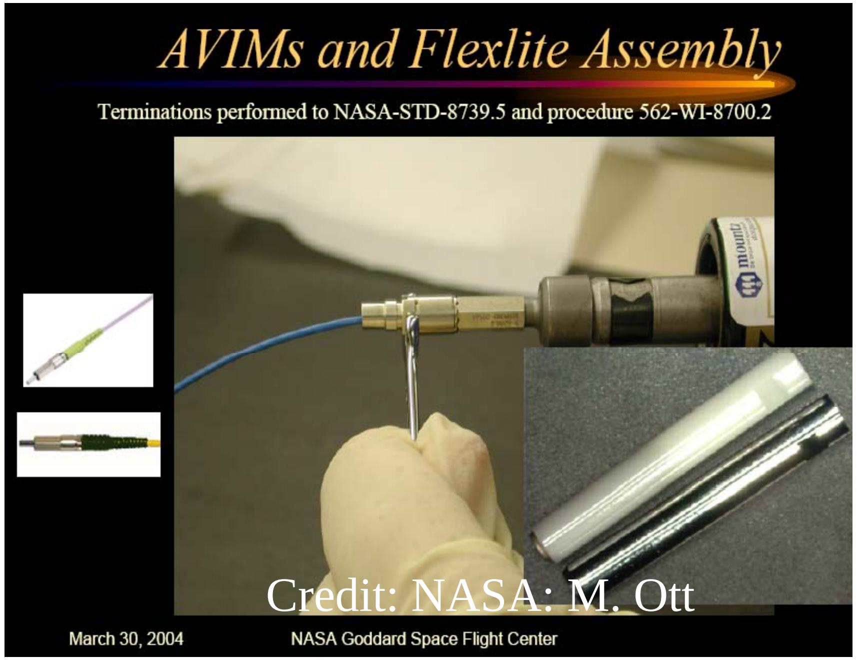


Fig. 7. LRO Laser Ranging Configuration Concept [11]

DIAMOND AVIM Connectors for Space Environments (NASA and ESA)

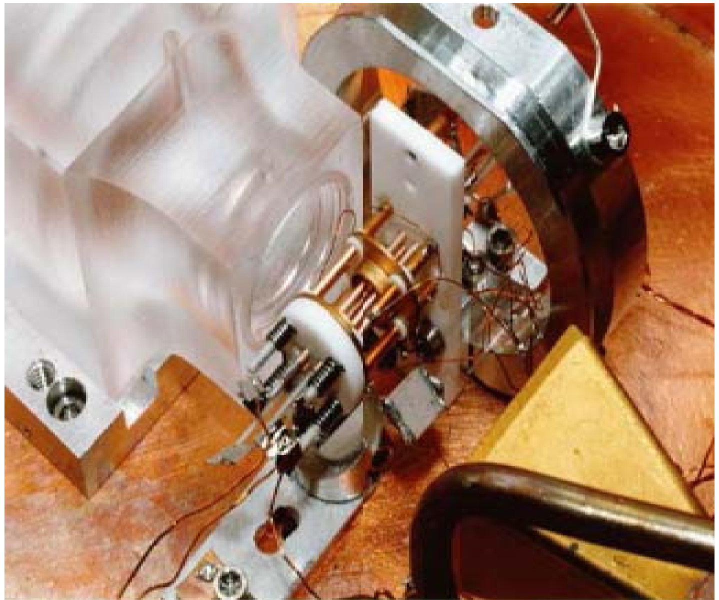


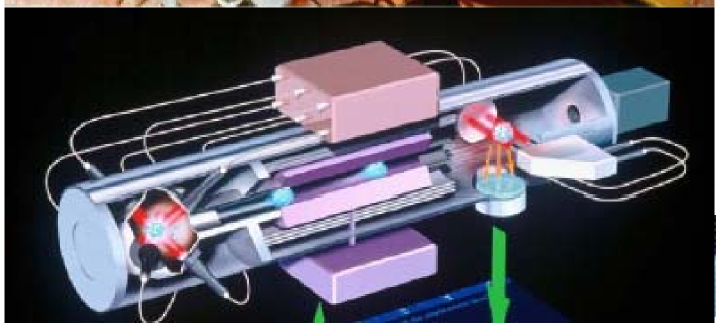
Mini-AVIM

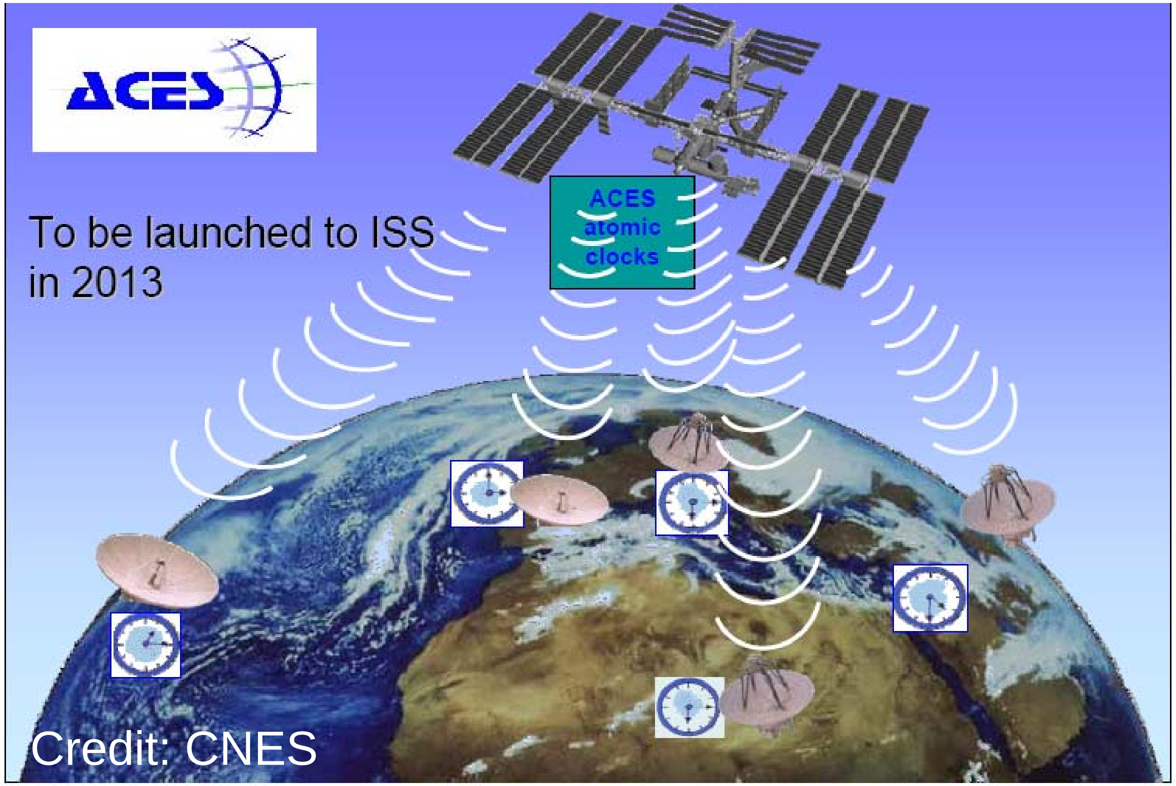
Miniature fiber optic connector for Space,
MIL and harsh environment application

- Basic Specification ESCC 2263010, ETP for Simplex Optical Fibre Connector Sets released in 2006.
- Part of an ongoing ECI Phase 2 activity with Diamond (Switzerland), following specification will be proposed to the PSWG in 2011:
  - Revision and updating of the **ESCC Basic Specification 2263010**
  - **Generic Specification** (ESCC qualification): Simplex fibre optical connector.
  - **Detail Specification**: Simplex optical fibre connector based on type AVIM.
  - **Detail Specification**: Simplex optical fibre connector based on type mini-AVIM.
- In the frame of 2 parallel ongoing GSTP activities T&G (Norway) and Fibre Pulse (Ireland), the ECSS-Q-TM-70-51 Technical Memorandum on the fibre cable assembly will be updated (2011-2012).

Qualification of a Caesium optical atomic clock in Pharao (EADS SODERN/CNES)

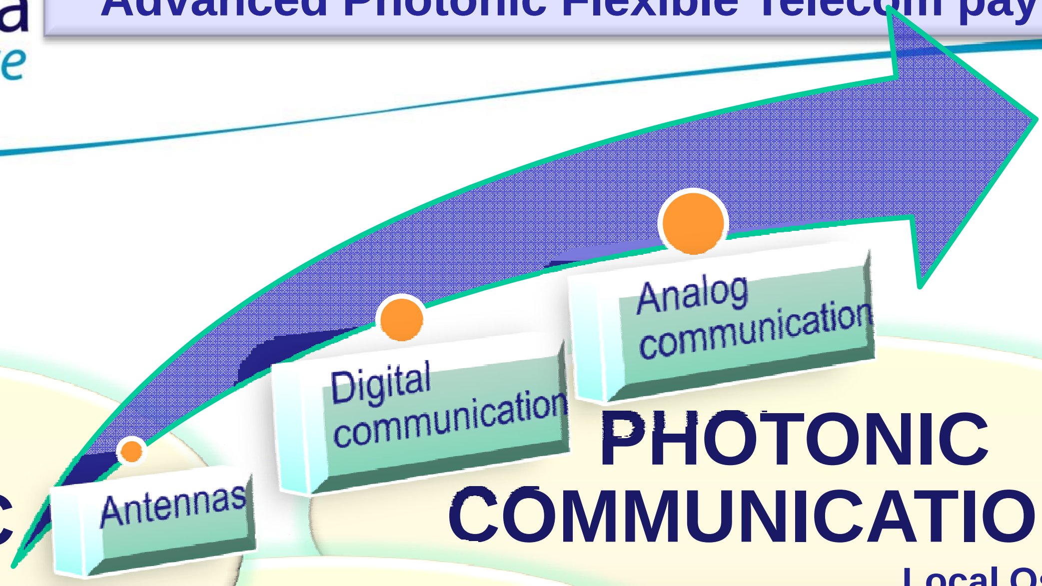






- A cold atom Cesium clock in space
- Fundamental physics tests
- Worldwide access

The key optical areas in Telecom application payloads : Advanced Photonic Flexible Telecom payloads



PHOTONIC SENSING

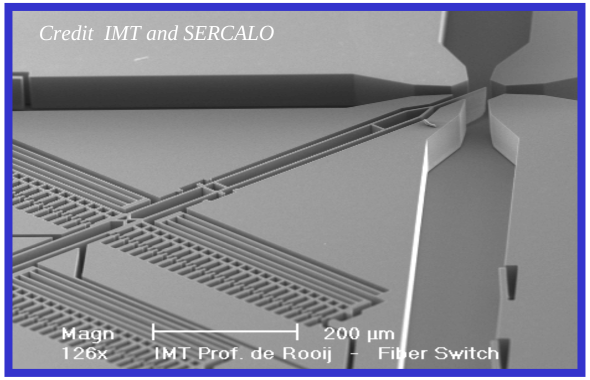
Structural Panels and Equipment
Antenna Reflectors
Direct Radiating antenna
Chemical propulsion
Electric propulsion
Fiber Optic Gyroscopes

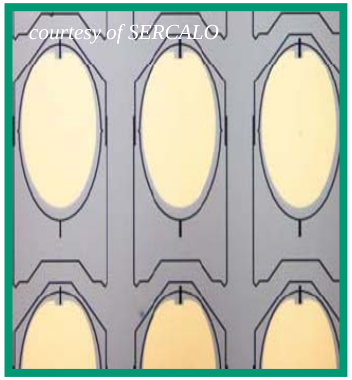
PHOTONIC SIGNAL PROCESSING

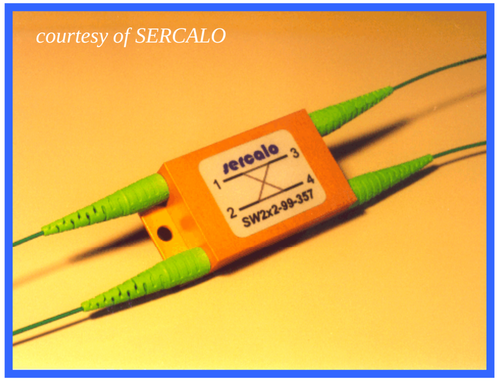
Equipment to equipment interconnects
Inter or intra-board interconnects
Inter or intra-chip interconnects
ADC to DSP and DSP to DAC interconnects
Electro-photonic fast sampling
Ultra-fast switching (ns switching time) for packet/burst switching

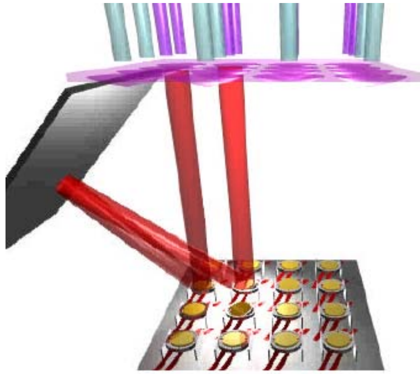
PHOTONIC COMMUNICATIONS

Local Oscillator Generation
Down Conversion
Switching
Analog to Digital Conversion
Beam Forming
Novel Photonic payload architecture concept
Opto-microwave transparent analog repeater

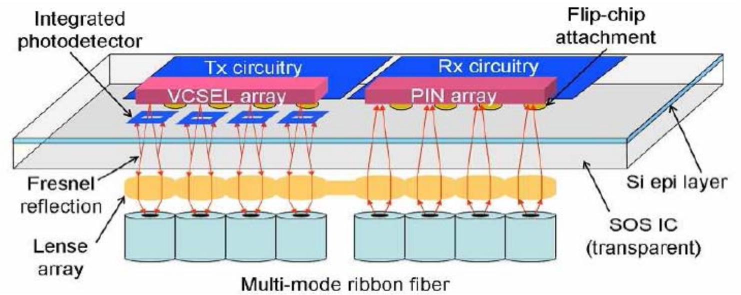


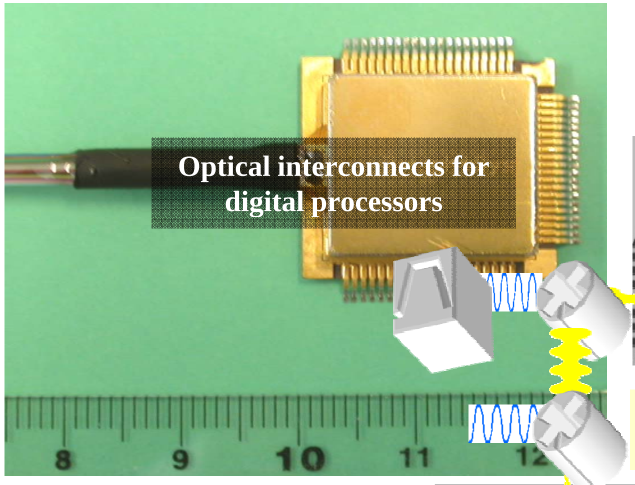


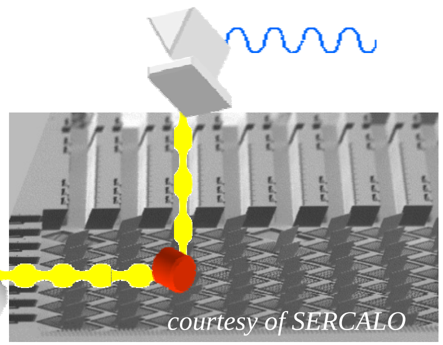




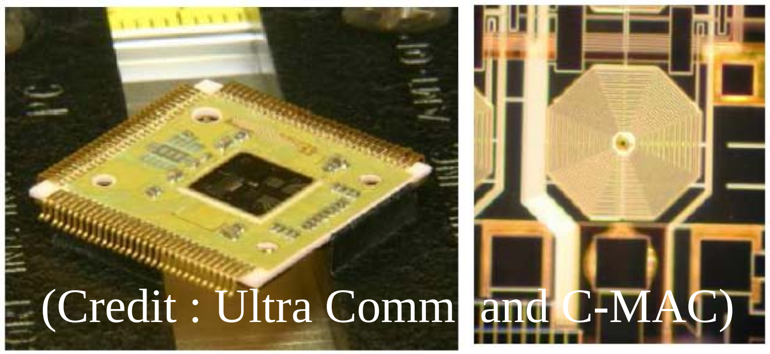
courtesy of LUCENT Technology





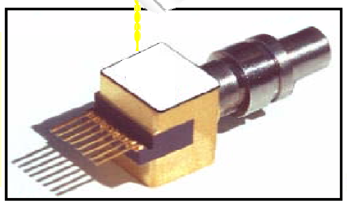


Opto-Microwave Repeater concept
MOEMS switching matrix



(Credit : Ultra Comm and C-MAC)

Flip-chip assembly with the flip-chip VCSEL/PIN .



ROSA photo-receiver

Who is going to use Optoelectronic system architectures as innovative solutions and for what specific and strategic reasons ?

How to be ready to adopt new technologies ?

- In High tech, products are often more costly and complicated
- Therefore market adoption of a technology product is dependent upon helping customers reduce perceived risk.
- In the risky world of high tech, the customer will not rely only on the word of the provider.

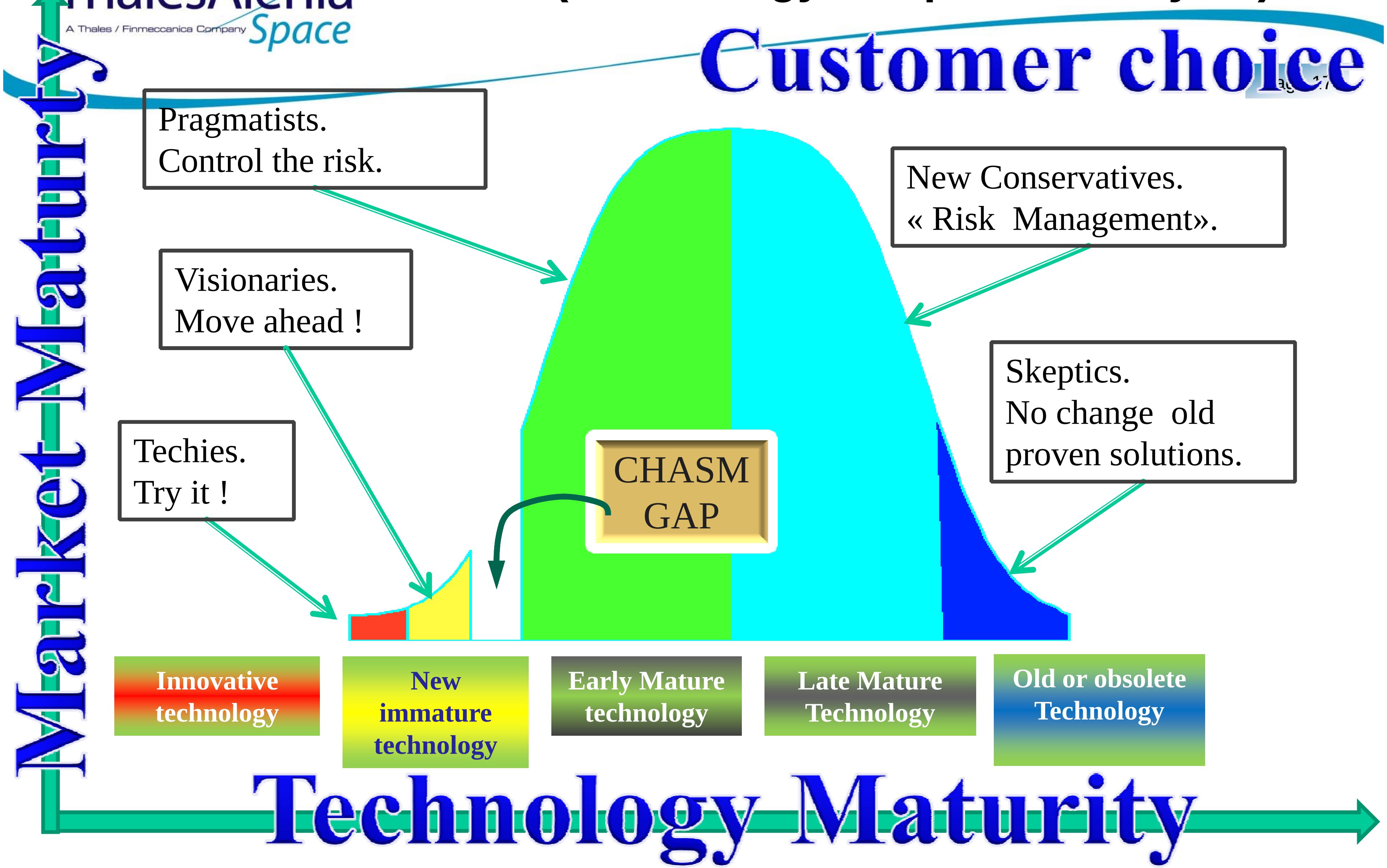
These new technologies are disruptive for Space application.

How to manage their introduction ?

The TALC (Technology Adoption Life cycle)

in the High-Tech Space market.

TALC (Technology Adoption Life cycle)



THALES

Discontinuous innovations require an infrastructure to prosper and proliferate.

Discontinuity has significant (and sometimes unintended) consequences.

Proven benefits

Existing infrastructure

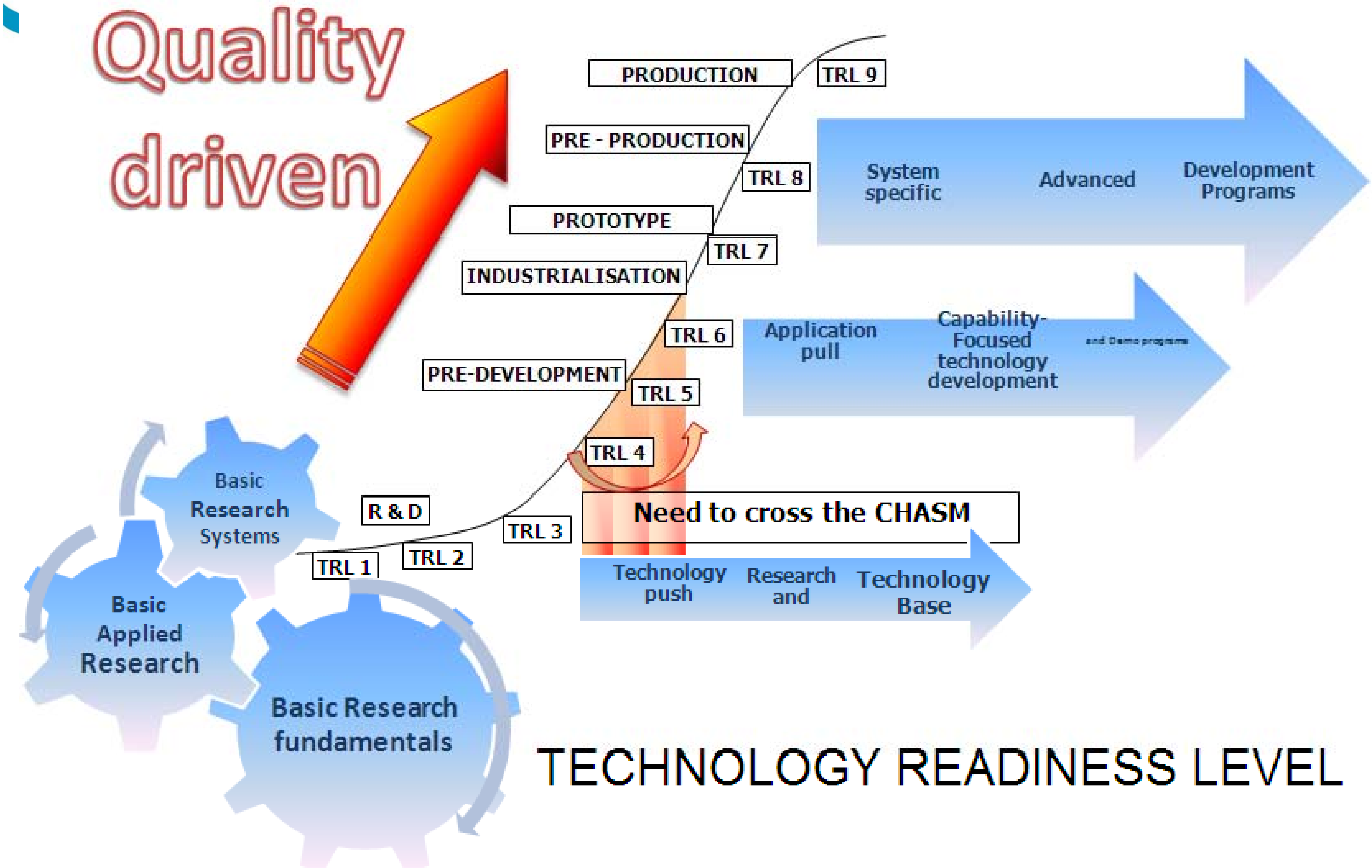
New Benefits

New infrastructure

Discontinuous innovations foster new power structures … *if they get adopted.*

HOW, WHO, WHEN TO MANAGE SUCH DISCONTINUOUS INNOVATIONS ?

All is about risk assessment: TALC and Valley of Death version applies to discontinuous innovations, meaning the product forces the user to change behaviour.



TECHNOLOGY READINESS LEVEL

How to adopt new technologies ?

Customer's decision process is based on finding objective information from reliable sources, something the vendor cannot provide.

Have you ever had someone call and ask you what kind of computer to buy ? This is a common method of lowering risk by gathering objective evidence.

We must consider :

- **THE COMPLEXITY AND VARIETY OF PRODUCTS OR FUNCTIONS**
- **HIGH TECHNOLOGY LEVEL PRODUCTS (from micro-electronics, Quantum Physics, Photonics, interaction light with matter (2D and 3D)),**
- **RAPID EVOLUTION OF THE TECHNOLOGIES AND PRODUCTS**
- **CONSTRAINTS AND STRESS ENVIRONMENTS (Thermal management, radiation, vacuum, mechanical including vibration and acceleration, …)**
- **BUILT AND DESIGN INNOVATIVE APPLICATIONS (new functions for new concepts, risk management, quality control and proof, design for performance and long term lifetime, …)**

For a pragmatic approach.

For what purpose ?

Which level of integration ?

On which parameters ?

How to define stress conditions ?

Who will be responsible ?

Which methodology ?

Industrialization concerns

Quality constraints

Screening

Evaluation

Qualification

Optical measurements

Electrical test methods

SUB-SYSTEMS	• Lev 3 : Product qualification
MODULES	• Lev 1 : Endurance qualification • Lev 2 : Packaging qualification
ELEMENTS	• Lev 1 : Characterization and qualification • Lev 1 : Environmental qualification

Existing Quality assurance tools for Micro-Opto-Electronics

European Space Agency

- ECSS-Q-ST-60-05: Generic procurement requirements for hybrid microcircuits.

JEDEC

- JEDEC JESD49 Procurement Standard for Semiconductor Die Products Including Known Good Die
- JEP149 : Application Thermal Derating Methodologies
- JEDEC-13 committee approved formation of Fiber-Optic Test & Qualification for Harsh Environment Applications Committee - JEDEC 13.6/SAE Committee
  - ✓ Objective: Bring fiber optic community to a standards level enjoyed in the semiconductor marketplace – i.e. QPL/QML for fiber-optic components.

MILITARY

- MIL-PRF-19500, General Specification for Semiconductor Devices
- MIL-PRF-38534, General Specification for Hybrid Microcircuits
- MIL-PRF-38535, General Specification for Integrated Circuits Manufacturing
- MIL-STD-883 Microelectronics Test Methods, and Procedures,
- MIL-HDBK-781A: Handbook for reliability test methods, plans and environments for engineering, development, qualification and production.

OTHER

- TELCORDIA GR-468-CORE : Generic Reliability Assurance for Optoelectronic Devices used in Telecommunications Equipment

First step before to implement Quality and Reliability Standards is

to collect best practices from Manufacturers, Industries, Agencies and Laboratories in an Optoelectronic and Reliability Handbook

To prepare Quality Standards assurance documents, it is needed :

- to prepare an handbook document
- to synthesize and to present the best practices on design, testing, industrialization, usage, quality control and production on optoelectronic products for end-use in Space Application.

A tentative was initiated to work on a common document titled :

"OPTOELECTRONICS and RELIABILITY HANDBOOK"

Today, this initiative was agreed to be enlarged and more deeply activated thanks to the effort of the existing Space community and supported by the CTB Photonics WG.

The guide is foreseen to be a high technical synthesis for :

- ✓ understanding the various aspects of Opto-Electronic devices
- ✓ behaviors under Space Environment constraints
- ✓ Semiconductor material properties and device structures along with the final products (Emitters, Receivers, Sensors, Opto-Electronic functions, passive Opto-Electronic functions)
- ✓ Performance and reliability aspects of Opto-Electronic devices.
- ✓ Failure mechanisms and analysis
- ✓ Quality assurance and qualification methodologies overview.

It will present in details Opto-Electronic device designs, packaging, development, manufacturing, industrializations, application usage, test and controls, screening sequences, qualification procedures and test methods, environment effects (Radiation, vacuum, thermal, mechanical, long term and end of life, …) and will help the reader to understand the means of developing suitable qualification plans and demonstrate high reliability equipment achievement using optoelectronic products.

CONTENT OF THE HANDBOOK

The content of this handbook is composed of chapters written by the contributors acting as honorary, benefactor or active members.

Optoelectronic handbook

Grand Chapter I
Solid State physics for optoelectronics

Grand Chapter II
Space environment constraints description.

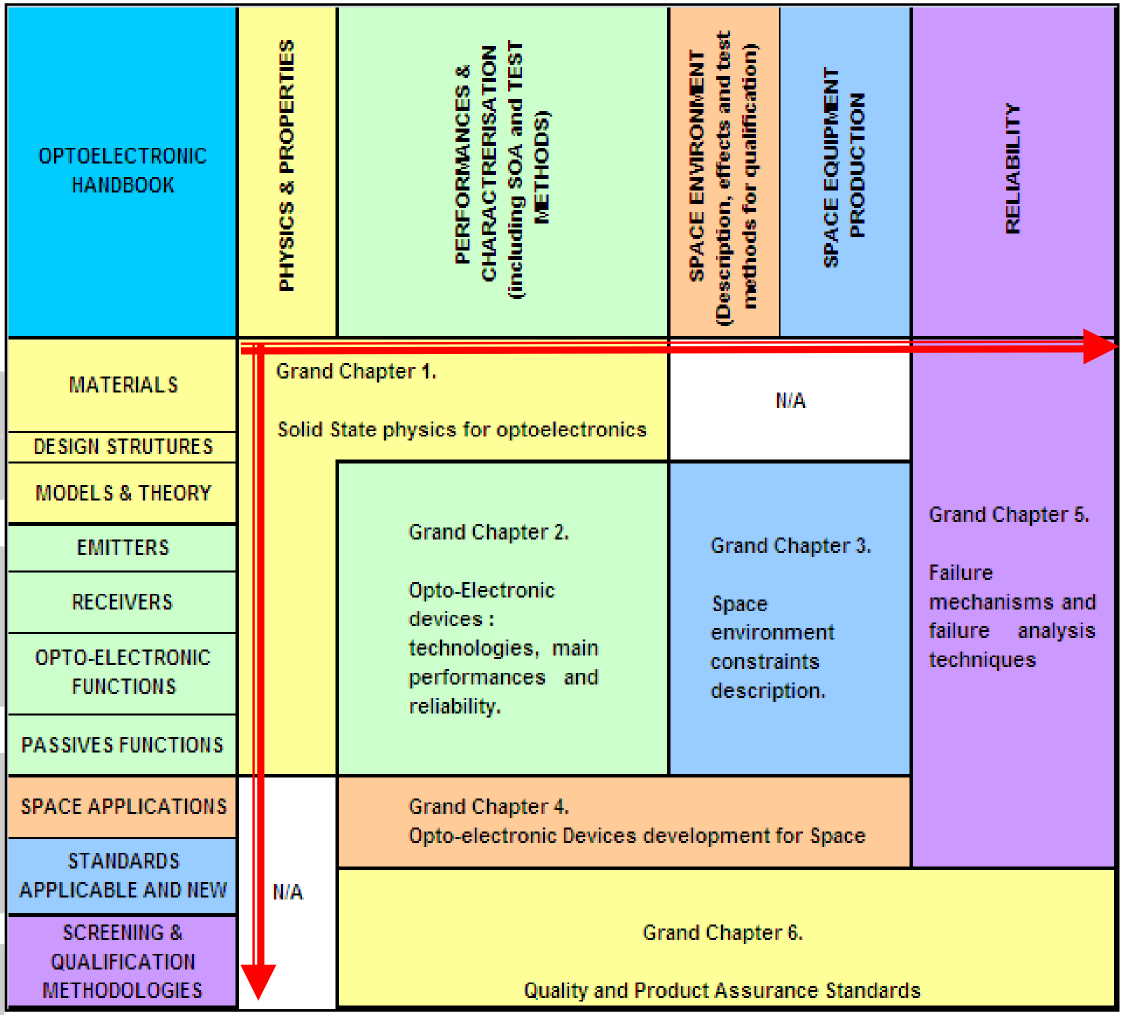
Grand Chapter III
Opto-Electronic devices : technologies, main performances and reliability.

Grand Chapter IV
Opto-Electronic Devices development for space

Grand Chapter V
Failure mechanisms and analysis

Grand Chapter VI
Quality Assurance Space Standards

Transverse thematics



Basic thematics

How to prepare this handbook ?

It is proposed a WIKI platform.

Open to anyone would like to participate in a partnership build up based on **ECM** : **E**nterprise **C**ontent **M**anagement : a collaborative platform open to all external partners.

A secured browser :

https://www-ecm.thalesaleniaspace.fr/ecm

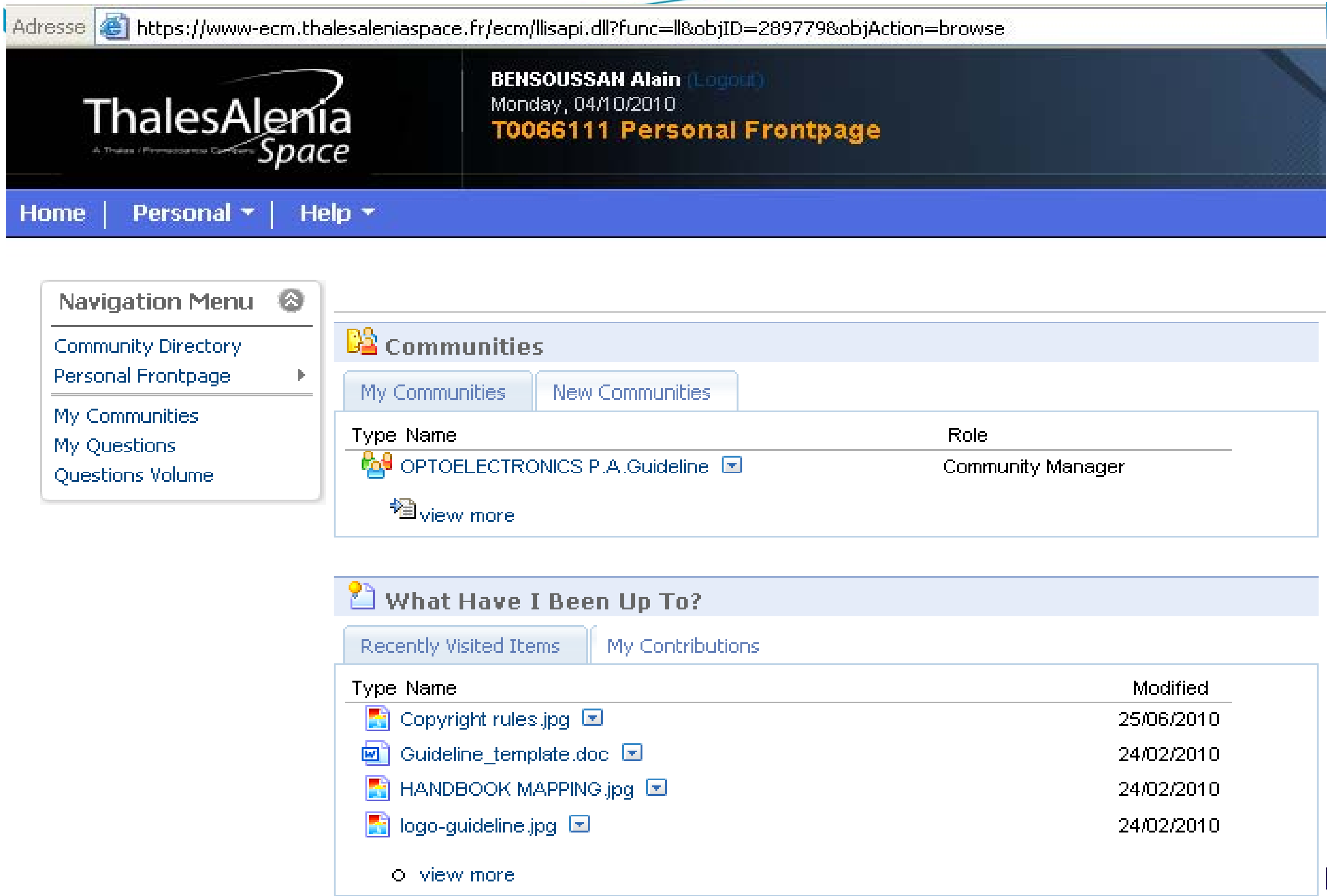
A secured browser :

https://www-ecm.thalesaleniaspace.fr/ecm

Please ask me for a free access, you will have a dedicated login and individual password attributed.

E-mail : alain.bensoussan@thalesaleniaspace.com

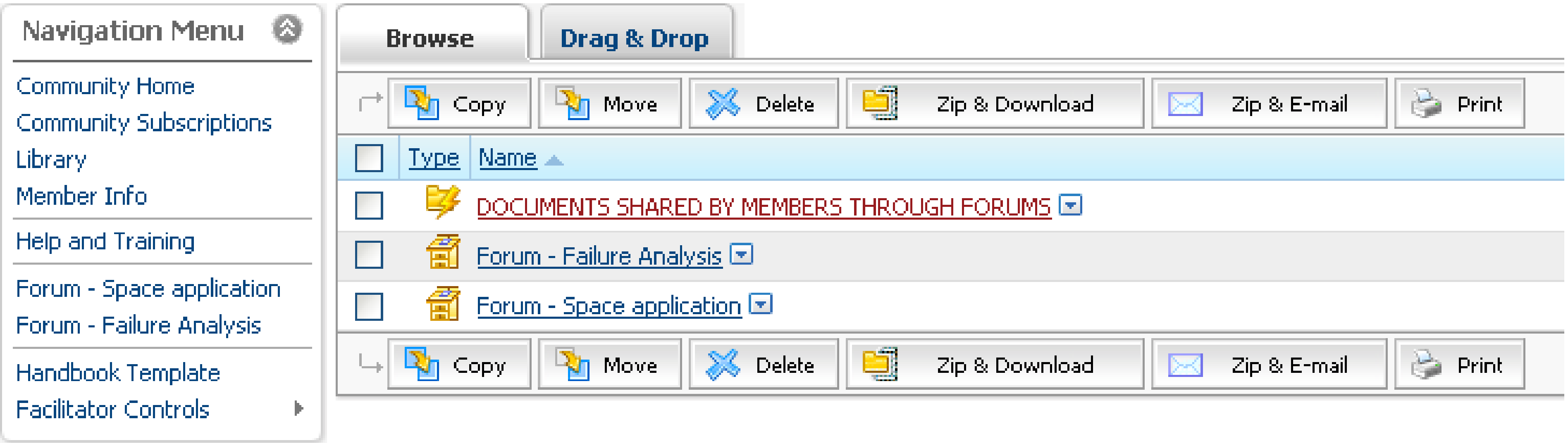
"OPTOELECTRONIC and RELIABILITY HANDBOOK"



Livelink ECM

NEW FORUMS will be implemented soon!

DOCUMENT SHARING PLATFORM



Conclusions

- Optical Links in Space Application
- Industrialization concerns and Risk management
- Quality and Reliability Needs
- Optoelectronic and Reliability handbook

Acknowledgements:

Thank you to my colleagues for their valuable inputs in the overview of Space application :

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Stephane MARIOJOULS (ASTRIUM)
Melanie OTT (NASA)
Chuck TABBERT (Ultra Communication)

Thank you

European Space Components Conference.

Challenge for Advanced Payloads:
Next generation ASICs, FPGAs and advanced Conversion components needs.

Louis Baguena: Thales Alenia Space
Mark Childerhouse: EADS Astrium

ESTEC, 15-17 March 2011

All the space you need

ThalesAlenia
A Thales / Finmeccanica Company Space

ASTRIUM
AN EADS COMPANY

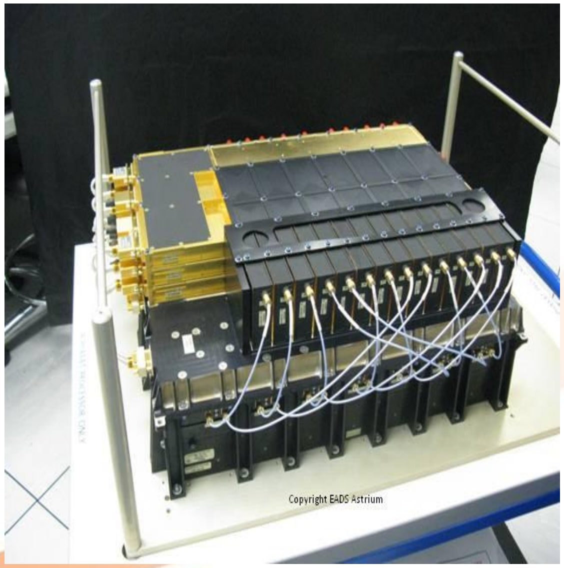
Introduction

- Many extremely valuable and highly strategic European capabilities are dependant upon space borne systems to deliver telecommunications, navigation, civil and military observation and television services.
  - These systems have become ever more complex and this trend will continue into the future.
  - This trend requires ever more complexity in the electronics and this can only be achieved in flight payloads efficiently by deploying highly integrated ASICs and FPGAs, as well as high end standard components such as ADC, DAC.
  - Unfortunately, many of these technologies are subject to ITAR restrictions and the most advanced of these may be difficult to access by European satellite manufactures.
- The purpose of this presentation is to highlight the required performances of these components and to emphasise the technology gap to be achieved.
  - If this gap can be closed, or even surpassed, in a reasonable timescale, this would significantly advantage the European space industry.

State-of-the-art

- Both companies AST & TAS are involved in telecom domain building telecommunication systems based upon Integrated processors either in OBP or Transparent processors

- ASIC main features used in Processors
  - One ASIC implementing main required functions for transparent processors such as Demux, Mux ….
  - Implementation
    - ATMEL ATC18RHA 0.18 µm
    - 132 mm^2 core area, Packages up to 625 LGA
    - Complex Logic embedding RAMs, meaning up to 5 M equivalent gates with system frequency over 300 Mhz
    - Power: up to 8W depending upon configuration



ASIC

- Extremely large and complex ASIC development
  - Stretching the technology in all parameters: area, speed and I/O.
  - Recent ASICs at limits of qualified European 180nm technology
- New applications will require Deep Sub Micron ASICs as an enabling technology in the coming years.
  - Particularly in Telecom to improve bandwidth and channels to be handled, but also in High Performance Data Handling, both demanding
    - Higher integration, lower power/gate, higher interconnection.
- Main requirements are:
  - Up to 20 million equivalent gates integration capabilities
  - Implementation of embedded HSSL (High Speed Serial Links) up to 10 gbps
  - Implementing macros such as RAMs and PLLs as a minimum
  - System frequency capability in the range of 3 to 400 Mhz

ASIC

- ASIC technology offerings from US companies will include 90nm from 2012 - but access will be restricted.

- In 2008 ESA started a project to develop European ASIC technology
  - STMicroelectronics - KIPSAT
    - Supported by Astrium and Thales Alenia Space.
    - Radiation hardened 65nm ASIC libraries
    - Multi Gbps HSSL are a key requirement of any DSM offering. Multiple HSSL inside ASICs and stand alone chips
    - High PIN count packaging with high power dissipation capabilities will be a key enabler.

- Secondary users of DSM 65nm technology
  - A move to DSM ASIC is not compulsory for many applications.
    - However, there may be considerable performance, power, integration and test benefits.
    - Price is critical for this market segment.

ThalesAlenia Space
A Thales / Finmeccanica Company

ASTRIUM
AN EADS COMPANY

FPGA

- FPGAs are preferred over ASICs in some cases
  - Smaller missions that do not have highly parallel architectures.
  - Missions with low or moderate processing rates.
  - Functions where the power and gate density overhead of the FPGA technology is manageable.
  - Functions that are control and configuration orientated.
  - Functions that might be subject to late changes.
  - Missions that cannot afford the ASIC costs or timescales.

- Many recent equipments have used anti fuse based FPGA.
  - MicroSemi RTAX, ~10K cells, ITAR restricted.

- Within Europe, comparative FPGAs are expected to be available soon.
  - Atmel ATF280K, ~14K cells in 2011. ATF450K, ~23K cells in 2012

- Offerings from US companies will include high density FPGAs (>80K cells) from 2011/13.
  - Xilinx Virtex5 SIRF, MicroSemi ProASIC4

FPGA

- In 2009, a consortium lead by Atmel proposed a new high density FPGA development to the EC.
  - Atmel RAHDHIFFS FP7 proposal based on Abound Logic architecture targeting 65nm technology.
  - Supported by Astrium and Thales Alenia Space.
  - Unfortunately, this development has not started.
  - European satellite manufacturers continue to encourage the development of ITAR free, very large cell count FPGAs.
- Emerging US FPGA technologies might be used in future if their suitability is established.

Conversion

- *ADCs/DACs are key components of digital satellite payloads.*
- *Without ADCs/DACs, payload processors for telecommunication, navigation, Earth observation and space science satellites would simply not exist.*
- *ADCs and DACs have been flown on all missions where digitalization equipments are used .*

ADC/DAC specification requirements to fulfil future customer needs

- ***Single power supply rail devices***
- ***Low power consumption, i.e. < 2W***
- ***ENOB performance > 11 bits***
- ***The ability to synchronise multiple devices***
- ***The ability to null part-to-part spreads***
- ***No in-band, non-carrier related spurs***
- ***Wideband ADCs***
- ***Return-to-zero DACs***

Conversion

- ***European ADC/DACs must offer technical and commercial advantage to European satellite manufacturers when competing for global satellite contracts.***

- ***European ADC/DACs which offer comparable performance to existing parts and enter the market late will never succeed as there is no added value for European payloads and the cost to re-design is too expensive.***

Summary

- There is a clear need for DSM ASIC technology with HSSL to enable:
  - Next Generation Telecom Payload and High Performance Data Processing Products
    - Attractive pricing would further broaden the application scope and subsequent part quantities.
- FPGA
  - For moderate cell count devices (>10K) US parts are available now.
    - Comparative European FPGA parts are expected in 2011/12.
  - For very large cell count devices (>80K) US providers have indicated availability in 2011/13.
    - European satellite manufacturers continue to support the development of ITAR free, very large cell count FPGAs.
- ADC/DAC
  - European parts must offer a technical and commercial advantage.
- Questions?

CENTRE NATIONAL D'ÉTUDES SPATIALES

ESCCON 2011
European Space Components Conference

March 15-17, 2011

Challenge for advanced payloads : Next generation ASICs, FPGAs and Advanced Conversion components Development

Florence MALOU, David DANGLA - CNES
Laurent HILI, David MERODIO - ESA

Outline

- **Introduction**
- **DSM Technologies**
- **DSM Program**
- **Data Converters**
- **ASIC technology**
- **FPGA**
- **Conclusion and way forward**

Introduction

- Space needs DSM technology
  - The availability and performance of European components is a key issue for European Industry to deliver the next generation of digital payloads
- The Deep Sub Micron (DSM) initiative, coordinated within the frame of the CTB, identified critical technologies for next generation telecommunication satellites :
  - Broadband ADC and DAC
  - HSSL
  - digital ASICs
  - FPGA.
- ESA TRP, CNES Strategic components and European Community FP7 budgets have been used to develop and evaluate, according to ESCC standards, these strategic components and technologies, with requirements :
  - Rad-hard (100Krad), SEL immune,
  - Reliable (20 years lifetime)
  - Operating in military temperature range (-55°C/+125°C)

Those programs will improve satellites manufacturers competitiveness by enabling an independent European components procurement

Outline

- Introduction
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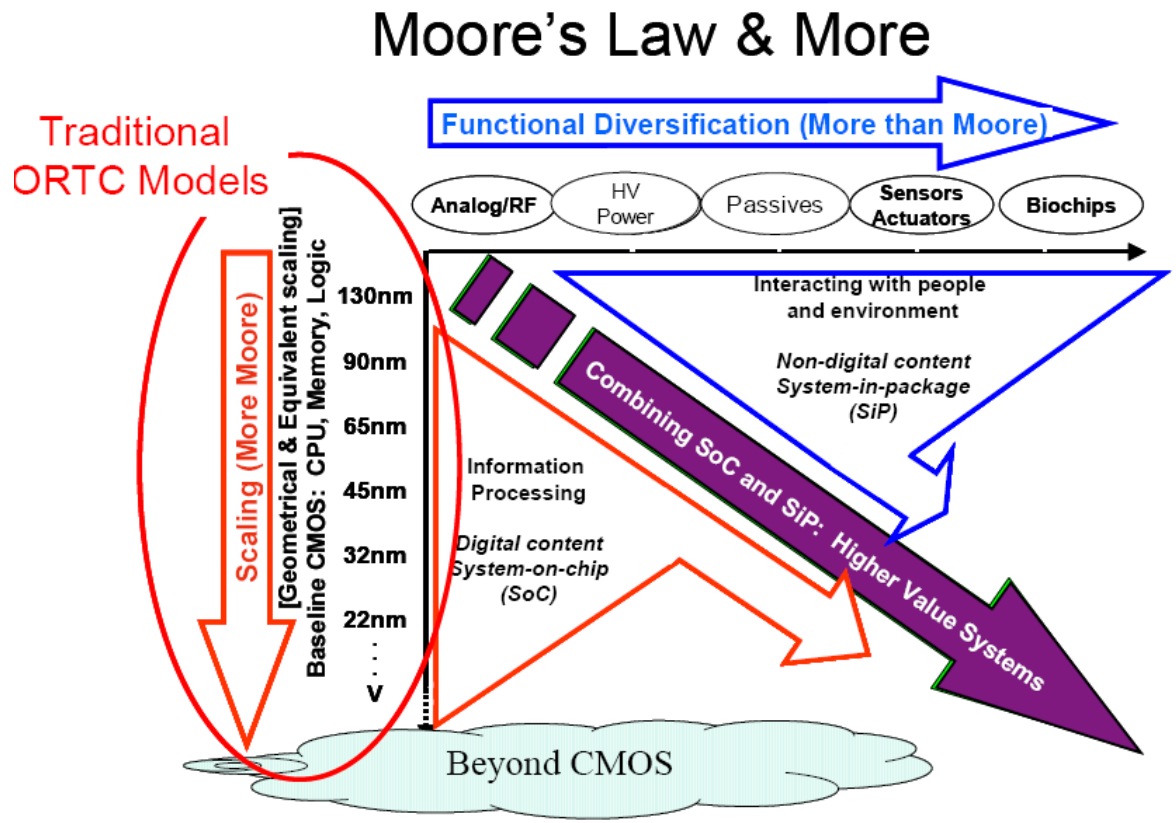
Moore law

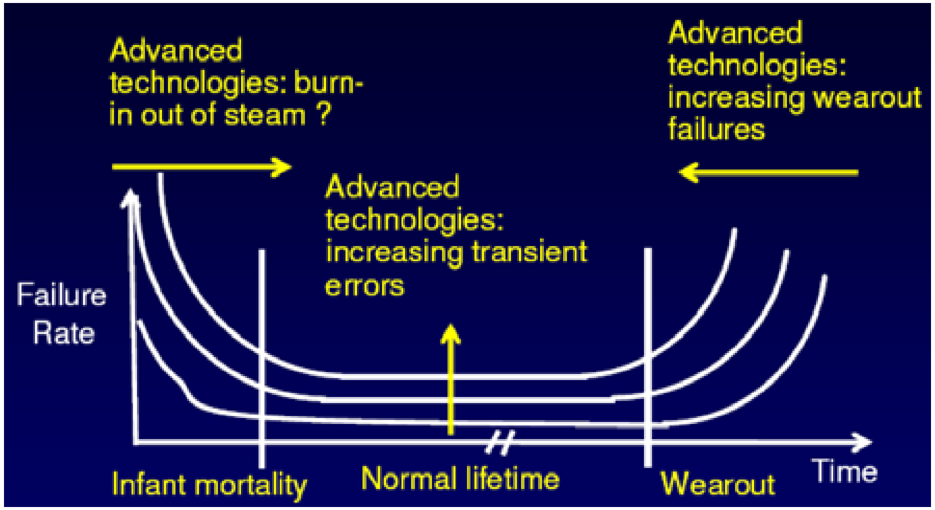
- According to Moore's Law, technology are still speedily evolving
- The downscaling of minimum dimensions enables the integration of an increasing number of transistors on a single chip
- DSM technology = 90nm and beyond
- Payload Processor ASIC requirements (10-30 Millions gates, 6Gbit/s Serial I/Os, Low dissipation …) and Next Generation general purpose ICs (NG-Microprocessor, NG-FPGA) are only achievable with Deep Sub Micron



Source: 2009 ITRS Executive summary

Reliability

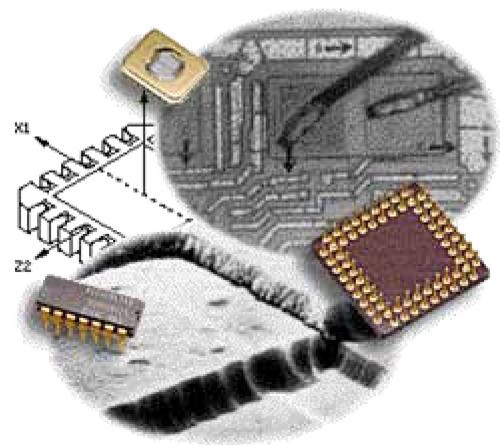
- Process development of DSM technologies is becoming more and more challenging
- The rising reliability concerns are closely related to :
  - the reduction of critical dimensions,
  - the increase in electrical field strength and in interconnections current densities
  - and to the use of new materials/processes.
- New preponderant Failure mechanisms :
  - Hot Carrier Injection (HCI)
  - Negative Bias Temperature Instability (NBTI)
  - …



Source : Subhasish Mitra (Stanford University),2005

Mandatory

- To insure Reliability for space DSM technology :
  - DSM lifetime has to be early taken into account
  - DSM reliability parameters have to be correctly chosen and modeled for lifetime simulation purpose
  - Manufacturer involvement is a critical issue : close relationship is needed



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Combining ESA and CNES efforts and budgets

	phase 1 first iteration design / prototyping	*phase 2* second iteration design / prototyping and ESCC evaluation	*phase 3* qualification according to ESCC standards
asic technology • harden library • high speed serial link • high pin count package	**T.R.L 3/4** **TRP Budget 1.2M€** **CNES Budget 60K€**	**T.R.L 5** **CNES Budget 1.43M€** **TRP Budget 2.5M€**	**T.R.L 8**
analog to digital converter	**T.R.L 4** **TRP Budget 0.9M€**	**T.R.L 5** **FP7 Budget 2M€**	**T.R.L 8**
digital to analog converter	**T.R.L 4** **TRP Budget 0.9M€**	**T.R.L 5** **CNES Budget 0.89M€**	**T.R.L 8**

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E2V EV10AS180
Low power 10-bit 1.5 Gsps ADC

ESA TRP - 900K€ + COMETS - European Community's 7th FP under grant agreement n° 242521 - 2M€

- **Objective : Development and ESCC evaluation of the E2V EV10AS180 1.7W L-Band 10-bit 1.5 Gsps ADC**
- **Consortium : E2V(F), INFINEON (G) , TAS (F), ASTRIUM (UK), CNES (F), CNRS IEMN, Xlim (F)**
- **Schedule :** T0 = Feb 2008 – End = Q3/12

- **Main Features**
  1.5 Gsps Guaranteed Conversion Rate Selectable 1:1/2/4 DEMUX LBand 1.7 W Power Dissipation
  CI-CGA255 Package B7HF200 SiGeC technology from Infineon (G) 100Krad Radiation tolerant
  Low latency < 4 cycles times

- **Key Performances**
  - **2.2 GHz Full Power Input Bandwidth (-3 dB)**
  - **Single Tone Performance @ Fs=1.5Gsps :**
    - SFDR = -60 dBFS, ENOB = 8.5 Bit; SNR = 55 dBFS at Fin = 750 MHz @-12 dBFS
    - SFDR = -60 dBFS, ENOB = 8.4 Bit; SNR = 53 dBFS at Fin = 1800 MHz @-12 dBFS
  - **Broadband Performance:**
    - NPR = 44 dB at -13 dBFS Optimum Loading Factor in 1st Nyquist
    - NPR = 43 dB at -13 dBFS Optimum Loading Factor in L-band
- **Status :**
  - **Design Completed with First prototypes showing very good dynamic performances but still some improvements needed design respin**
  - **Design respin completed**
  - **Final Silicon under electrical characterization by E2V**
  - **ESCC evaluation will start in Q2/2011**

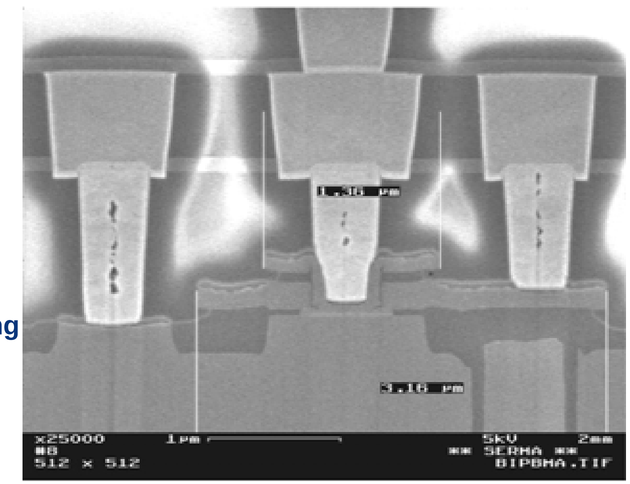
EV10AS180 ADC in EPPL in Q3/12

E2V Low power 12-bit 1.5 Gsps ADC

COMETS - European Community's 7th Framework Programme under grant agreement n° 242521 - 2M€

- **Objective : Design and Characterization of the 12-bit ADC by E2V and end-users**
- **Consortium : E2V(F), INFINEON (G) , TAS (F), ASTRIUM (UK), CNES (F), CNRS IEMN, Xlim (F)**
- **Schedule :** T0 = May 2010 – Duration : 36 months

- **Key Features :**
  - 1.5Gsps conversion rate (no on-chip interleaving)
  - L band application
  - Selectable ratio DMUX output (1:1/1:2)
  - Low latency
  - User friendly feature
  - LVDS compatible
  - B7HF200 SiGeC technology from Infineon (G)
- **Status :**
  - Ongoing characterization work for improved B7HF200 technology device modeling by IEMN and XLIM
  - Test chip under validation with encouraging preliminary results
    Single Tone Performance @ Fs=1.5Gsps :
    - SFDR < -70 dBFS, ENOB = 9.4 Bit; at Fin = 750 MHz @-12 dBFS
    - SFDR < -70 dBFS, ENOB = 9.3 Bit; at Fin = 1800 MHz @-12 dBFS

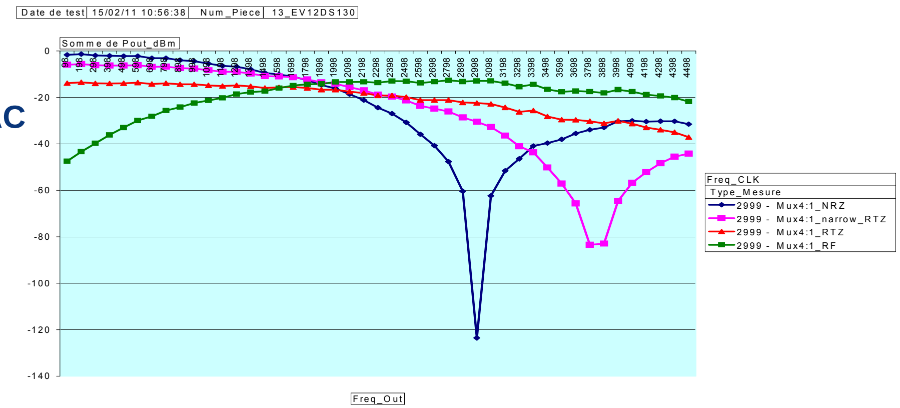


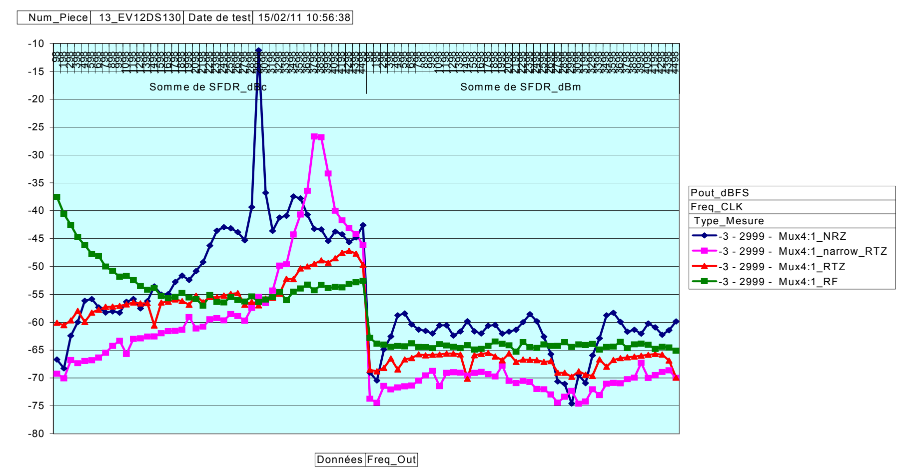
SiGeC B7HF200 technology cross-section

12-bit ADC validated prototypes in Q2/13

Data Converters

E2V EV12DS130
Low Power 12-bit 3 Gsps DAC with 4/2:1 MUX





CNES Strategic Component Plan – 890K€

- **Objective : Development and ESCC eval. of the 12-bit 3 Gsps DAC**
- **Contractor : E2V(F)**
- **Schedule :** T0 = Nov 2009 – End = March Q3/12

- **Main Features :**
  - **12-bit resolution** — **3 Gsps Conversion rate**
  - **4:1 or 2:1 built in MUX (selectable)** — **1.3 Watt Power Dissipation**
  - **NRZ, Narrow RTZ, 50% RTZ, RF modes** — **100Krad**
  - **Ci-CGA255 Package, B7HF200 SiGeC technology from Infineon (G)**

- **Key Performances (charact. results):**
  - **Time domain: Full swing Rise Time=60ps**
  - **Broadband : NPR at -14dB loading factor, and Fs=3Gsps**
    - 1st Nyquist (NRZ or NRTZ): NPR= 47.4 dB ➔ 9.4 Bit equivalent
    - 2nd Nyquist (RTZ or RF): NPR= 40 dB ➔ 8.2 Bit equivalent
    - 3rd Nyquist (RF): NPR= 38.5dB➔ 7.9 Bit Equivalent
  - **Single tone (see plots of the four modes):**
    - Pout for Fout from 100MHz to 4.5GHz at 3Gsps
    - SFDR (dBc) and HSL(dBm) four Fout from 100MHz to 4.5GHz Aout=-3dBFS, 3Gsps (Bottom plots)

- **Status :**
  - **Design completed in March 2010**
  - **Silicon under electrical characterization to assess that is the final one**
  - **ESCC evaluation will start in April 2011**

EV12DS130 DAC in EPPL in Q3/12

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65nm CMOS technology

- 65nm-LP CMOS from ST France : European technology, ITAR free
- Payload Processor ASIC requirements (10-30 Millions gates, 6Gbit/s Serial I/Os, Low dissipation …) are only achievable with Deep Sub Micron
- Next Generation general purpose ICs also need DSM: NG-Microprocessor, NG-FPGA

- 65nm CMOS commercially qualified in 2007
- 65nm CMOS Core Process :
  - Dual / Triple Gate Oxides
  - Dual / Triple Threshold Voltages for MOS Transistors
  - 7-9 Full Copper Dual Damascene Interconnect Levels
  - 0.20µm metallization pitch
  - Low K (dielectric)
- Characteristics :
  - 750 kgates/mm2
  - 2GHz stdcells
  - 5.7nW/(MHz x gates)
  - 1.25-7.5GBit/s High Speed Serial Link (HSSL) modules
  - Flip-Chip packaging needed

❖ST proposed its CMOS 65nm-LP process for space
❖Reliability maximization and Radiation hardening at process and design stages

ASIC technology

ST 65nm CMOS technology / Space Library

1st Step

Pre-assessment and 1st developments

Stand-alone HSSL Development

KIPSAT (ESA TRP)

2nd Step

Space Library offer

(Rad-hard cells, Memories, PLL, HSSL, cold spare I/O …)

LIB-EVAL (CNES)
+
New ESA TRP

3rd Step

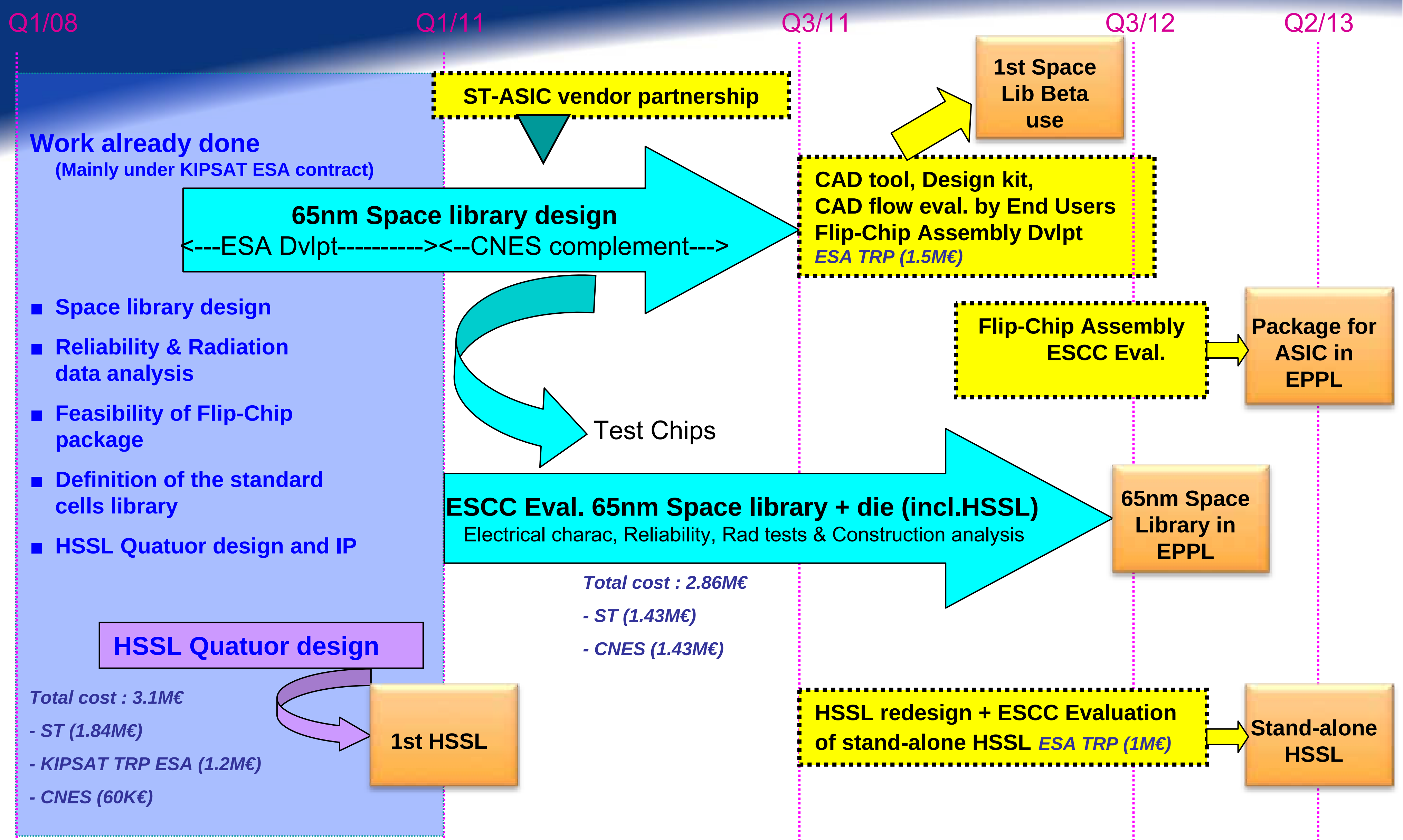
Optimized Space Library offer

Flip-Chip package and stand-alone HSSL

New ESA TRP
+
tbd

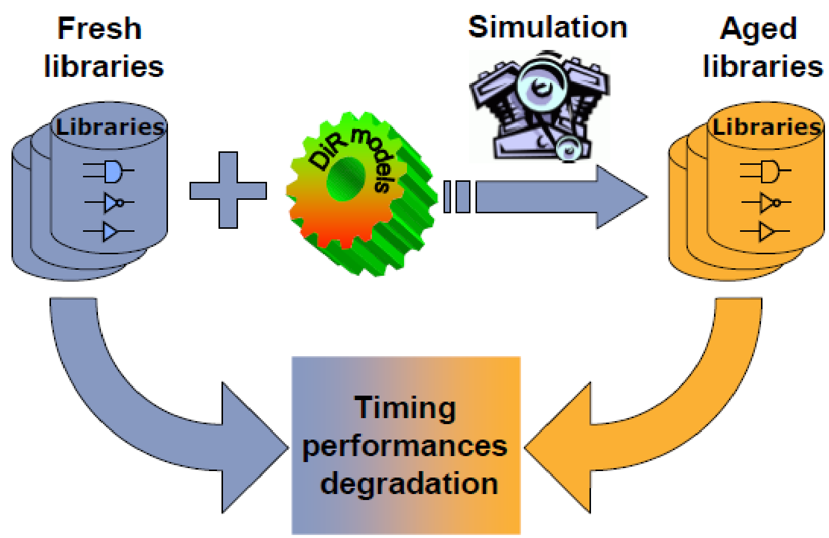
ASIC technology

Activity to be funded or performed/started



Reliability maximization

- Systematic application of ST Design in Reliability (DiR) methodology :
  - focusing HCI and NBTI with dedicated tools for ageing simulations
  - Eventual specific layout rules for reliability enhancement
- Application of ST Design for Manufacturing (DfM) :
  - Study of tighter controls at process level
  - Analysis of reliability figures from Std qualification



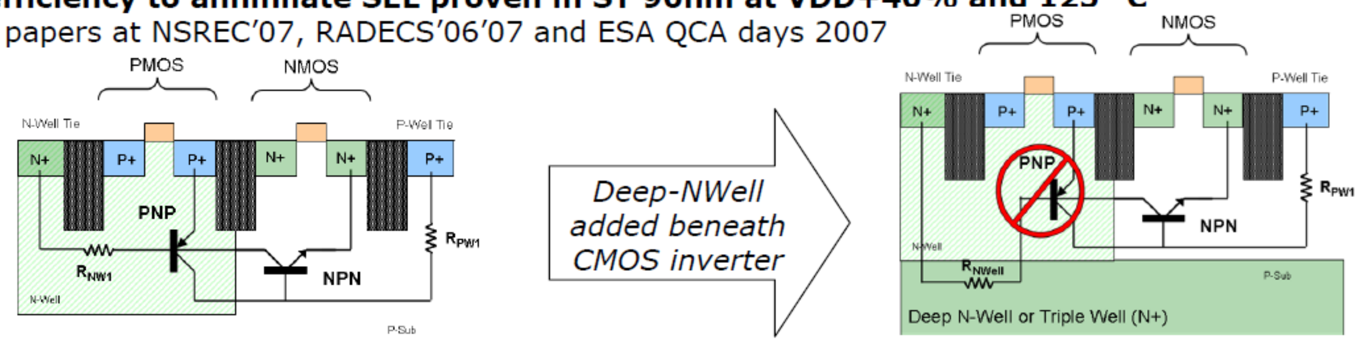
- ST has built an industrial flow which allows a full coverage of reliability effects all along the product value chain
- Reliability tests will be also performed during ESCC evaluation

Radiation hardening

- Rad-hard capabilities measured under ESA contracts (ST 130nm, 90nm, 65nm and 45nm)
  - No current increase seen up to 300krad(Si) TID
- SEL-free with Deep-N well process option

DNW efficiency to annihilate SEL proven in ST 90nm at VDD+40% and 125 °C

- ST papers at NSREC'07, RADECS'06'07 and ESA QCA days 2007



- SEE/SETs fault injection techniques for Digital and Analog blocks sensitivity analysis
- Usage of existing Robust cells, TMR
- Hardening of clock-trees against SETs
- Shadowing of configuration registers + scrubbing
- Development of Rad-Hard new cells
- Layout techniques

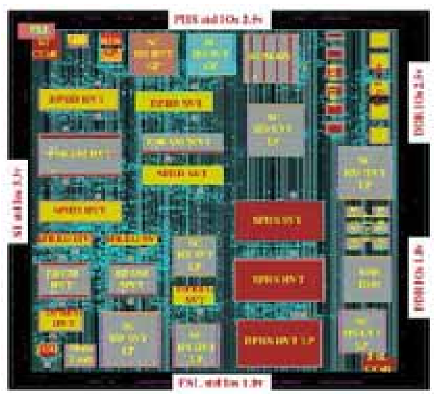
ESCC Evaluation

■ Evaluation Test Programme :

- Representative Test chips manufacturing of the Space library
- Electrical characterization of representative the Test chips
- Reliability tests addressing NBTI and HCI to confirm life time of 20 years @ Tj=110°C
- Radiation tests : TID, SEE under heavy ions and protons
- Construction analysis

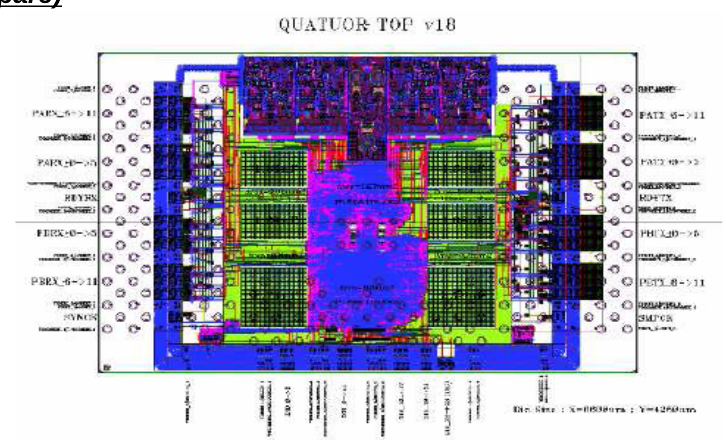
TC1 (rad hard library):

TC4 (commercial library subset):



TC2
(PLL + IOs cold spare)

TC3 (HSSL) **Quatuor / 4 x 6.25 Gbps**



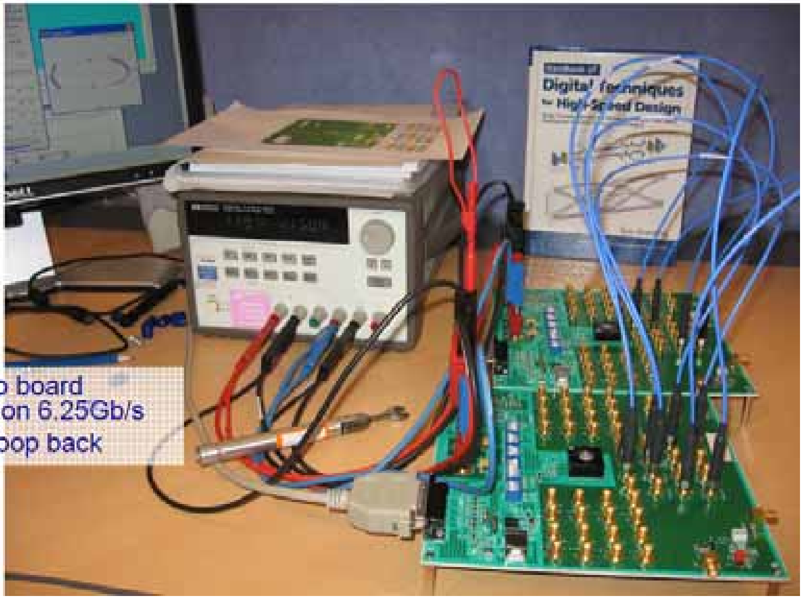
65nm space library in EPPL in Q3/12

Quatuor HSSL

- **Functional specification :**
  - **1 clock slice + 4 data slices**
  - **24 // LVDS port in + 24 // LVDS port out at 375Mhz DDR max**
  - **24 digital IOs to support I²C, SPI, UART, JTAG, TIC, MDIO protocols**
  - **Max Serdes rates are :**
    - 25Gbps Tx simplex
    - 25Gbps Rx simplex
    - 50Gbps full duplex with 4 active lanes (25Gbps Tx / 25 Rx). Full duplex mode limited to 2 active lanes due to power dissipation. 12.5Gbps Tx / 12.5Gbps Rx

- **Statuts :**
  - **Design completed under KIPSAT ESA TRP**
  - **1st silicon available in Q3/10**
  - **Electrical characterization on going :**
    - Functionality validated, some minor bugs identified
  - **Heavy ions tests report and Preliminary reliability test on going**

- **HSSL + IP completion is planned under new ESA TRP**



4 x 6.25Gbps HSSL prototypes available

Outline

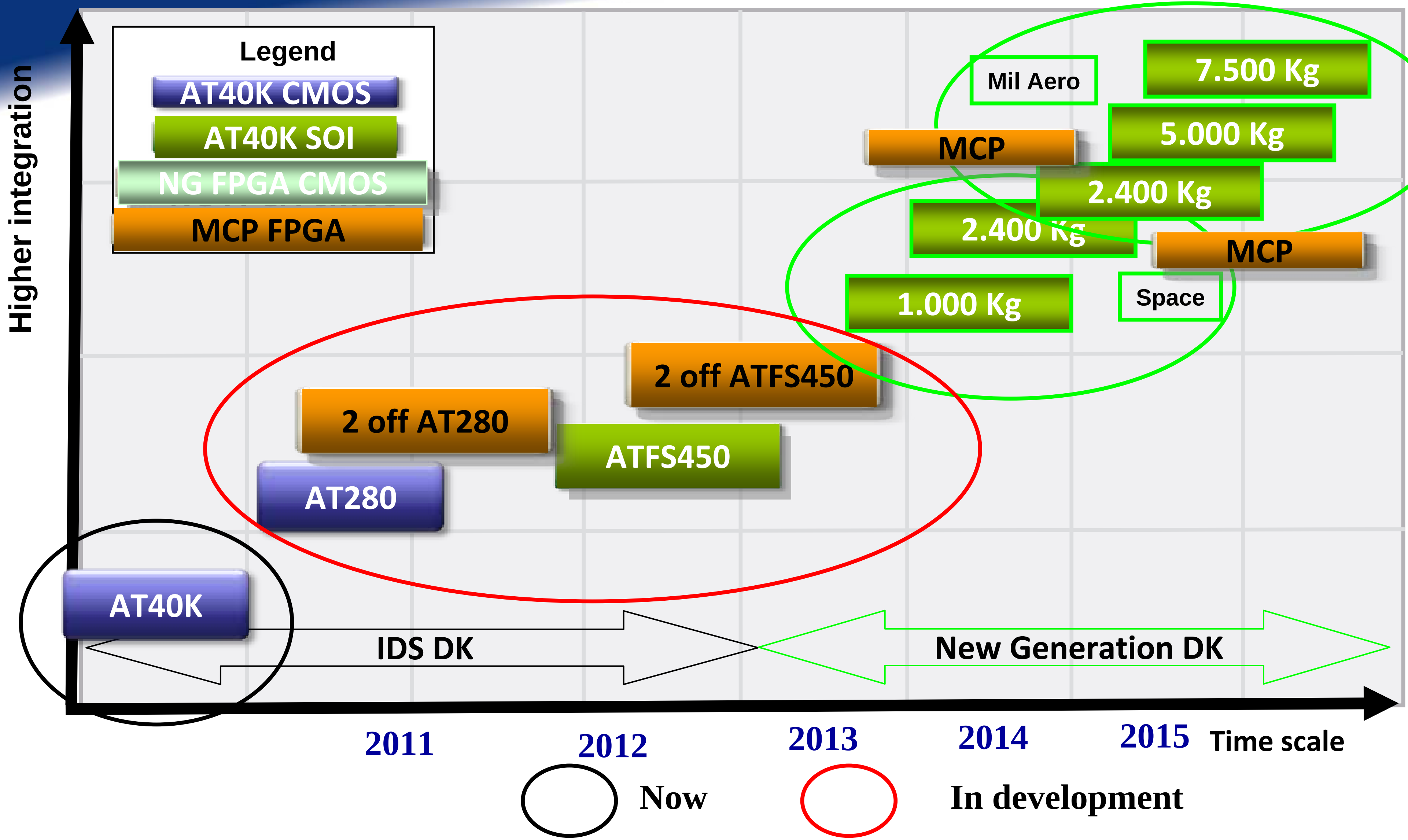
- Introduction
- DSM Technologies
- DSM Program
- Converters
- ASIC technology
- FPGA
- Conclusion and way forward

FPGA

- Current status :
  - ACTEL is the leader but without reconfiguration capabilities with up to 500Kg/100MHz, process 150nm
  - ATMEL is coming with ATF280F and ATF450, SRAM based, for a complexity of 280Kg/50MHz and 450Kg/75MHz.

- The needs for the Next Generation European reprogrammable FPGA are :
  - a DSM technology,
    - such as the specific 65 nm CMOS process technology currently developed at ST
    - current US FPGA space program is the “ SIRF ” from Xilinx (SEU Immune Reconfigurable FPGA) based on their Virtex-5 family.
  - a new field reprogrammable logic architecture with the associated tools,
    - such as already existing (ex-)Abound Logic FPGA architecture developed in Europe and whose main features are :
    - a highly hierarchical architecture allowing for very deterministic propagation times, gates utilization ratio as high as 90%, low operating power and half the bit stream size of any of their competitors,
    - a good trade off between programmable logic, on one side, and memory and mathematical function blocks, on the other side.

Xilinx Virtex5 SIRF	ATF280F	ATFS450	NG-FPGA
450 MHz	50 MHz	75 MHz	tbd
844 IOs	308 IOs	214 IOs	tbd
1.3 Mgates	280 Mgates	450 Mgates	1-2.4 Mgates
65nm (TSMC)	180nm (LFoundry)	150nm SOI (OKI)	90nm/65nm (UMC/ST)
Mature HW architecture	Old, limiting HW	Old, limiting HW	Advanced new HW IP
Mature SW	Old, limiting SW	Old, limiting SW	Advanced new SW IP



Higher integration
Legend
AT40K CMOS
AT40K SOI
NG FPGA CMOS
MCP FPGA
Mil Aero
7.500 Kg
5.000 Kg
MCP
2.400 Kg
2.400 Kg
MCP
1.000 Kg
Space
2 off ATFS450
2 off AT280
ATFS450
AT280
AT40K
IDS DK
New Generation DK
2011
2012
2013
2014
2015
Time scale
Now
In development

ATMEL/OKI/HIREC ATFS450E
450Kg FPGA on OSC 0.15µm SOI technology

CNES Strategic Component Plan – 800K€

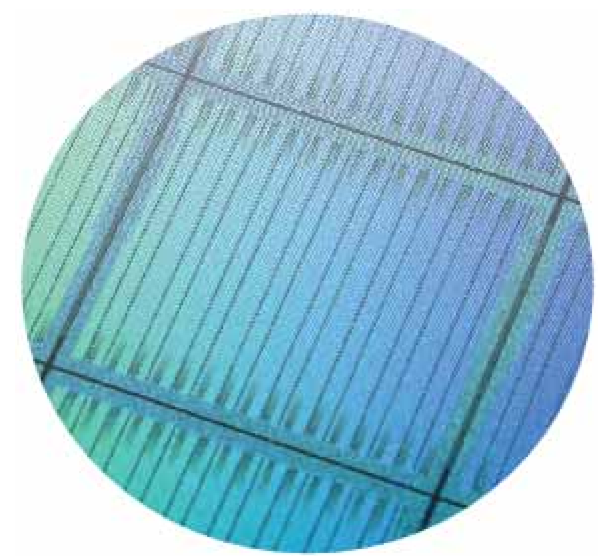
- **Objective : 450Kg FPGA Development (Joint ATMEL and HIREC development with CNES and JAXA support)**
- **Contractor : ATMEL (F)**
- **Schedule :** T0 = Q4/08 – End = Q3/12
- **Key Features :**
  - 450K equivalent ASIC gates☐ 152x152 core cells
  - 75 MHz internal performance ☐
  - 3.3V and 1.8V programmable IO and 1.5V array bias voltages
  - 8 Global SEU/SET immune Clocks
  - OSC 150nm SOI process☐
  - Package MQFPF256 (118 IOs), MQFPF352 (214 IOs)
  - Latch-up free SEU/SET free at LET of 64 MeV/mg/cm² ☐ 100 krad
- **Status :**
  - Design completed in Q4/10
  - Silicon under assembly for electrical characterization
  - Prototypes availability : Q3/11
  - ATMEL industrialization and internal Qual : Q3/12
  - ESCC evaluation report (Activity to be funded): Q1/13

ATFS450E FPGA in EPPL in 2013

1Mg – 2.4Mg Rad-Hard reconfigurable FPGA based on a new architecture

ESA TRP- High density European rad-hard SRAM-based FPGA :
Abound-Logic-based first validated prototypes – 2M€
+ European Community's 7th Framework Programme – RADHIFFS – 2M€
+ Necessary complementary fundings are needed

- **Objective : Develop a reconfigurable rad-hard by design FPGA based on Abound Logic architecture**
- **FP7 Consortium :** ATMEL (F), Abound Logic (F), ASTRIUM (G, F et UK), CNES (F), EADS IW (F), Politecnico torino (I), Space Research Center PAS (Poland), Surrey University (UK), TAS (F), Tubitak Uzay (T), University of Padova (I), AICIA Sevilla (Spain)
- **Schedule :** T0 = not started, duration : 3 years
- **Status :**
  - Abound Logic FPGA IP has been sold to Meta Systems subsidiary of Mentor. ATMEL is in negotiation with Meta Systems,
  - ATMEL proposes to proceed in 2 steps (TBC) :(1tile = ATF280F capacity)
    - a 1Mg FPGA (4 tiles) : Space rad-hard FPGA manufactured in UMC 90nm technology (TBC)
    - a 2.4Mg FPGA (9 tiles) : Space rad-hard FPGA manufactured in ST 65nm technology (TBC)



2.4Mg FPGA in EPPL in 2015

Outline

- Introduction
- DSM Technologies
  - Moore law
  - Reliability
- DSM Program
- Converters
- ASIC technology
- FPGA
- Conclusion and way forward

Conclusion and way forward (1/2)

- The DSM initiative, initially driven by next generation telecommunication satellites, and coordinated within the frame of the CTB, identified critical technologies, namely Broadband ADC and DAC, HSSL, digital ASICs and FPGA for for high integration and processing power applications.
- Strong efforts from ESA, CNES and European Community to support the development and ESCC evaluation of these strategic technologies.
- First ADC, DAC and HSSL prototypes and First 65nm Space Library test-chip are available showing Encouraging results
- Development and ESCC Evaluation on-going
- Highlights :
  - End-users involvement and European harmonisation efforts
  - Close relationship with manufacturers
  - DSM reliability was early taken into account in technology selection and design phases

Conclusion and way forward (2/2)

- Technical and Business Challenges ahead:
  - Establish advance space-quality packaging solutions for DSM ICs
  - Secure more institutional funds (EEE critical components) to complete developments and qualification
  - Establish sustainable business models for European DSM supply chain.
  - Partnerships between manufacturers or key vendors (Foundries, Assembly and Test houses) and institutional support (ESA, Agencies, EC) are a must to succeed and maintain a small volume / expensive technology market, always driven by big volume commercial technology and products.
  - Though always low volume, general purpose converters and DSM ICs such as Microprocessors, reprogrammable FPGAs, DSPs should help sustain the business model, in addition to dedicated high-end ASICs for NG Telecom and Scientific payloads.

We should continue our efforts to give access to European DSM technologies to ensure the competitiveness of European equipment manufacturers

Thank you !

Any questions ?

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