SECTION 4. ARTIFICIAL RADIATION ENVIRONMENTS IN ORBIT

4.1. GENERAL

In the natural space environment, intense, transient pulses of ionising radiation do not occur except in the form of single-particle events. However, it is possible that even civil satellites may be exposed to the effects of distant nuclear weapons exploded in space, as happened in the 1962 "Starfish" nuclear test. In the future, exposure to pulsed beams of ionising radiation from spaceborne particle accelerators, X-ray generators or nuclear reactors is also possible. We will therefore give a brief account of "Transient Radiation Effects in Electronics" (TREE) and give references to the very extensive sources of information which have been generated mainly by defence agencies. An unclassified version of the yields from a nuclear event is given in Figure 4.1

4.2. WEAPON EFFECTS

A nuclear explosion generates a very short (20 ns) pulse of gamma rays from nuclear reactions, and X-ray, neutron and electromagnetic pulses which may last for milliseconds. Particle accelerators and X-ray machines can generate continuous beams, but are often operated in a series of pulses of microsecond duration. The exposure of a device to one of these sources will produce:

(a) dose-rate or "transient" effects (e.g. photocurrents),

(b) "total dose" or long-lived effects (e.g. charging or bulk damage).

There is likely to be "rapid annealing" of the material response during the first few seconds, then more gradual relaxations over many hours. In logic circuits, the transient photocurrents generate spurious signals and may produce "logic upset" or, at higher intensities, induce thermal destruction. In some semiconductor devices containing 4-layer junction structures, a low impedance condition, known as latchup may be triggered. Latchup leads to thermal destruction caused by the energy from the power supply.

"Logic upset" is fundamentally a transient effect, but - in some circuits - may have a permanent result. For example, while a simple NAND gate, set in the logic "1" state, may transiently indicate a "0" state during the burst, it will return to the "1" state within microseconds. A bistable circuit such as a memory cell may return to the original state or, instead, change to the opposite state. These two upset effects are called "temporary" and "permanent" respectively.

Brucker has tabulated some general values for the levels of pulsed radiation environment at which the above effects take place in certain CMOS and bipolar integrated circuits. These levels are given in Table 4(1). Only orders of magnitude are stated here, but the data still supply useful guidance for system engineers and circuit designers. Brucker notes that bulk CMOS logic gates can be used in a transient radiation environment (20 nanosecond pulse) if they are not required to operate during the radiation burst. Limiting resistors or SCR crow bars can be used on CMOS voltage supplies as protection against latchup. Bulk CMOS shift registers or memories are vulnerable if they are required to store data through a radiation burst without loss. These devices are subject to permanent upset or scrambling of stored data. SOS CMOS shift registers, memories or logic gates can be used in a transient environment without risk of latchup. Logic gates are still subject to temporary and permanent upsets, but the limiting dose rates of the SOS devices exceed those of the bulk devices by at least an order of magnitude.

Brucker comments further that upset and latchup rates are strongly dependent on the circuit design and that the reduction of operating voltage from 10 to 5 volts increases by at least a factor of two the dose rate threshold for latchup. In some circuits, latchup dose rates may be very high. For example, the CD4061 is very resistant to latchup. In a transient environment, the higher noise immunity of CMOS devices makes them preferable to TTL.

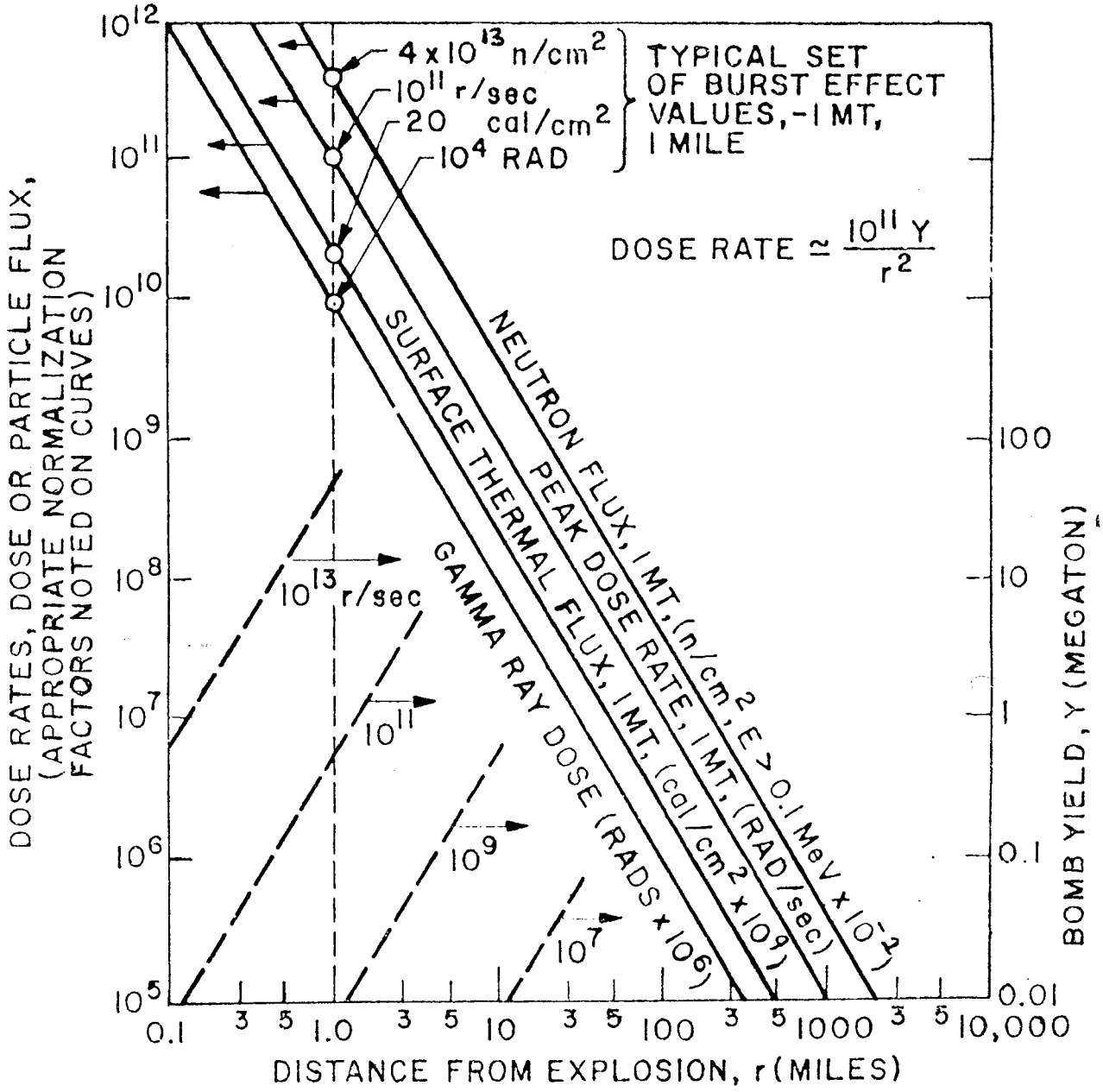

FIGURE 4.1 - NOMINAL RADIATION LEVELS FROM NUCLEAR EXPLOSIVES IN SPACE

TABLE 4.(1) - SOME UPSET LEVELS FOR CMOS CIRCUITS

	Effect	General range
CMOS/BULK LOGIC GATES		
	Temporary upset	10^8 - 10^9 rad/s
	Latchup	10^6 - $5x10^9$ rad/s
- Transient (20 ns pulse)	Survival	10^{12} - 10^{13} rad/s
- Long-lived	Total dose	10 - 1000 Krad
	Neutrons	10^{15} n/cm^2
CMOS/BULK SHIFT REGISTERS		
	Temporary upset	10^8 - 10^9 rad/s
	Permanent upset	$5x10^8$ - $5x10^9$ rad/s
- Transient	Latchup	10^8 - $5x10^9$ rad/s
- Long-lived	Survival	10^{12} - 12^{13} rad/s
	Total dose	10 - 1000 rad
CMOS/BULK MEMORIES		
	Temporary upset	10^7 - 10^8 rad/s
- Transient	Permanent upset	8 x 10^7 rad/s
	Latchup	8 x11 rad/s
	Survival	10^{11} rad/s
- Long-lived	Total dose	10 - 1000 Krad
	Neutrons	10^{15} n/cm^2
CMOS/SOS MEMORIES		
	Temporary upset	7 x 10^9 rad/s
- Transient	Permanent upset	10^{11} rad/s
	Latchup	Not possible
	Survival	10^{11} rad/s
- Long-lived	Total dose	6 Mrad
	Neutrons	10^{15} n/cm^2
CMOS/BULK MICROPROCESSORS		
	Permanent upset	10^8 rad/s
	Latchup	10^8 rad/s
	Survival	10^{11} - 10^{12} rad/s
	Total dose	10 Krad
	Neutrons	10^{15} n/cm^2

TABLE 4(1) - SOME UPSET LEVELS FOR CMOS CIRCUITS
(Continued)

	Effect	General range
TTL LOGIC, JUNCTION ISOLATED	Temporary upset Latchup	10^8 - 10^9 rad/s Very limited evidence of existence
- Transient - Long-lived	Survival Total dose Neutrons	10^{12} rad/s 10 Mrad 5×10^{13} n/cm^2
TTL DIELECTRIC-ISOLATED LOGIC	Temporary upset Latchup Survival Total dose Neutrons	10^9 - 10^{10} rad/s Not possible 10^{12} rad/s 10 Mrad 3×10^{14} n/cm^2
I^2L LOGIC	Temporary upset Latchup Survival Total dose Neutrons	2×10^9 rad/s Not possible 10^{12} rad/s 1 Mrad 10^{13} n/cm^2