# SECTION 10. POWER DEVICES

## 10.1. GENERAL

The power subsystems of large space equipment, radiation-generating equipment and nuclear power sources are frequently required to be capable of handling high currents and voltages greater than the kilowatt range.

Additionally, the other subsystems require local regulation by power transistors, thyristors, large rectifiers etc. Silicon power devices of the type described operate on the same general principles as the junction devices discussed earlier, but their construction is often different: the chip is larger and may even be in the form of a "pellet" having the full diameter of the source ingot (say, 30 mm). Epitaxial growth is used more extensively in power devices, while special doping (e.g. neutron transmutation) and unusual geometry are required to achieve a high junction breakdown voltage, low "on" resistance and good heat removal. In general, locally low levels of doping are required for high-voltage devices and, in terms of radiation-effect engineering, this is significant because carrier removal due to particle irradiation will be more noticeable. Also, in order to accommodate large depletion regions, large values of base width are required in the design of power transistors and thyristors. This can impart unusually high sensitivity to gain degradation (see Section "Bipolar Transistors").

In some respects, the power MOS device is also structurally different from its low-power relatives (see, for example, "VMOS" and "HEXFET" construction). Nevertheless, the response of the gate oxide layer - probably the dominant effect in space and gamma rays - can still be predicted by the methods described earlier.

## 10.2. BIPOLAR POWER TRANSISTORS

The degradation of gain in transistors under particle irradiation has been discussed earlier and details of commercial power transistors were given. It can be seen that unless these devices are carefully selected, neutron-induced damage becomes serious below a fluence value of $10^{12}$ n. $cm^{-2}$ (1 MeV). To understand the generally high radiation sensitivity of power devices, it is necessary to outline the theory of transistor breakdown and its influence on base width. The avalanche breakdown voltage of the collector-base junction of a silicon transistor, $BV_{CBO}$, is highest when the collector region is very lightly doped. To a first approximation:

$$BV_{CBO} = \frac{2 \times 10^{17}}{N_{coll}} \qquad \text{.....10(i)}$$

where $N_{Coll}$ is the doping concentration in units per $cm^3$ in the collector region. Thus, for a breakdown voltage greater than 100V, a doping level of less than $2.5 \times 10^{15}$ $cm^{-3}$ is necessary. This is equivalent to a resistivity higher than 2 ohm. cm.

Now, the practical limit of collector-to-emitter voltage in transistor operation is, in fact, lower than this value. The reason is that two collective effects occur in the npn or pnp structures, the "punch-through" and the "open-base" effect. At high collector-base voltages, the depletion region of the collector-base junction extends completely through the base region. If this occurs, the collector-emitter voltage is, in a sense, "shorted" because the p-type base region, once depleted, no longer rectifies. A large current, $I_{CE}$, flows between emitter and collector. This punch-through conduction is at its highest when the base contact is "open". The base region is then floating (i.e. capable of taking up the potentials due solely to $I_{CE}$) and the net result is that $I_{CE}$ (in this case termed $I_{CEO}$) is increased further by the amplifying action of the npn structure. As a result, the "breakdown value of $V_{CE}$ with base open" ($BV_{CEO}$) is lower than $BV_{CBO}$ with a ratio:

$$\frac{BV_{CBO}}{BV_{CEO}} = (h_{FE}), \qquad \text{.....10(ii)}$$

where $h_{FE}$ = is the forward gain of the transistor.

To achieve a high value of $V_{CE}$ before punch-through occurs, a wide base is required. Other factors being equal:

$$BV_{PT} \propto W_B \qquad \text{.....10(iii)}$$

where $BV_{PT}$ is the punch-through value of $V_{CE}$ and $W_B$ is the base-width.

The above rationale leads to the conclusion that, for the design of high-voltage power transistors (devices in which the value of the rated $V_{CEO}$ is high), we require two physical features which lead to high sensitivity to neutron irradiation, namely:

(a) a low doping level for the collector and
(b) a high base width.

Additionally, and in accordance with equation 10 (ii), the initial value of $h_{FE}$ must be kept intentionally as low as possible. Thus, only a small "margin" for neutron-induced degradation will exist. Typical values for the rated parameters of a power transistor are:

| Device type | $V_{CEO}$ (max) (V) | $h_{FE}$ (max) ($I_C/I_b$) | $f_T$ (min) (MHz) | Power (max) (W) | Process specification |
|---|---|---|---|---|---|
| 1 | 400 | 40 | 50 | 10 | P 48 |
| 2 | 100 | 120 | 2 | 120 | P 4A |

To give an example of particle effects at neutron fluences of 2 x $10^{12}$ and 7 x $10^{11}$ $cm^{-2}$, a transistor of type 1 would lose respectively about 50 and 10% of its gain, while a specimen of type 2 would lose respectively 99 and 90%. This illustrates how voltage and power specifications alter the "hardness" obtainable from bipolar power transistors.

Despite the large junction areas, it is unlikely that transient, ionisation-induced leakage currents will be of any importance at the expected dose rates in space. A typical response to ionising dose rate is 5 x $10^{-9}$ A.rad.s. Similarly, at the high values of "drive" used, the impact of surface effects on gain and leakage (which are induced by ionisation and are important for low-power transistors - see earlier) is unlikely to add significantly to the large particle effects described above.

In the USA, radiation-hardened power transistors have been developed. Epitaxial collector regions are carefully adjusted for doping level and minimum acceptable widths (to minimise change in $V_{CE}(SAT)$ ) and base regions are adjusted to the minimum acceptable width (to minimise gain degradation). An example of the data for some advanced power transistors capable of operating reasonably well after a neutron fluence of $10^{14}$ $n.cm^{-2}$ has been given earlier. Ferranti have performed comparative neutron tests in the $10^{-12}$ to $10^{13}$ $n.cm^{-2}$ range on single diffused and planar-epitaxial power transistors.

## 10.3. THYRISTORS (previously known as silicon controlled rectifiers)

To perform triggering functions, the 4-layer thyristor structure requires high values of gain in the overlapping npn and pnp structures of which it is composed. Similar arguments indicate the need for:

- high base widths and resistivity values, as described for power transistors,
- a high doping uniformity to avoid the local triggering which is often induced if local regions of low resistivity are present,
- low minority carrier lifetime values in certain junction regions to avoid charge storage effects which induce slow turn-off.

Optically triggered thyristors are becoming widely used.

In these devices, one should anticipate some severe radiation-induced effects, arising in both the optical and the semiconductor media. For reactor neutron fluences higher than $10^{12}$ n.cm$^{-2}$ (1 MeV), it has been shown (SPIRE, 1980) that the characteristics of switching may change radically in existing commercial thyristors. The gate current at the triggering point may increase over 10 times and also the "holding current", while the forward voltage drop in the "on" condition may double owing to resistivity effects. Boswell and Widdows (1976) also found that, for certain commercial thyristor types, triggering parameters degrade suddenly as the neutron dose is increased. Few problems appear until a fluence of 2 x $10^{12}$ has been passed but, thereafter, parameters change at a rate more than linear.

## 10.4. POWER MOS FETs

### 10.4.1. Introduction

While MOS transistors for logic switching are being reduced to outline dimensions smaller than 10 µm on a side for VLSI chip technology, MOS transistors for power control are being enlarged to sizes up to 10 mm on a side. However, the power MOS transistor actually comprises many thousands of vertical MOS structures connected in parallel (typically, over 50,000). Hence, the technology bears some resemblance to that of integrated circuits. The gate oxide technology is similar to MOS integrated circuits and, hence, the same rules as for radiation hardness apply. Although some research efforts have been made to achieve radiation hardening (Roper and Lowis, 1985), no hardened MOS power devices are available commercially at the time of writing (1986).

### 10.4.2. Parameter changes under irradiation

The response of power MOS devices to radiation is mainly characterised by:

1. Threshold voltage shift,
2. Transconductance degradation and
3. Reduction in breakdown voltage.

(a) Threshold voltage shift.
As for other MOS devices, the shift of threshold voltage, $V_T$, is negative and shows a significant bias dependence (Seehra and Sluzark, 1982; Adams and Minnee, 1982). The following are typical test data of an 100V, 40 A, n-channel commercial MOS power transistor:

| Bias during irradiation ($V_I$) | Failure dose (Krads) |
|---|---|
| +10V d.c. | 25 |
| +10V to 0V (switched, 50% cycle) | 30 |
| -10V d.c. | 25 |
| +5V d.c. | 30 |
| -5V d.c. | 45 |
| 0V | 100 |

(b) Transconductance degradation.
This occurs as a result of mobility reduction due to interface state generation. However, significant changes in transconductance occur only at comparatively high doses - above 1 Mrad (Roper and Lowis, 1983).

(c) Reduction in breakdown voltage (BV).
Drain-source breakdown voltage ($BV_{DS}$) shows significant reduction as a function of total dose. The mechanism is believed to be charge trapping in the field oxide and generation of interface traps at the field oxide/silicon interface (Blackburn et al, 1983). The trapped charges alter the potential at the surface of drain and source junctions and hence become part of the junction termination and influence the breakdown voltage. The reduction of breakdown voltage is a strong function of the drain-source voltage applied during irradiation.

Typical changes in BV, noted during irradiation of a 500V n-channel device, are -40V at 1 Mrad for zero bias and -140V at 50 Krads for 300V bias. The behaviour at high drain-source voltages (>200V) during irradiation shows a sharp decrease in BV at low voltages and then an increase at about 150 Krads, followed by a small, gradual decrease. This implies that, in the rather low total dose environment of space, the reduction in breakdown voltage may be significant and must be considered in conjunction with normal derating requirements.

### 10.4.3. Radiation-tolerant power MOS circuits

Scope exists for radiation tolerance to be introduced as part of the circuit-design procedure when power MOS is used. In view of the earlier discussion of $V_T$ and $BV_{DS}$ bias dependence, it is clear that circuit designs should minimise both the magnitude and the

application time of bias voltages. For example, "overdrive" (i.e. the use of a negative gate voltage to turn off an n-channel transistor) should be applied with caution because the enhanced radiation sensitivity resulting from the use of gate bias may dominate (Adams and Minnee, 1983). Inverter circuits should be tested as complete circuits as it is found that a combination of dynamic switching and self-heating of transistors leads to a higher tolerance to radiation than simple assessments would indicate.

## 10.5. CONCLUSIONS

Of the many classes of semiconductor devices used in space equipment and other lightweight electronics, silicon power devices are among those few whose high sensitivity to damage from specific particles must be given major consideration. Calculations given in earlier chapters show that because of the high base-width values of such devices, electron and neutron fluences as low as $10^{14}$ and $10^{11}$ $cm^{-2}$ respectively may cause significant degradation in bipolar junction devices. The behaviour of the power MOS device resembles that of its corresponding smaller relation, the MOS switching device.

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