8th esa round table on micro and nano technologies – 2012, Oct 15-18 Noordwijk

Failure avoidance during component development by advanced simulation together with experiment based reliability assessment

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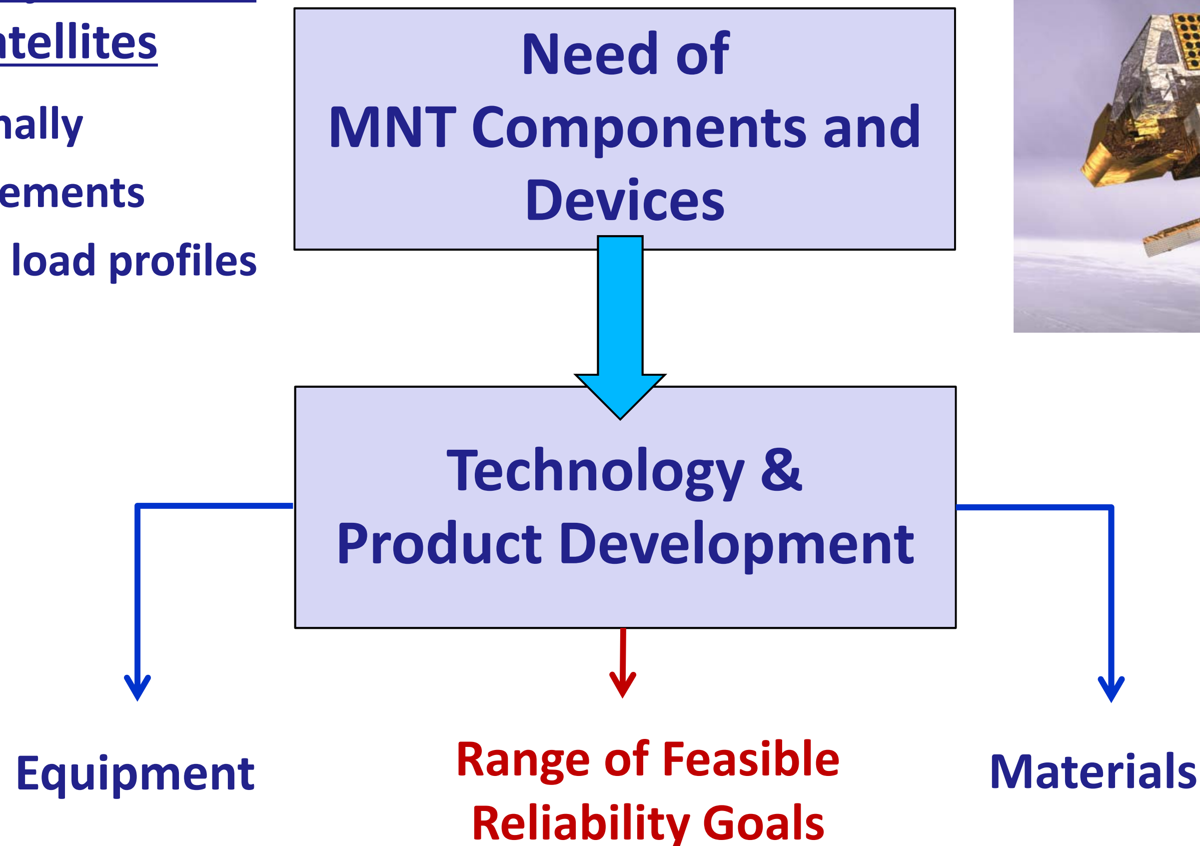
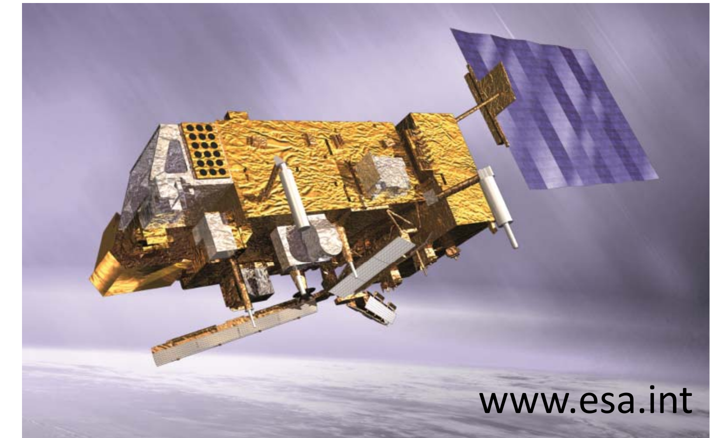
Decision Making on Reliability

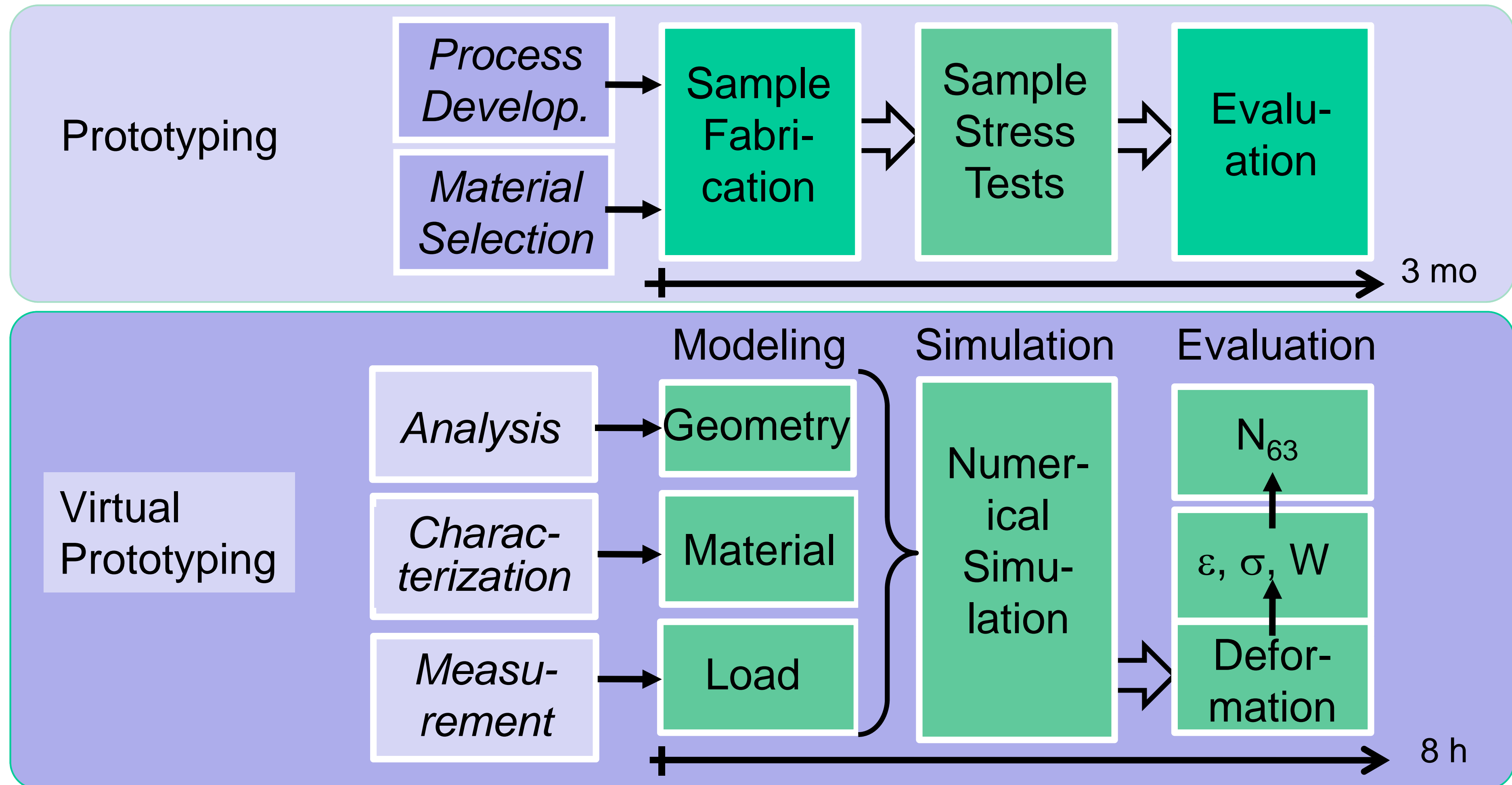
<u>New mission objectives & and types of satellites</u>

- device functionally
- payload requirements
- environmental load profiles
- ……





Taking Advantage of Virtual Prototyping



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Example of Design Optimization for Reliability Needs

-Low Loss Beam-Forming Networks for Satellite Broad-Band Communication -

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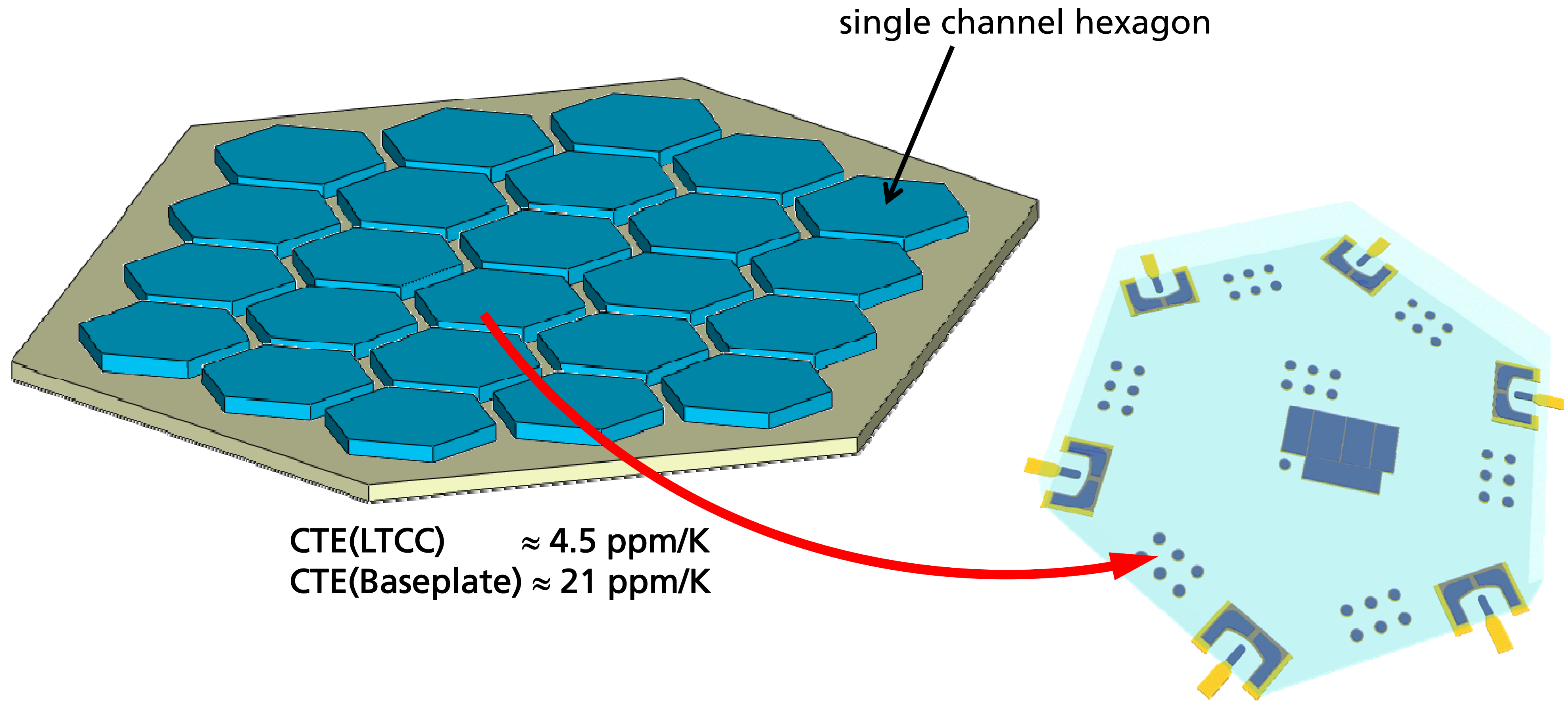
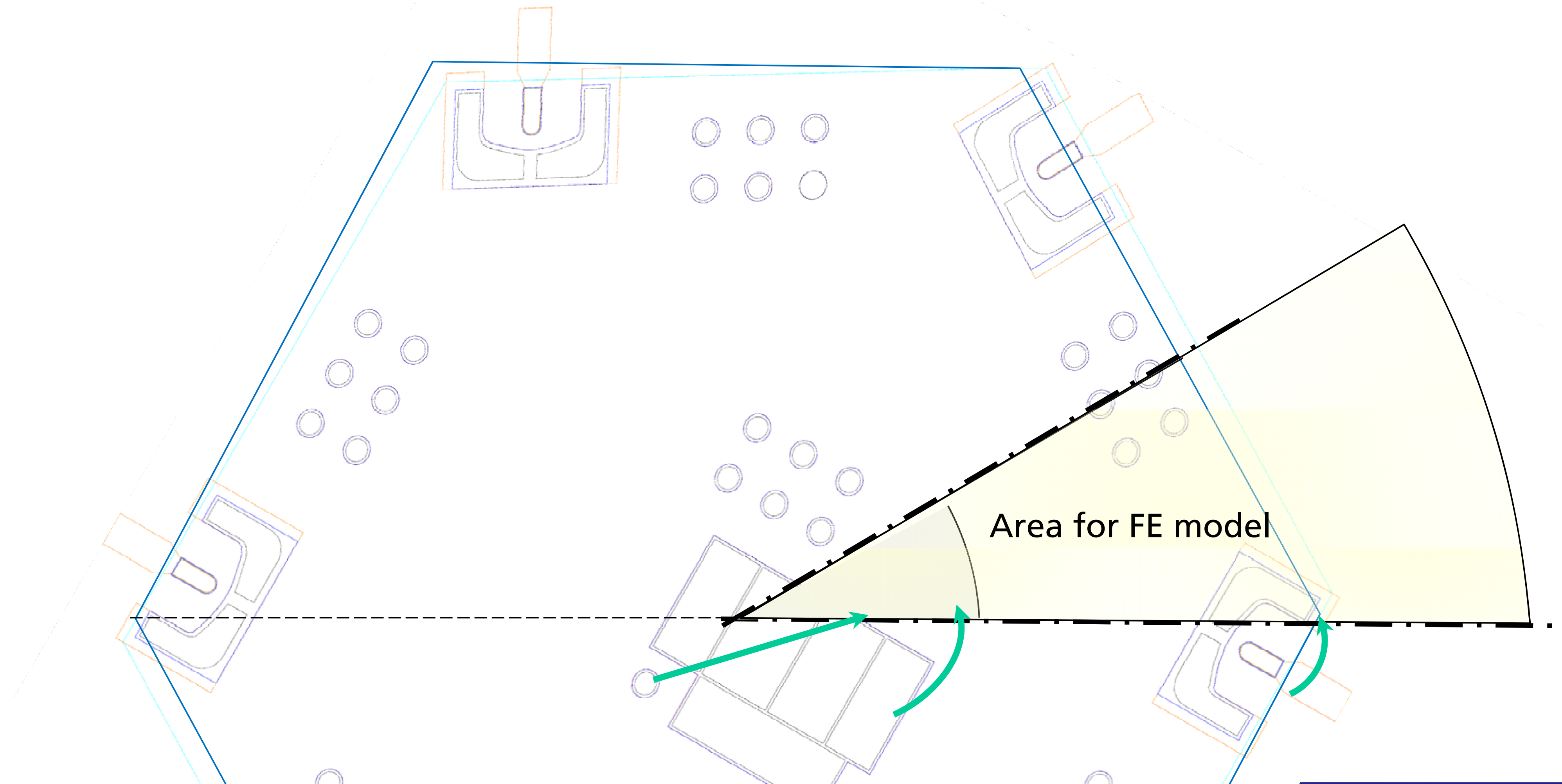
Solder Interconnection between Honeycombs and Base Plate

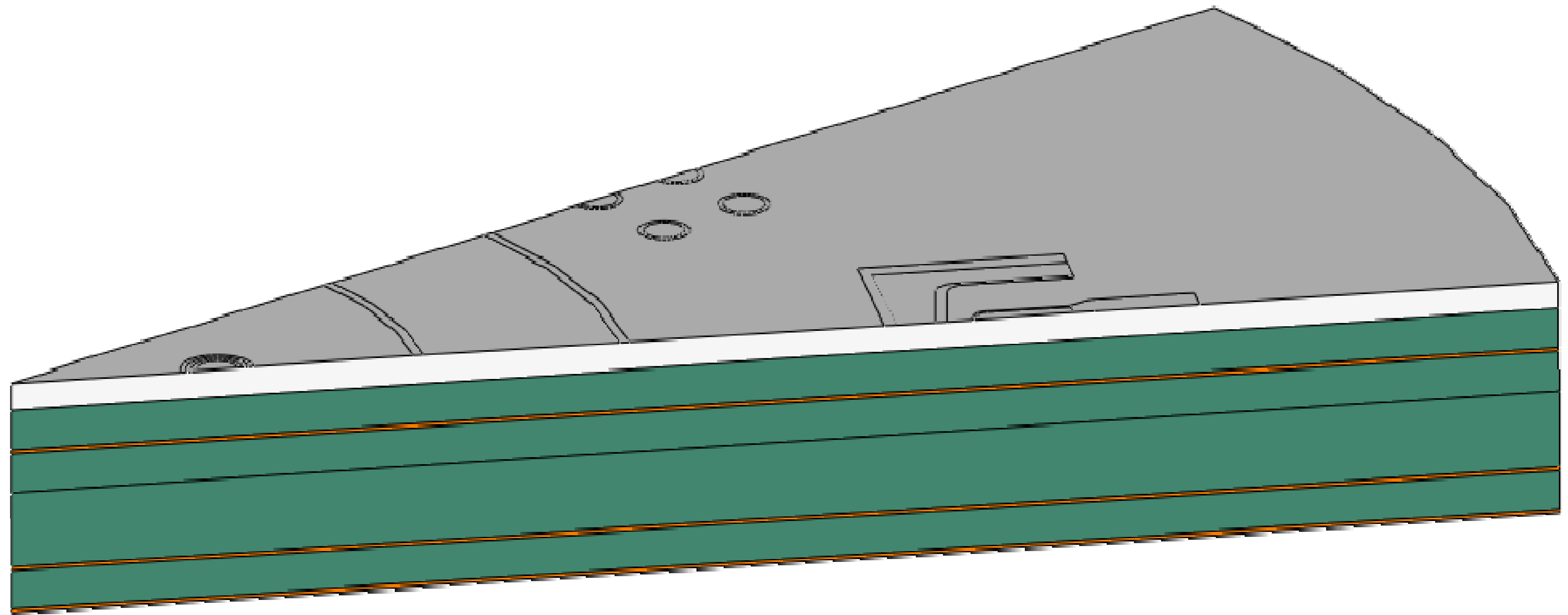


- Solder interconnects between LTCC honeycomb and base plate (dark blue areas)
- Challange: Manage the CTE mismatch reliably

Slight Simplifications Allow 1/12 FE Model



Geometry and Materials, FE Modell "inter-2"



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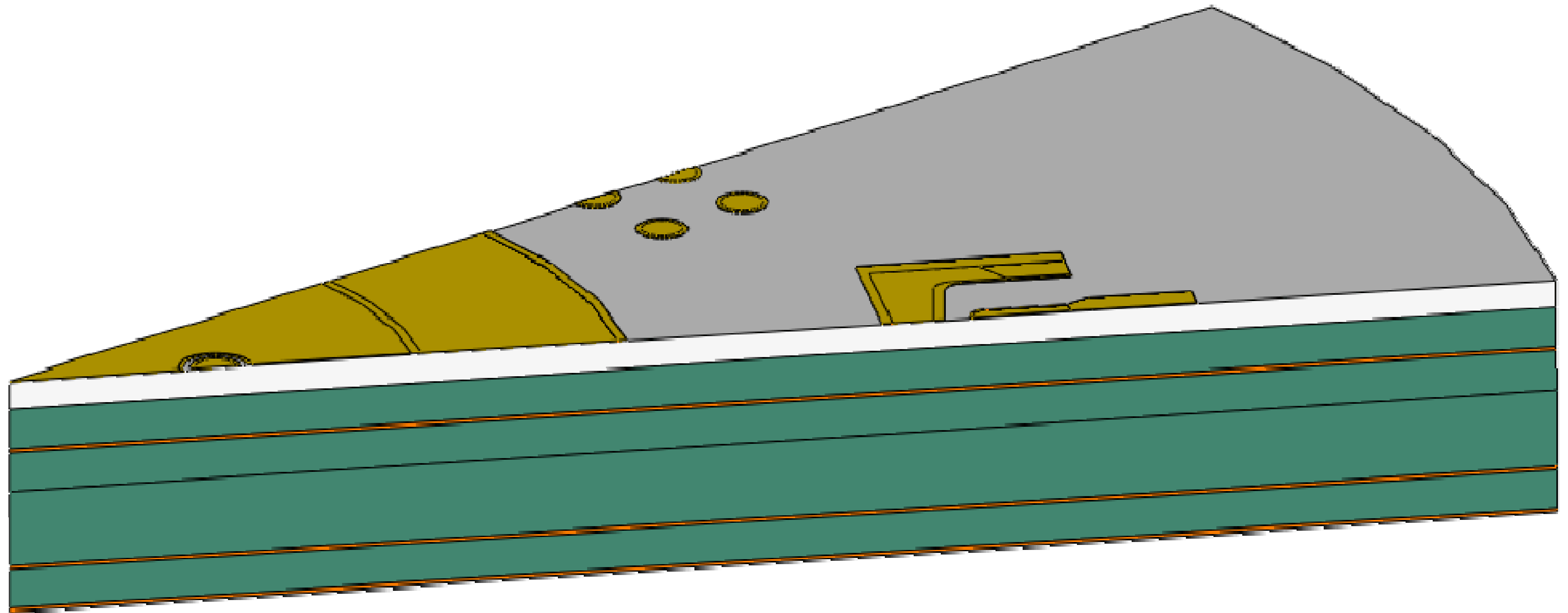

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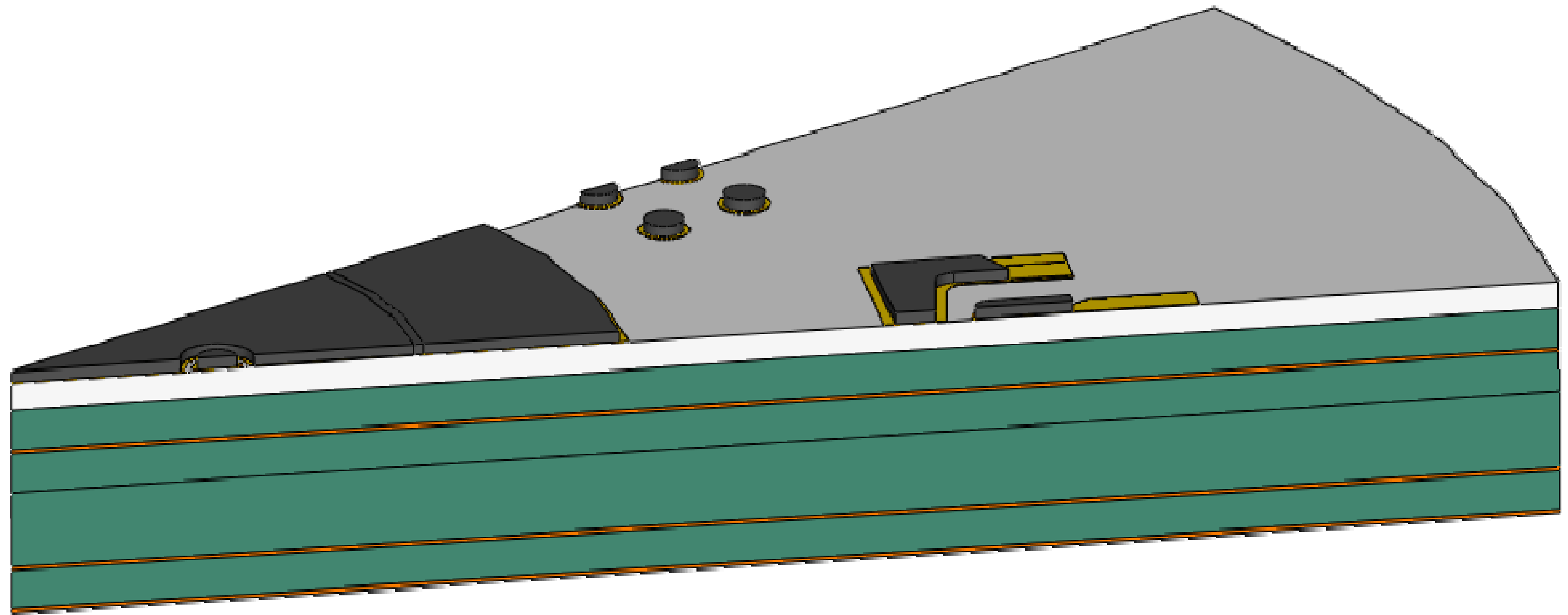
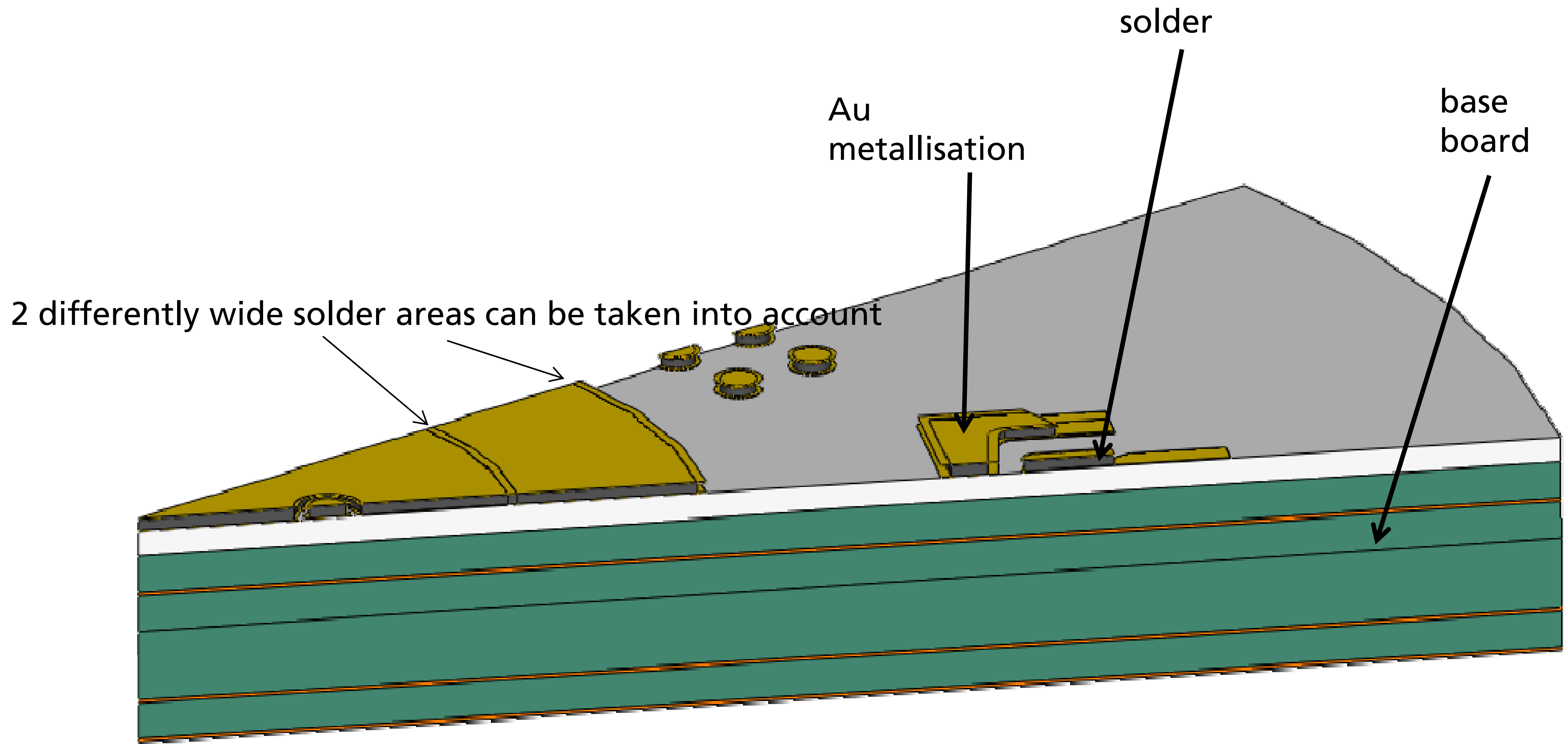
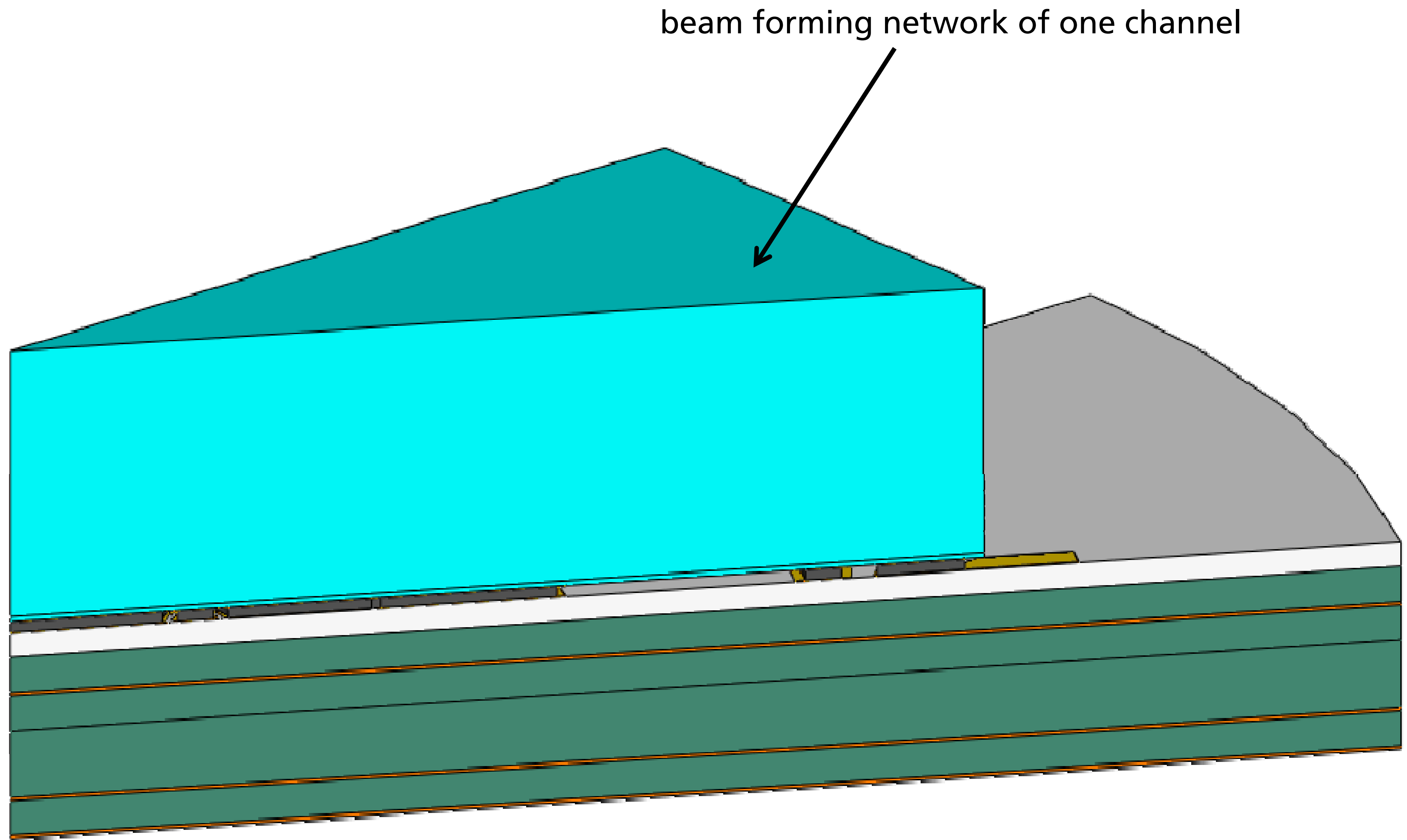


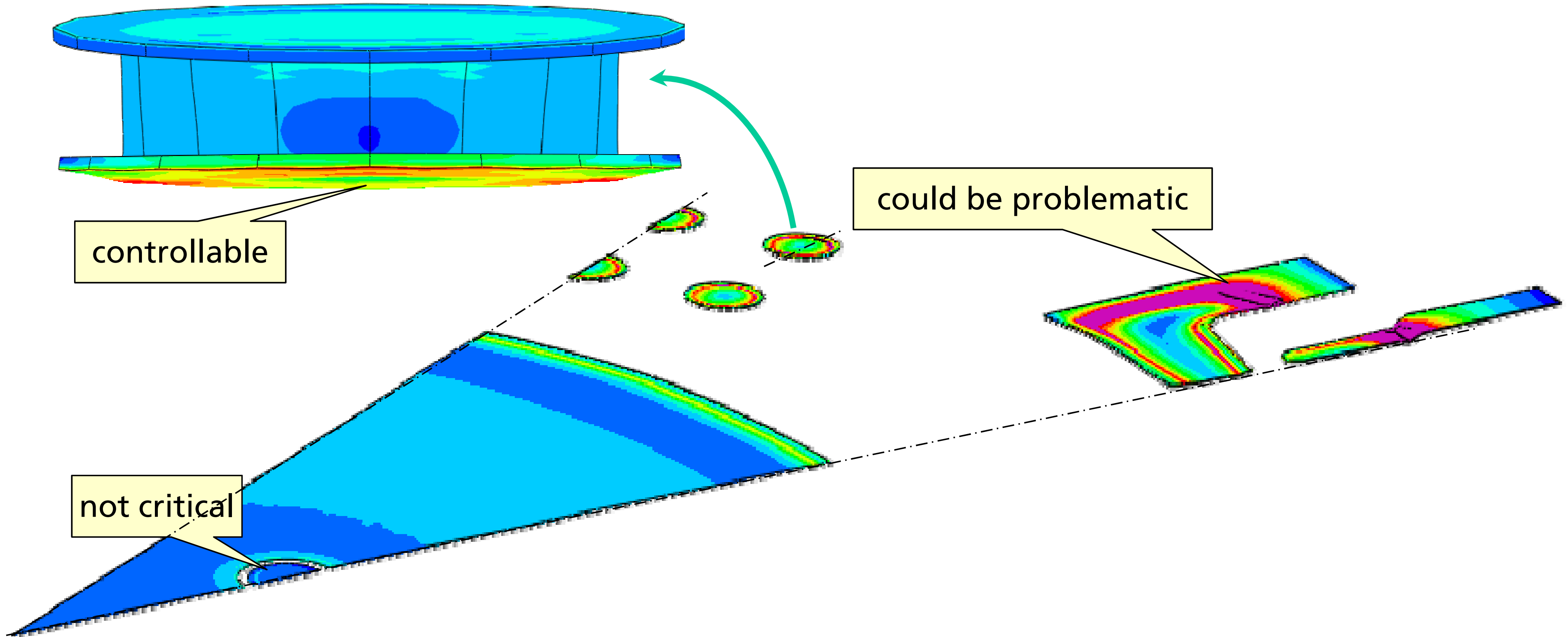
Geometry and Materials, FE Modell "inter-2"



Geometry and Materials, FE Modell "inter-2"



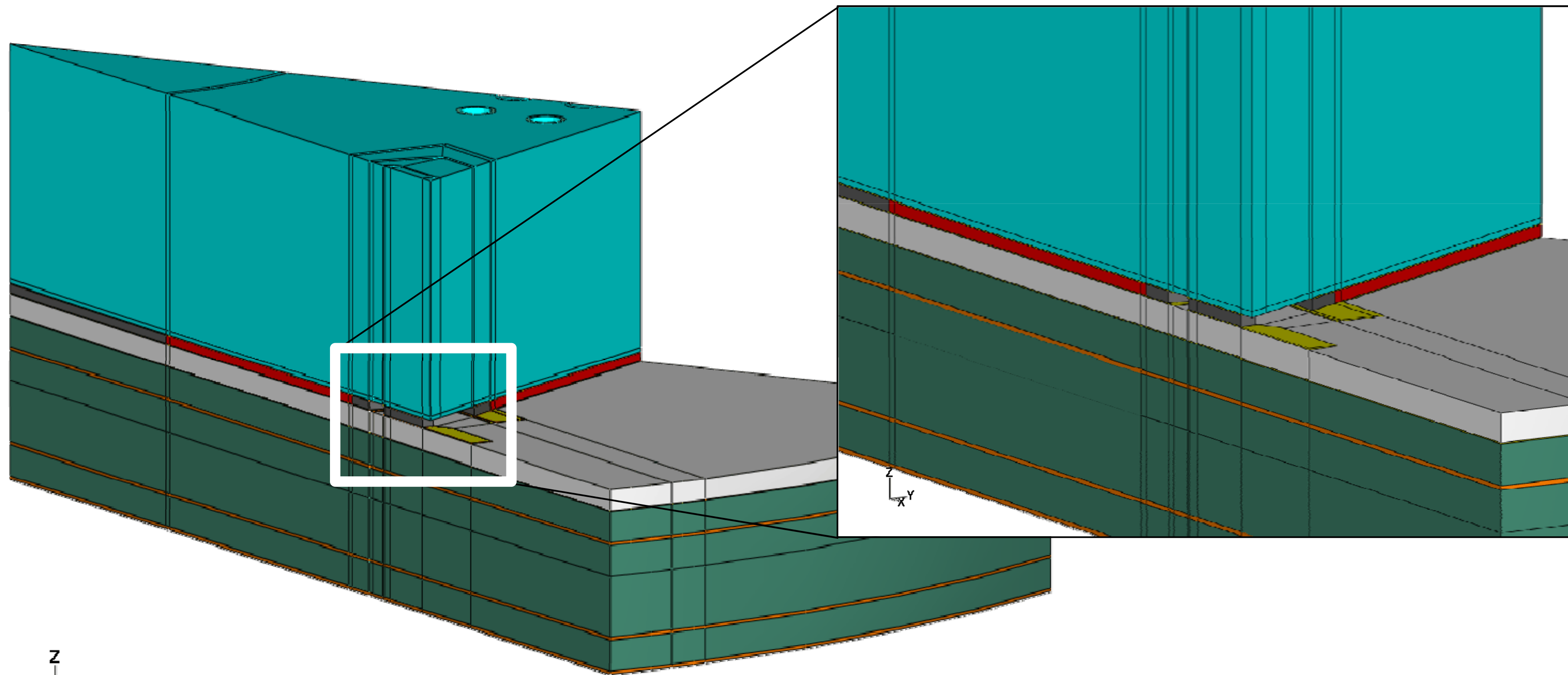
Stress Analysis (Mises): Base Plate Top Metallisation



- Au metallisation is most stressed at the interconnects to the neighbouring honeycombs
- Solution: Underfilling

(Deformation 20 x)

Investigate the Effect of Underfilling



- Underfill (red material region) = particle-filled epoxy
- Distributes forces across the solder gap
- Stress relief at interconnects
- RF contacts are not to be wetted

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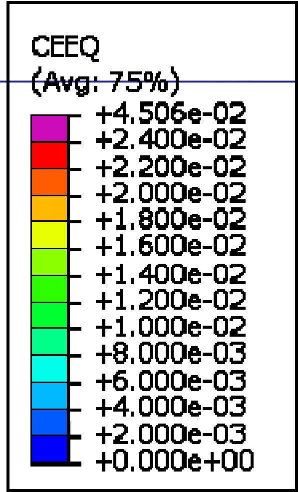

1/12 model before underfilling, cummulated creep strain due to thermal cycles

+ closed gap: no wetting on RF structures

without underfilling

underfilling applied, same scaling!

1/12 model after underfilling, cummulated creep strain due to thermal cycles

Advanced Approaches of Finite Element Analyses

- Failure avoidance in semiconductor BEoL stacks -

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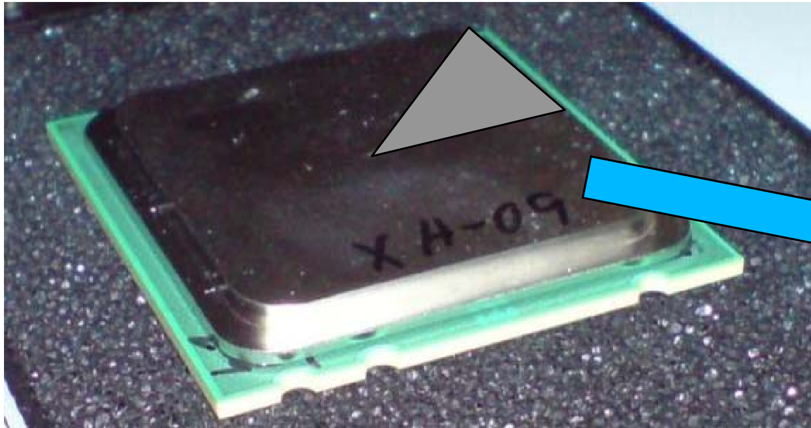
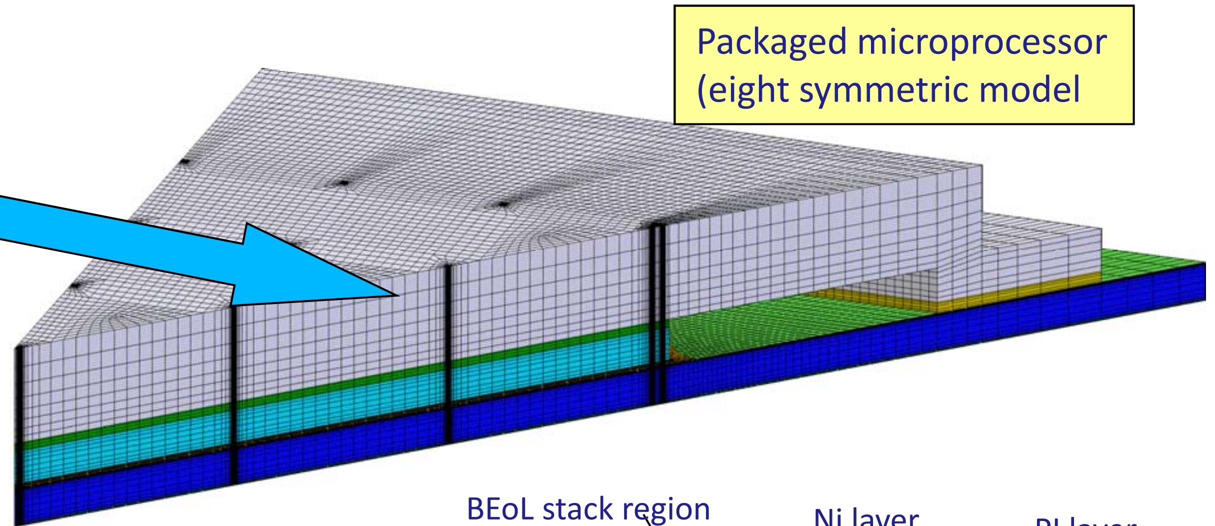
Multiscale Modeling

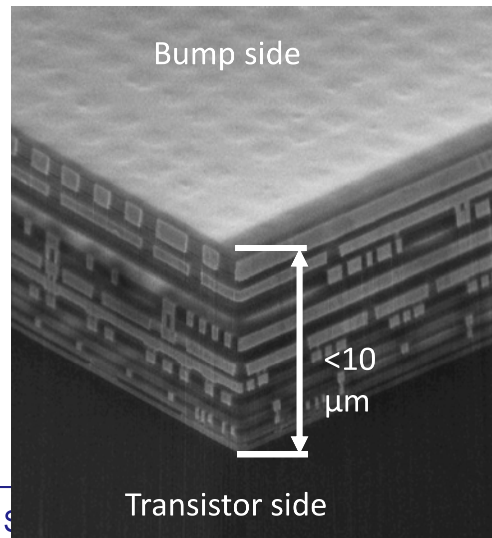
Geometry



Packaged microprocessor
(10 – 40 mm size)

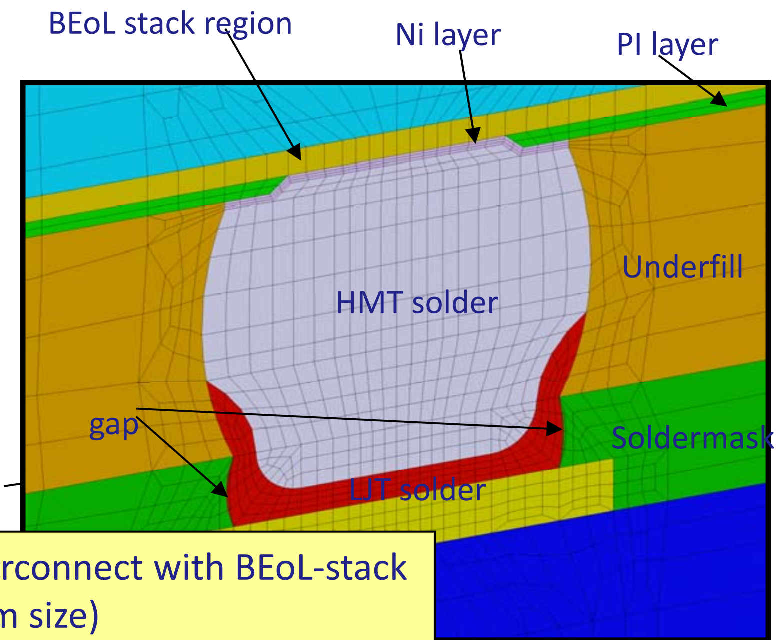


Packaged microprocessor
(eight symmetric model



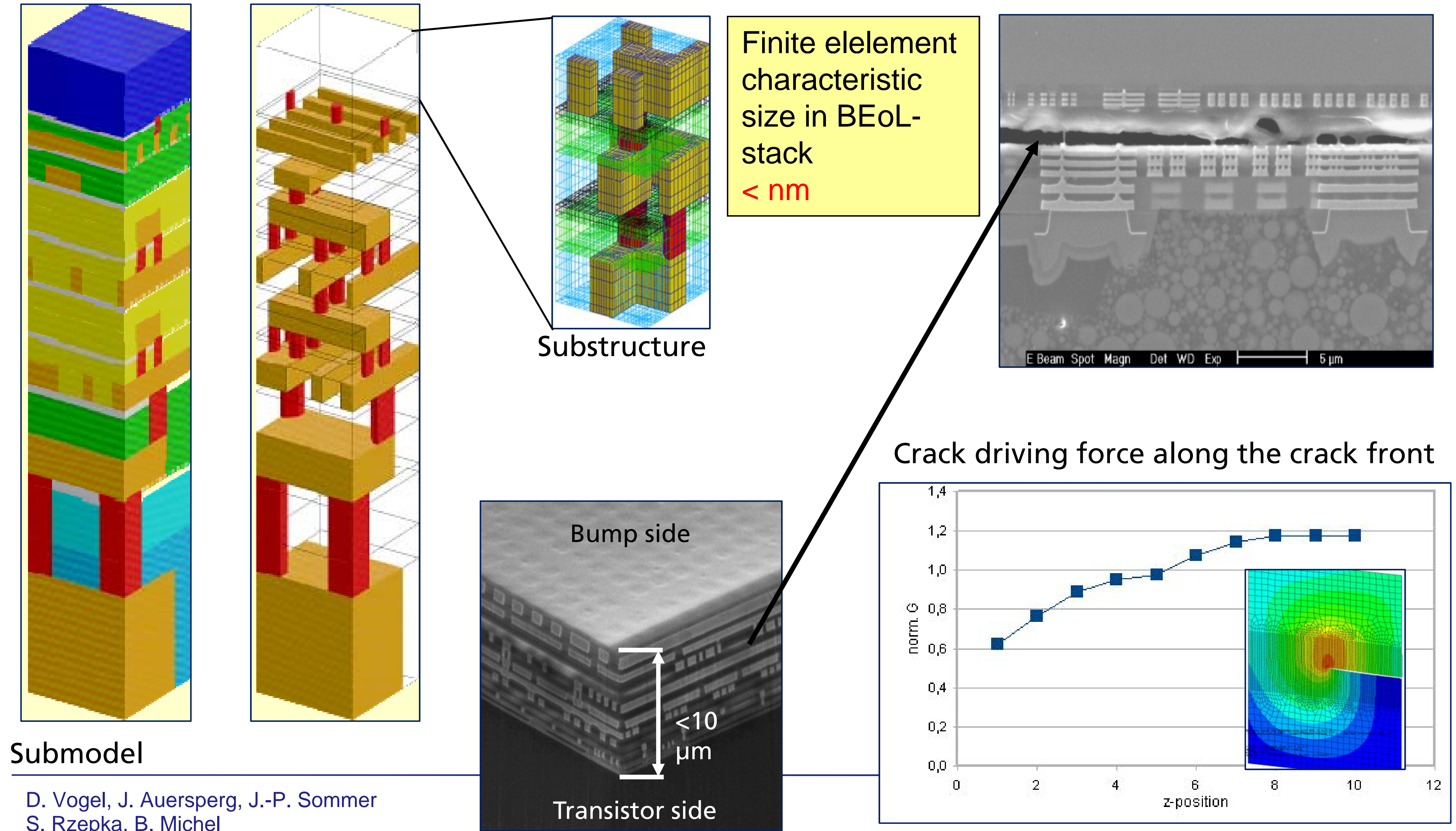
BEoL-stack
(5 – 10 µm size)

Feature sizes:
some nm!



Solder interconnect with BEoL-stack
(50 – 80 µm size)

3D BEoL Stack FEA – Simulation of the Cracking/Delamination Behavior



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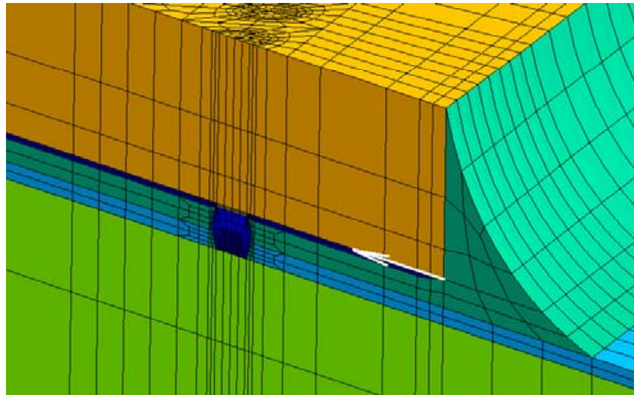
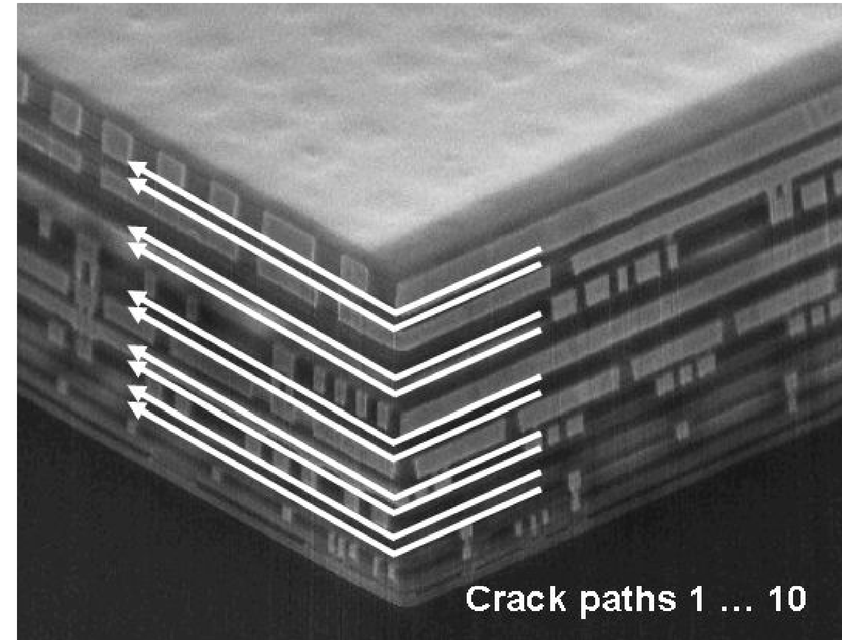
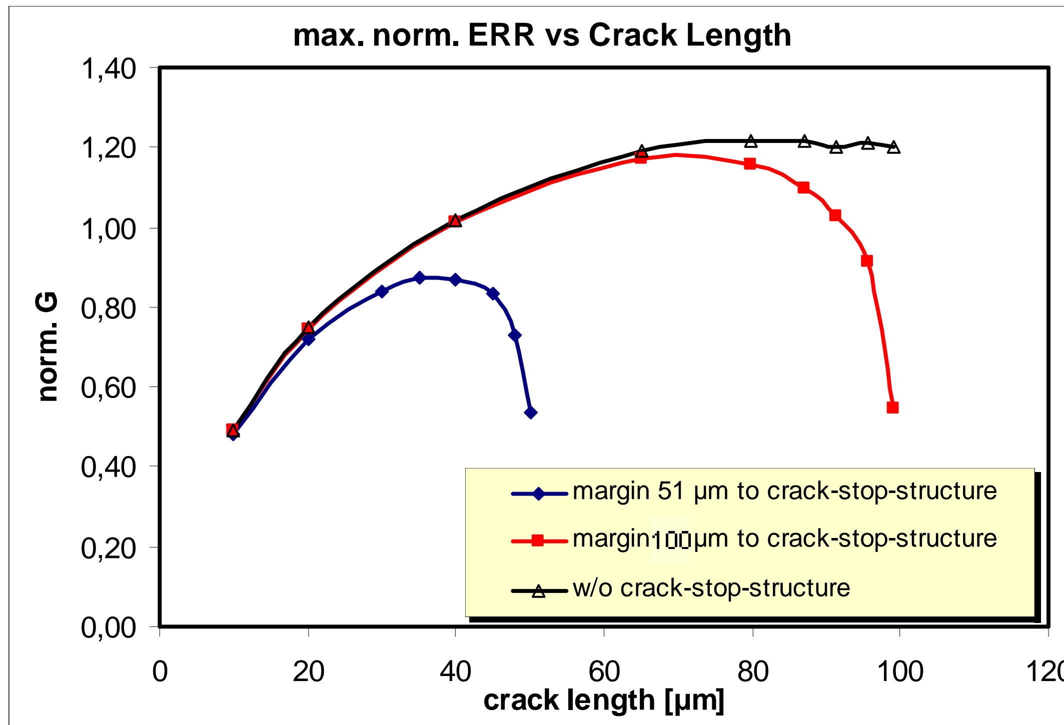
Multi-level FE-modeling approach

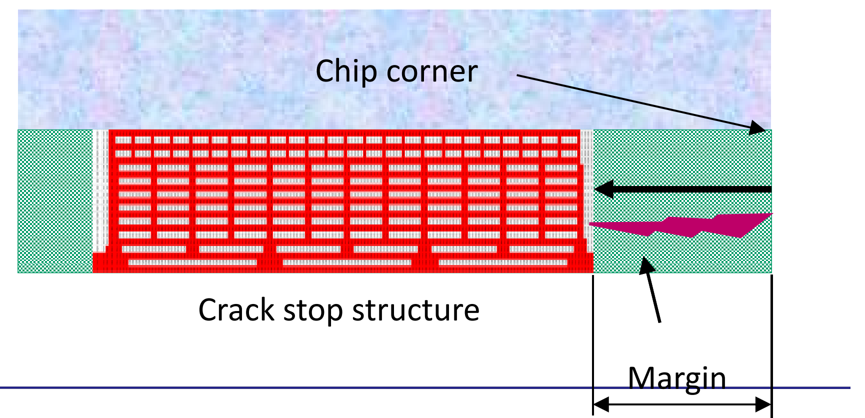
BEoL Stack of an IC – Die Edge Cracking - Interface Fracture Mechanics

CPI



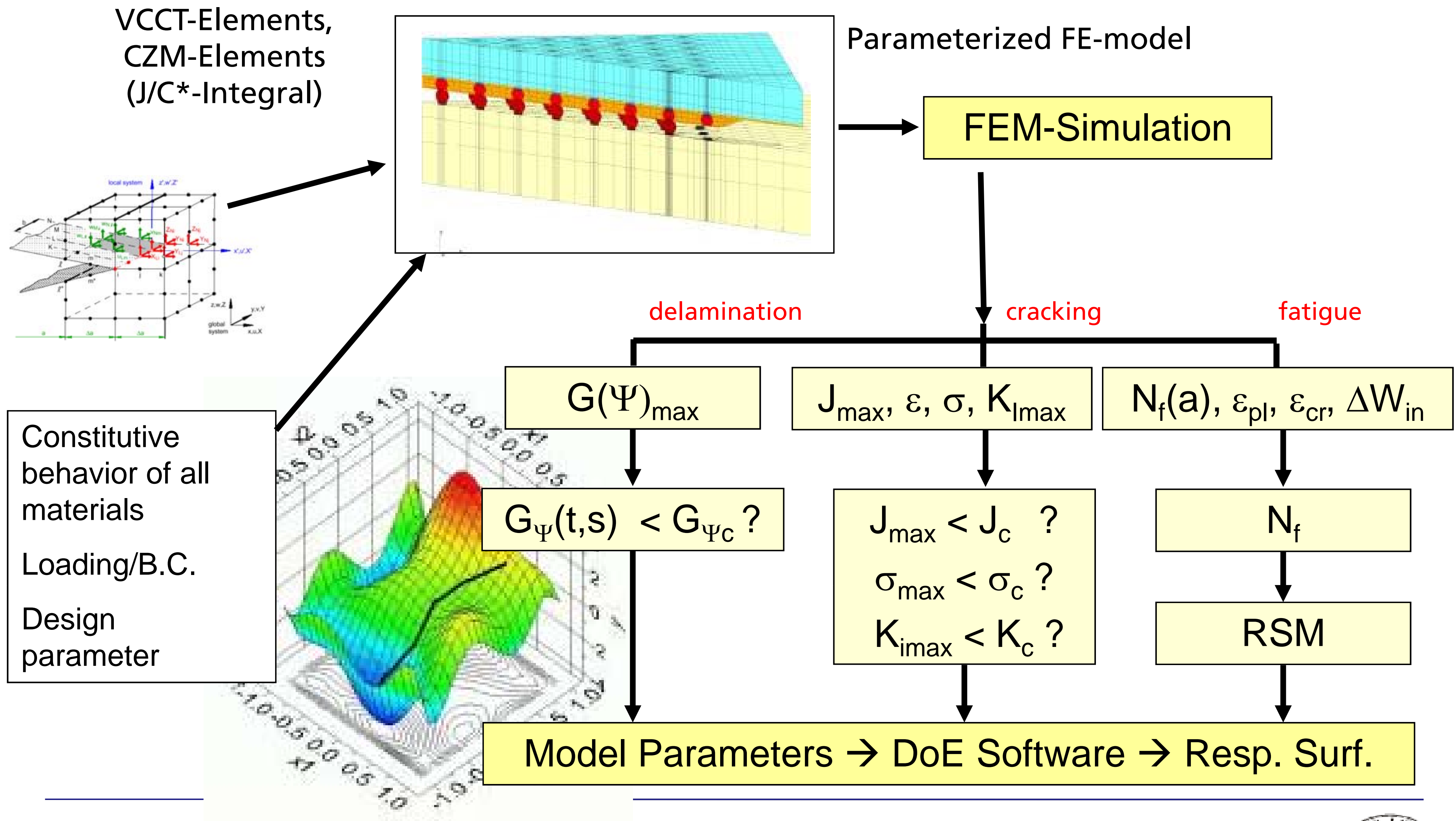






Bi-material interface fracture mechanics approach

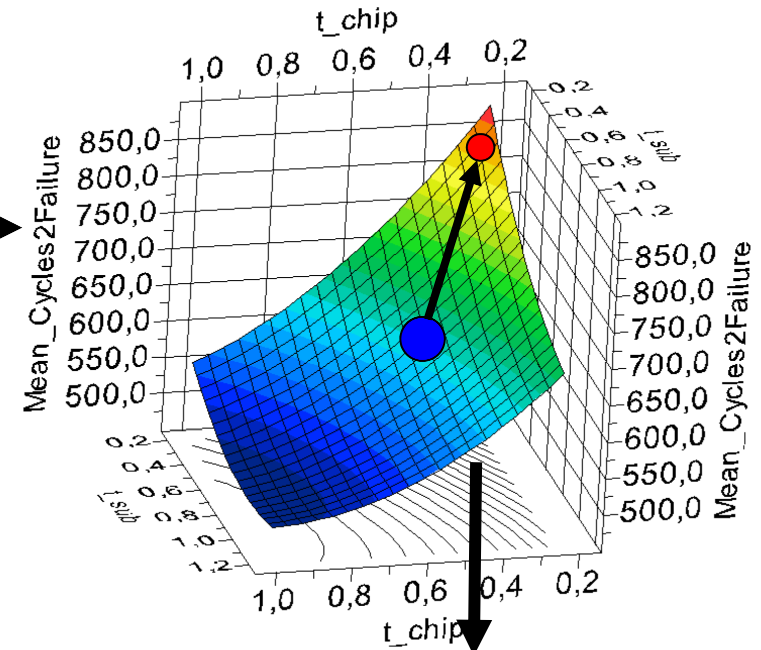
Solder Fatigue, Bulk Fracture, Interface Fracture – RSM/DoE

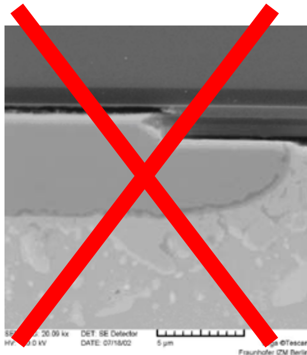


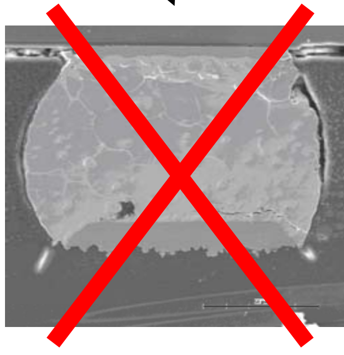
Optimization based on a DoE-Model or direct FEA – Define the Goal

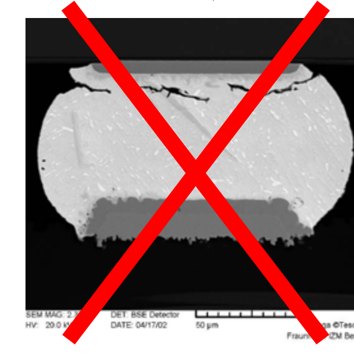
Single Goal of Optimization:

- Find the best pair of chip/substrate thicknesses for lowest solder fatigue
- Avoid delamination and chip cracking at the same time.









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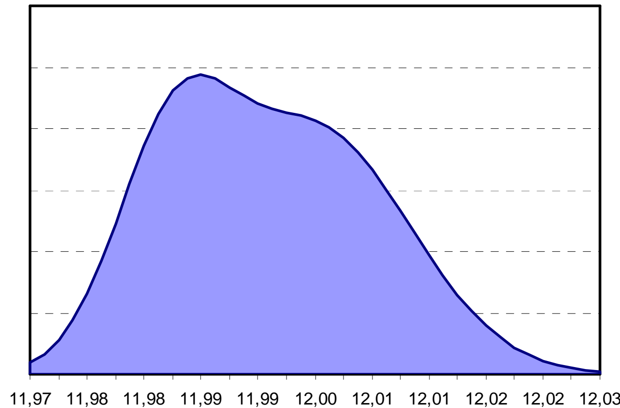
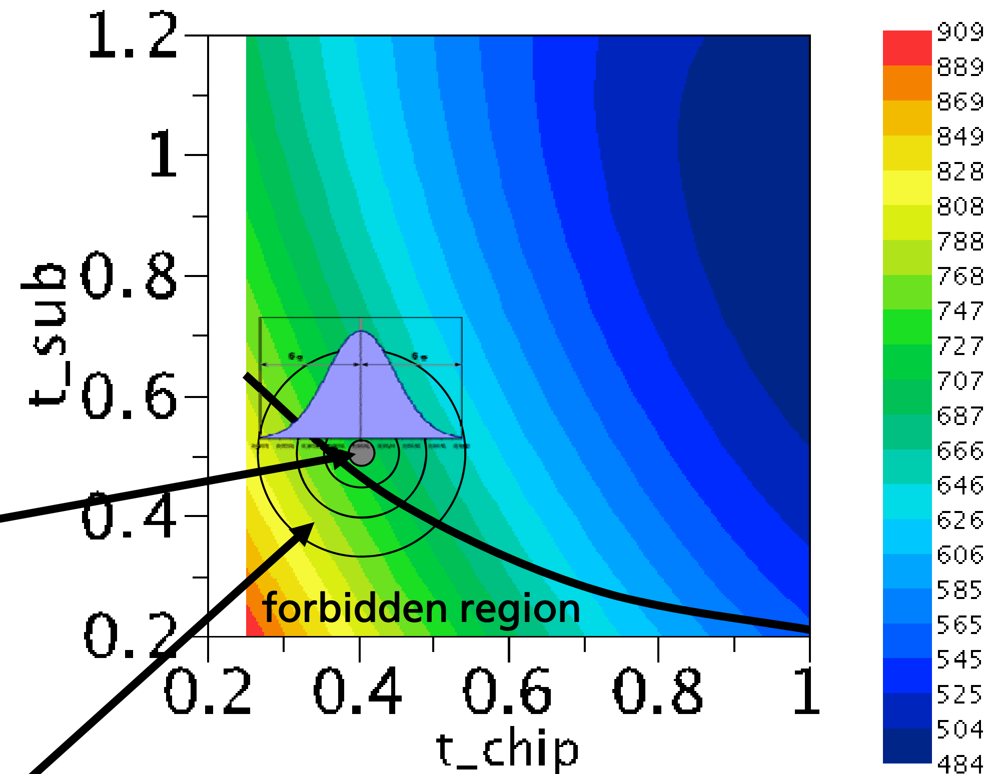
Robustness and Design for Six Sigma

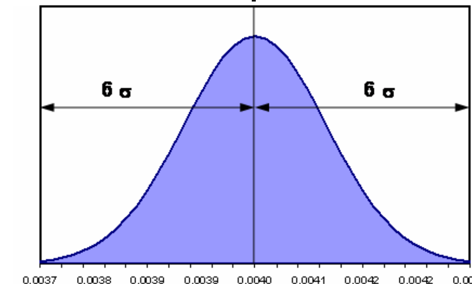
Scattering results





Optimum for a deterministic model resides often in a region near or directly at a boundary of a forbidden region (fracture toughness exceeded, for instance).

Some of the potential solutions reside in the forbidden region and will probably lead to failure.



Scattering model parameters

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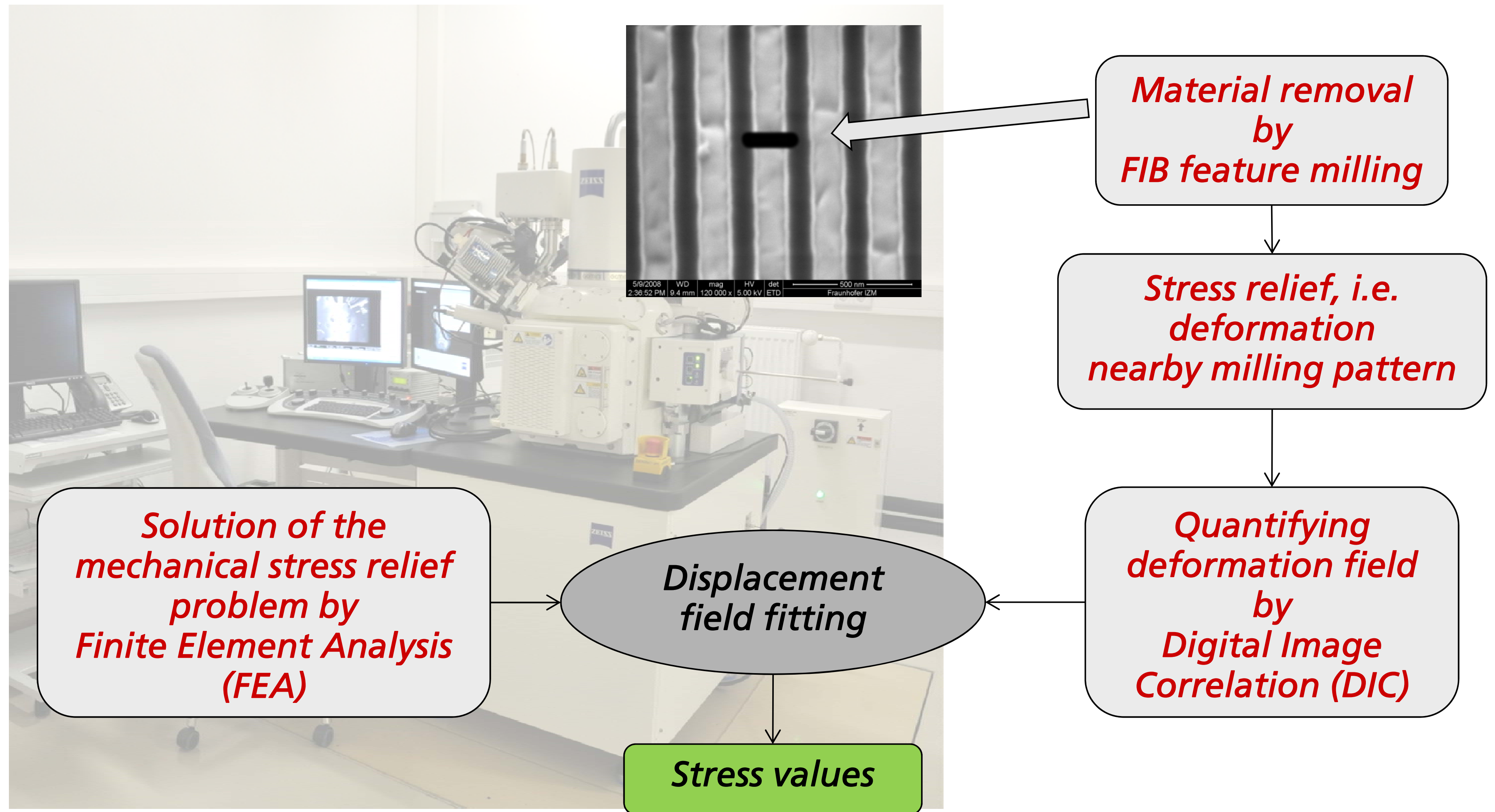
Local Mechanical Stresses – Initiator of Failure

- residual stress due to processing
- stress caused by operation of devices
- environmental stresses

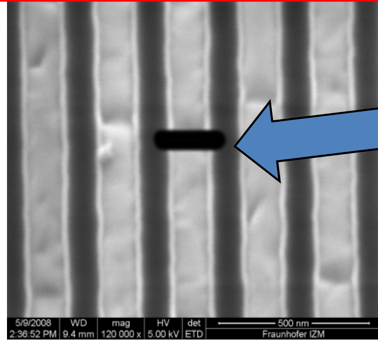
- Advanced stress measurement techniques
with extreme spatial resolution -

Local stress measurement concept – stress relief by FIB milling (fibDAC)



Local stress measurement concept – stress relief by FIB milling (fibDAC)

Object with residual stresses



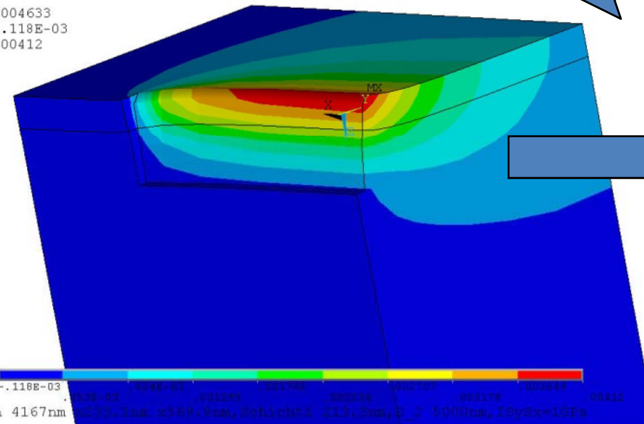
Local stress relief by ion milling

Pt (deposited after measurement for contrast purposes)

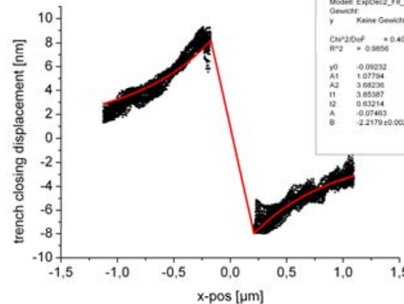
Si3N4

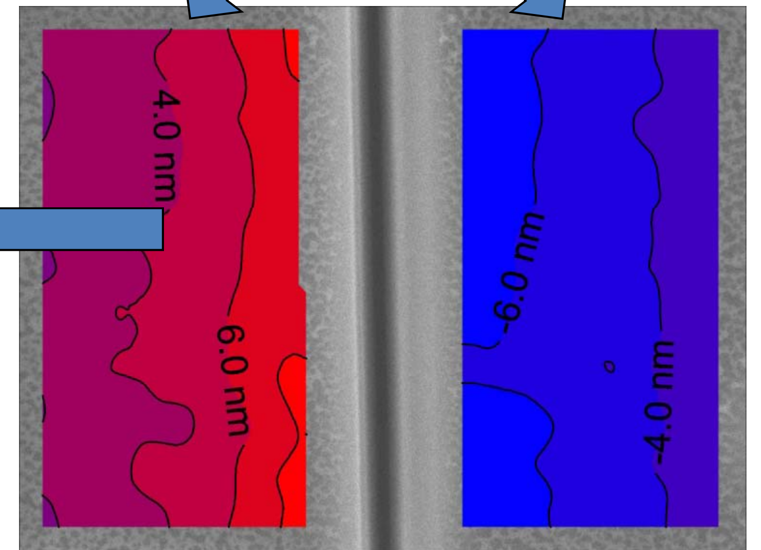
Displacement field by DIC

Expected displacement vs. stress



Mutual matching to determine stress

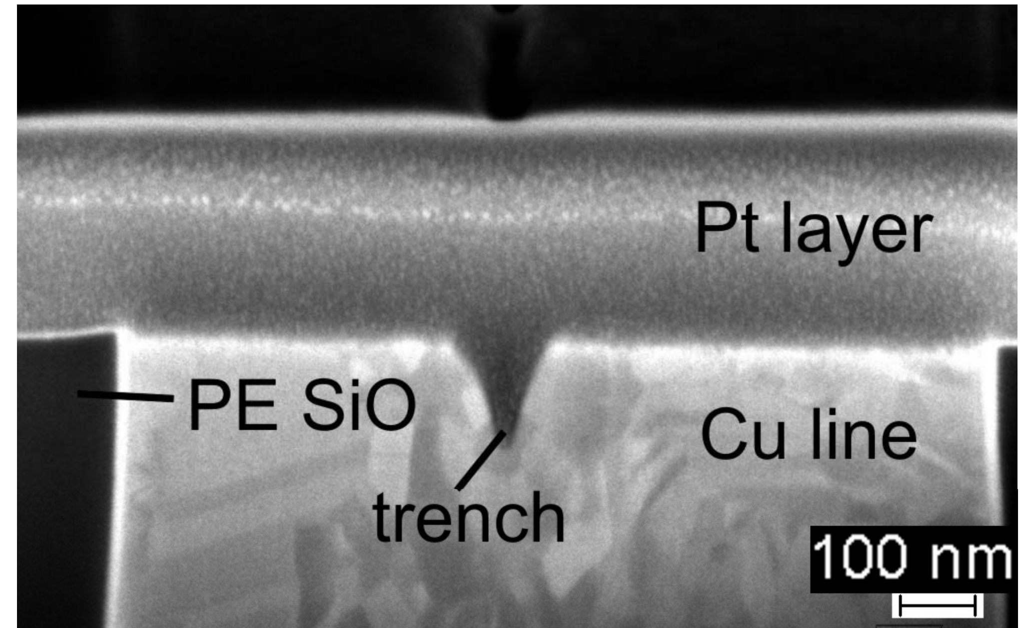


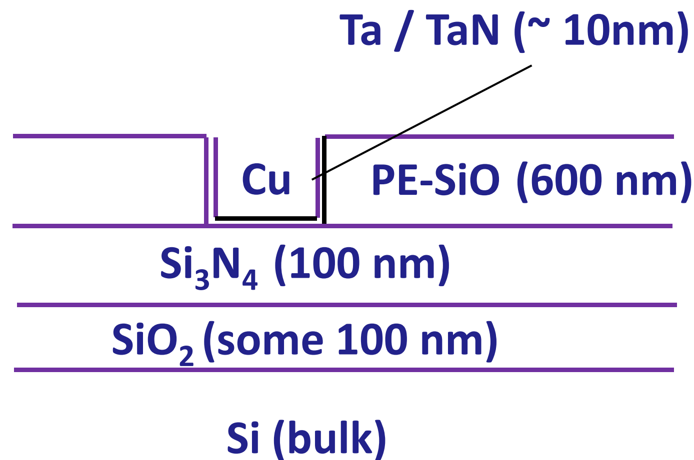


Extreme lateral resolution by fibDAC stress measurement

Research goals

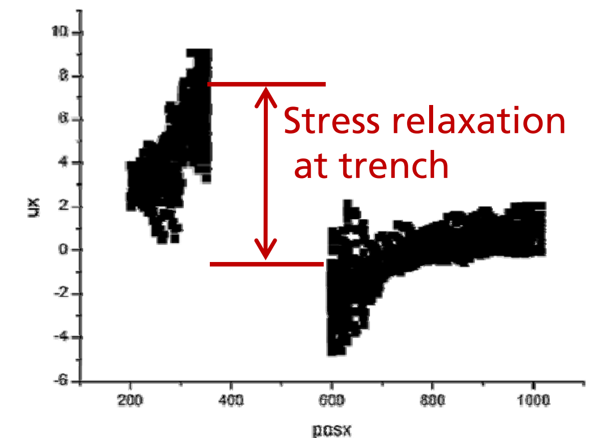
- Analysis of stress development in Cu / low-K BEoL systems
- currently PECVD SiO2 and SICOH as low-K materials
- stress in dependence on technological processes
- stress development over time (after CMP, tempering, Si_3N_4 barrier deposition)
- stress dependence of line / spacer gap





Trench displacment field for SiO

line width: 1.6 µm
line spacing: 1.2 µm



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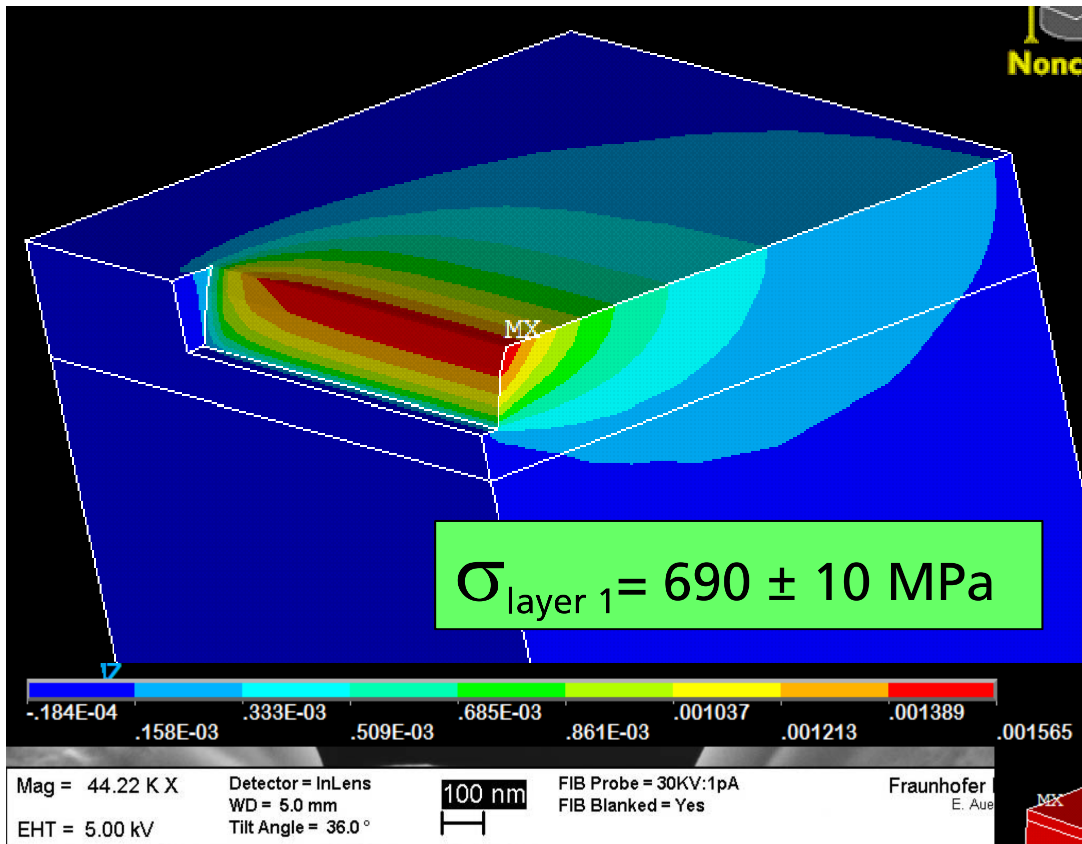
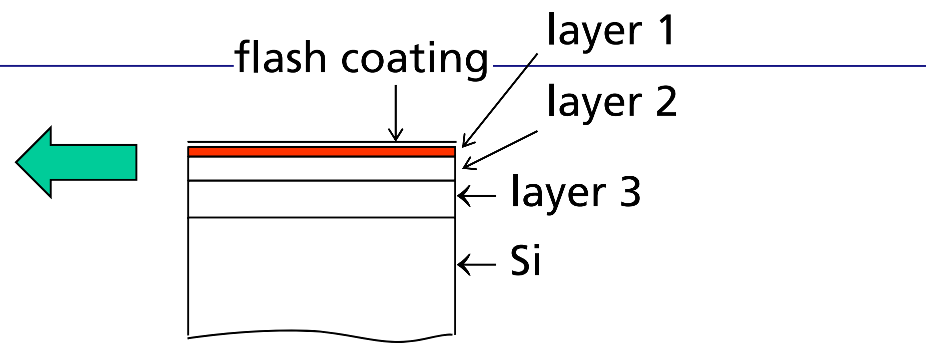
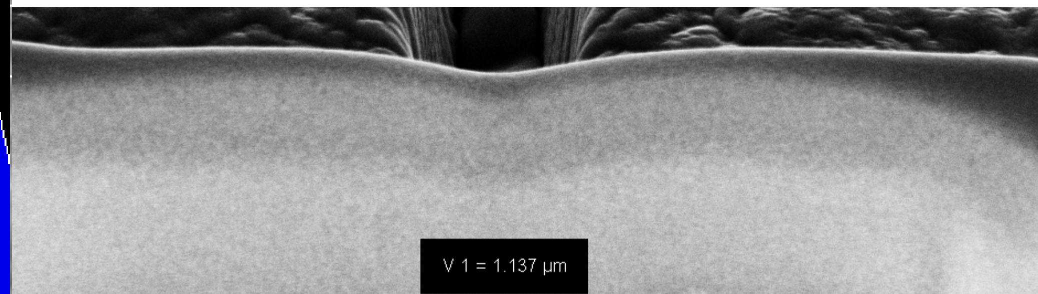
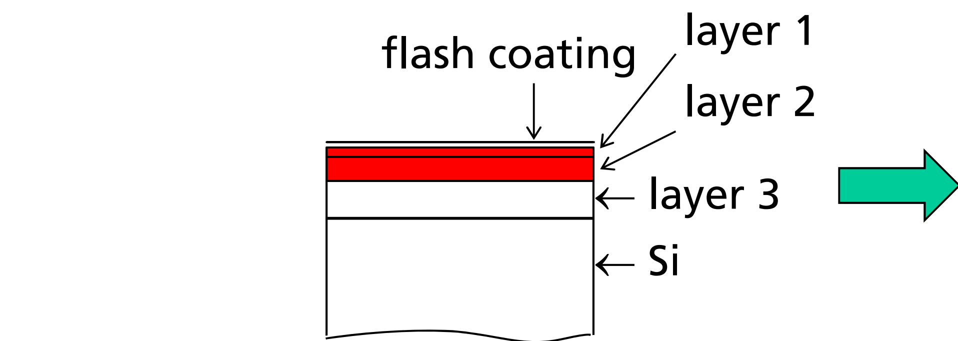
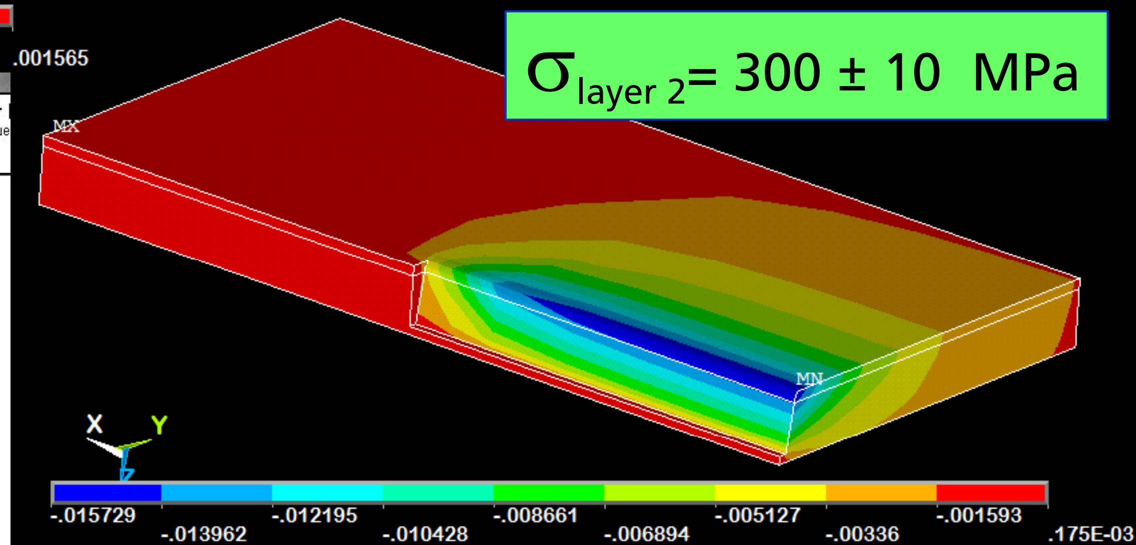
fibDAC stress relief – example of multilayer measurement











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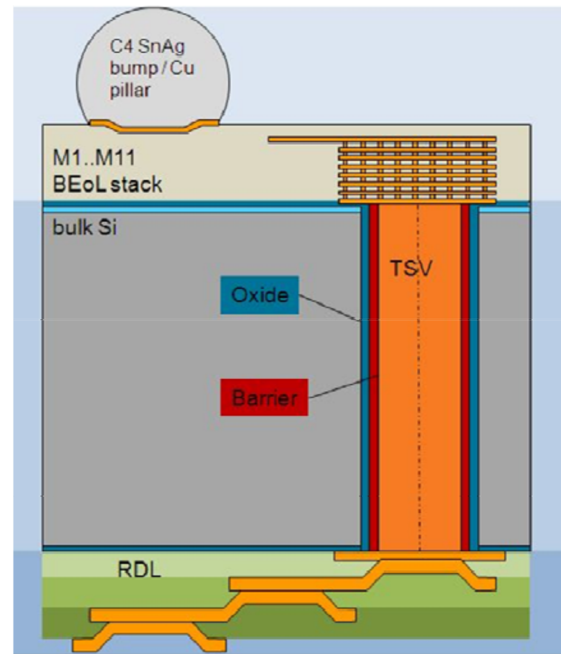
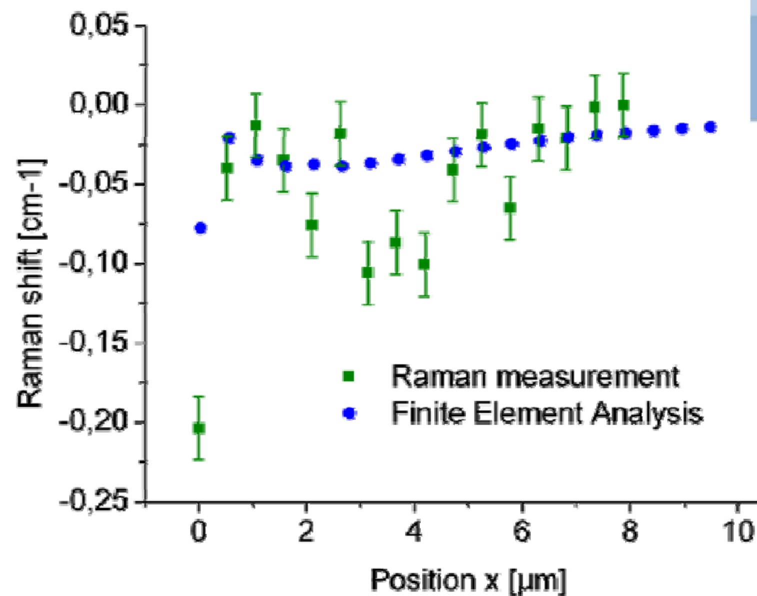
TSV and BEoL-structure for 3D-IC-integration

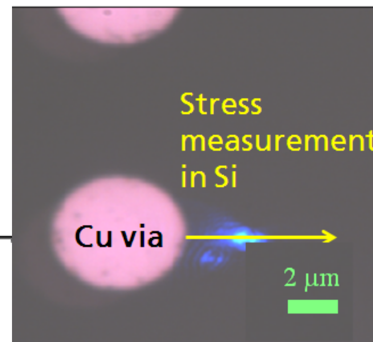
Basic problems with microRaman stress measurements on TSVs:
- accuracy limit due to mutual Raman shift compensation caused by different stress tensor components



Main obstacles of 3D integration are reliability concerns related to built-in stresses. Currently insufficiently understood and non-controlled issues are

- mobility changes of charge carriers due to stress
- stress driven delaminations and Si bulk cracks
- respective implementations into IC design rules





Examination of residual stresses caused by Cu-TSV manufacturing (microRaman measurement for validating finite element modeling)

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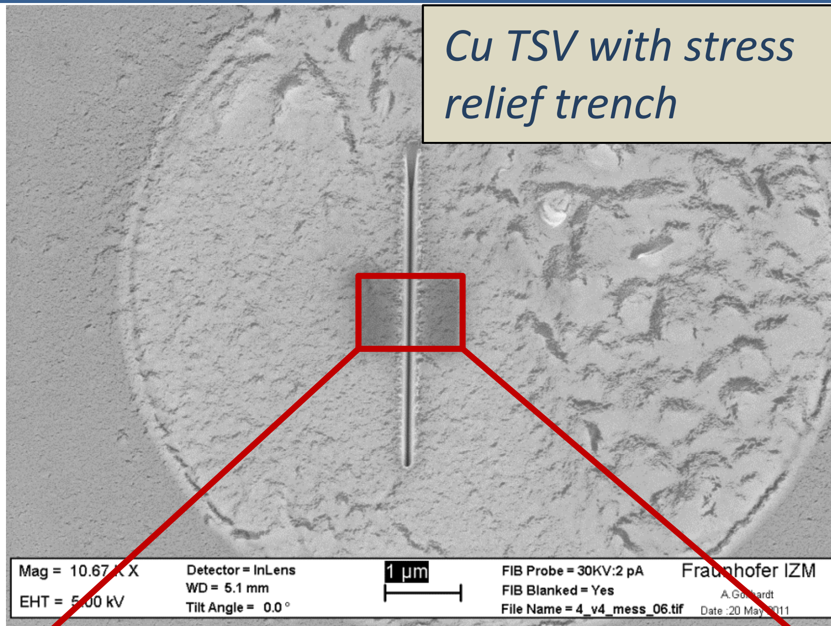
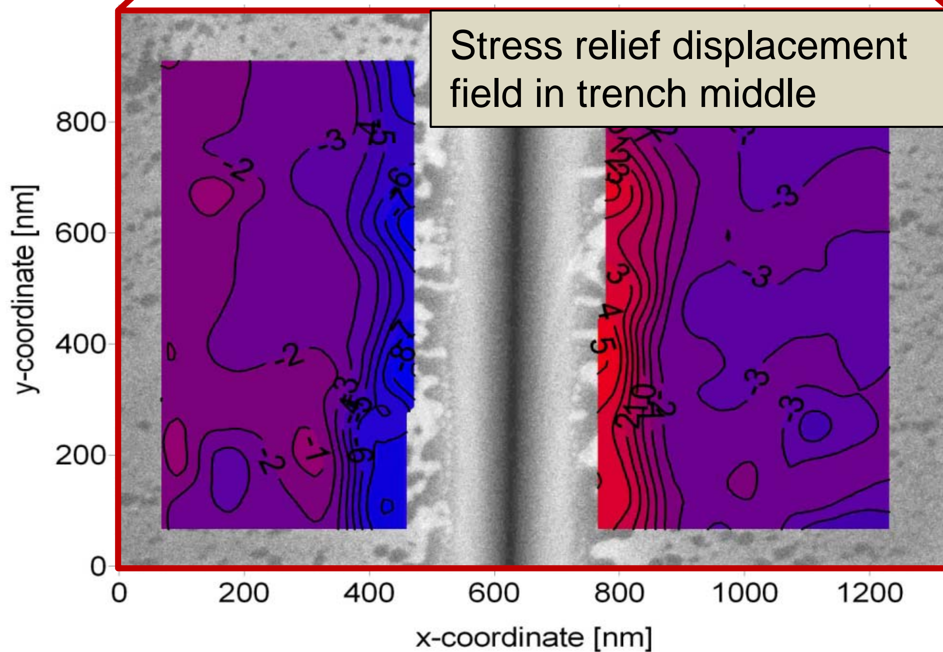
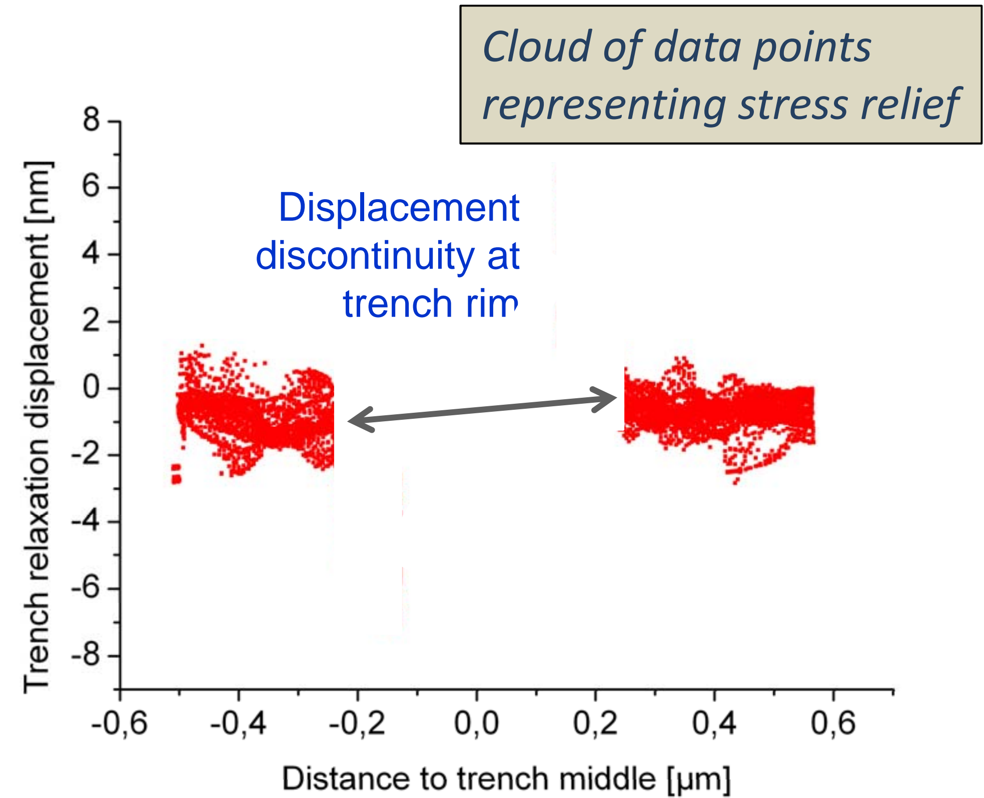
fibDAC measurements on Cu TSV's





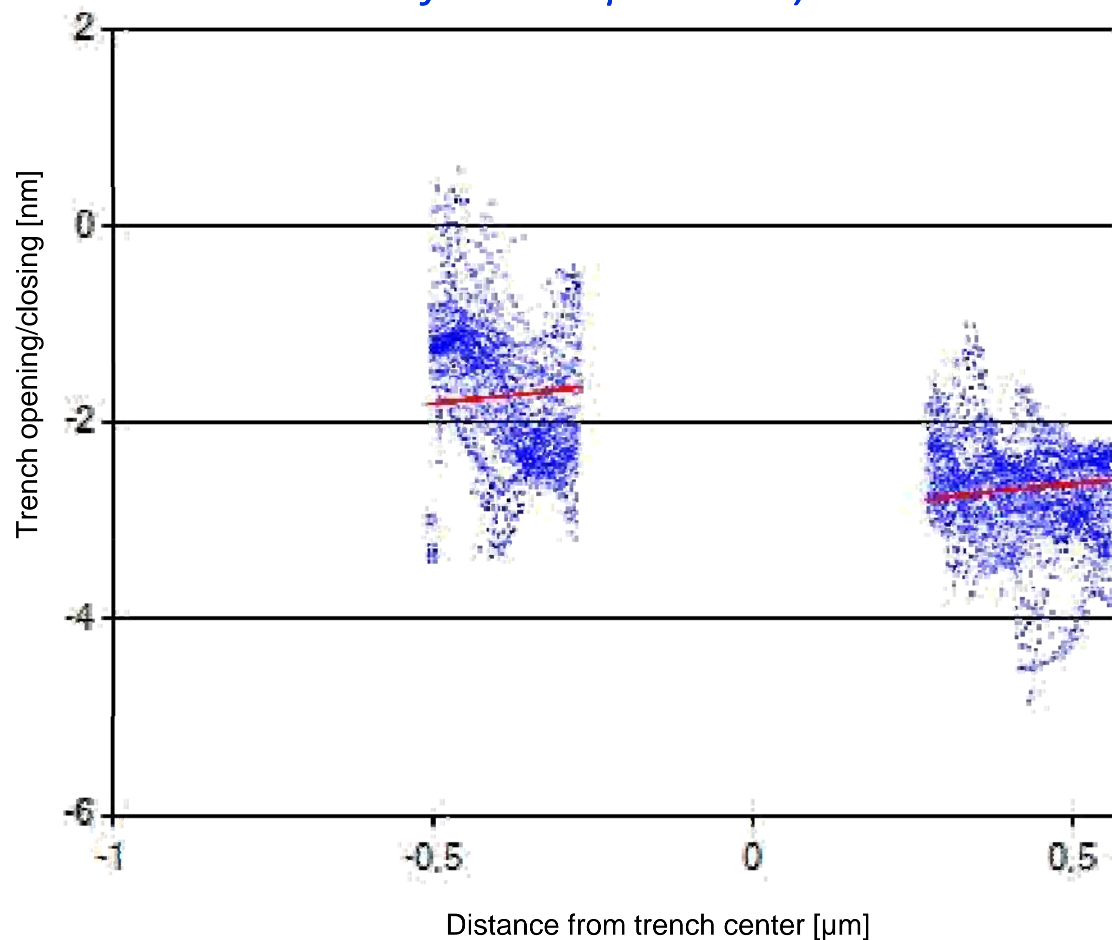


- *Stress extraction by fitting FEA results to experimental data*
- *Application of appropriate 2D & 3D stress models for FEA*

fibDAC measurements in Cu TSV's – stress extraction far from trench rim

Fitting of experimental and 2D simulation data

- ***obtained stress value: -127 MPa*** *(compressive stress)*
- *3D FEA model lead to values: -66 … -351 MPa (in dependence on material model and stress-free temperature)*



Stress levels computed by 3D FEA (elastic, elastic-plastic with kinematic strain hardening):

425_RT_elast:	-351
425_RT_el-pl:	-158
RT_425_RT_el-pl:	-66

Conclusions

- *Finite Element Analysis (FEA) – a powerful tool to accelerate and ease MNT device development*
- *Advanced FEA techniques to set up failure avoidance strategies*
- *FEA & failure modeling allows integration of reliability goals into device development*
- *New local stress measurement techniques give access to patterned multilayer systems on semiconductor and MEMS devices*

Thank you for your attention !