ADELES Program

ADvanced

ELEctronics

packaging

for

Space

15th October 2012

3D Plus
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Why this program ? What is the high level problem ?

- Reach customer expectations in terms of easy use of our modules for Space applications

- Competition is becoming stronger with the introduction of screened COTS

- Core technology of 3D Plus is based on stacking of IC TSOP:
  - These packages may disappear in the medium term
  - Memories of families are no longer available in TSOP

- Intellectual property must be renewed and strengthened:
  - Basic patents are old
  - Counterfeiting and copying are critical

3D PLUS must respond with
one (or more) jump(s) technology(s) and advanced products for the space market

What is Customer Need ?/ Voice for Space Module ?

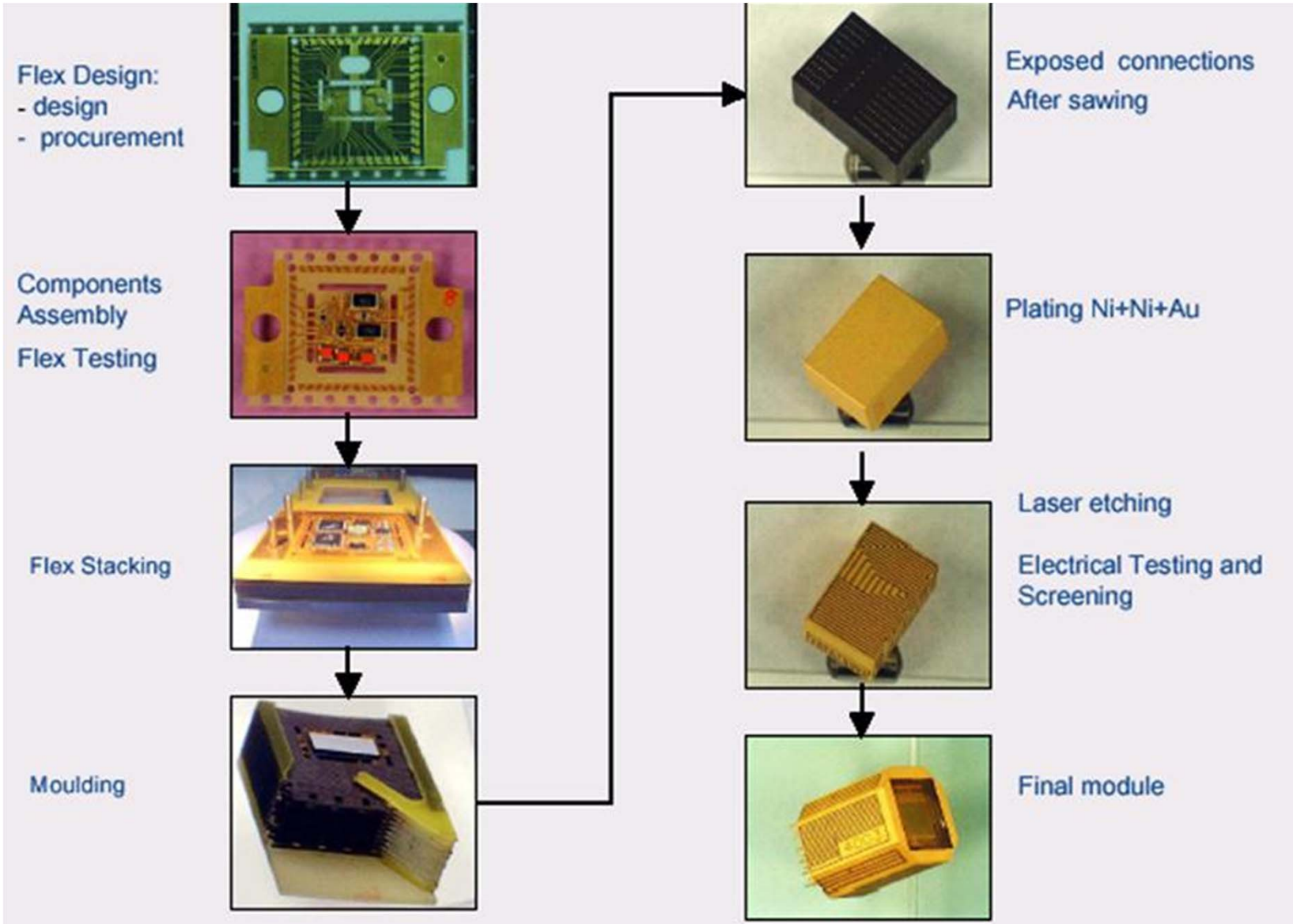
- **Voice Of Customer / Voice Of Business/Market:**
  - To ensure a wider process window for module assembly (on board)
  - To improve the vertical interconnection protection (active sides)
  - To have more standard leads : gull wing type
  - To miniaturize more and more in z-axis
  - To use a larger range of package type integrated in Module
  - To improve documentation
  - To improve performances

- **Constraints:**
  - Full compatibility with reference ESA-ECSS-Q-ST-60-05
  - Maintain or improve reliability
  - REACH compatibility

Multi project - which parameters to reach objectives?

- **To ensure a wider process window for module assembly on board**
  - o Peak temperature of body package max 225°C up to 245°C
  - o Moisture Sensitive Level 3 up to 2a/2
- **To improve the vertical interconnection protection (active sides)**
  - o For user during assembly on board (manual or automatic)
  - o For user during post assembly process (cleaning, repair,….)
- **To have more standard leads : gull wing type**
- **To miniaturize more and more in z-axis**
  - o To reduce the height of module (stacked levels and leads)
  - o To evaluate&qualify molding before stacking
- **To use a larger range of package type integrated in Module**
  - o Package BGA, Quad Flatpack No lead, Land Grid Array
  - o Bared die, Wafer Level Package, wire bonding – wirefree process
- **To improve documentations and data access**
  - o External and Internal documentation
  - o Design guidelines, Quality guidelines
  - o Database access for customer
- **To improve performances**
  - o Tooling for electrical and thermal modelisation & simulation
  - o Tooling for mechanical modelisation & simulation

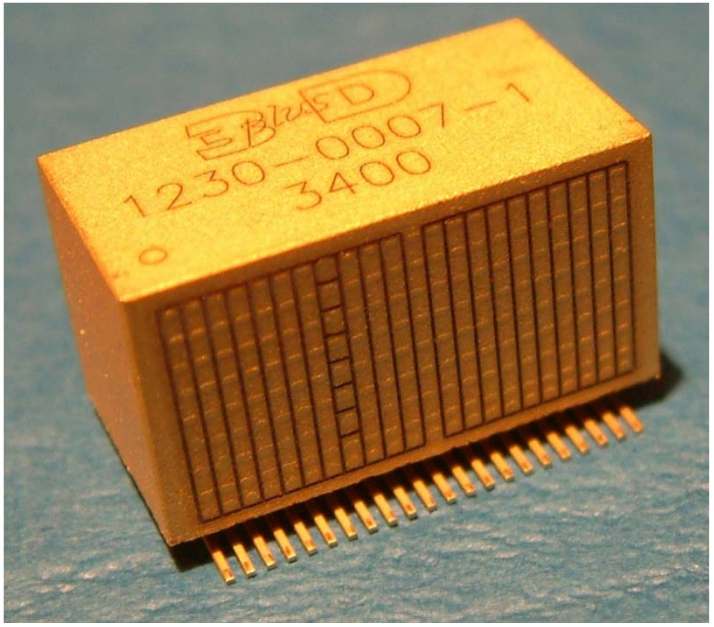
Edge connection manufacturing flow2(SoW)



What is the Current State (SoW)?
What is the Desired State?

Current state (PID7)

- *MSL6 – 215°C*
- *MapSil/Arathane varnish*
- *Connectic: SOP, QFP*
- *Height/Nb levels: 4 à 10,6mm / 2 à 8*
- *IC devices: TSOP*
- *Passive size 0805*



Example of ADELES results

Desired state (PID10&11)

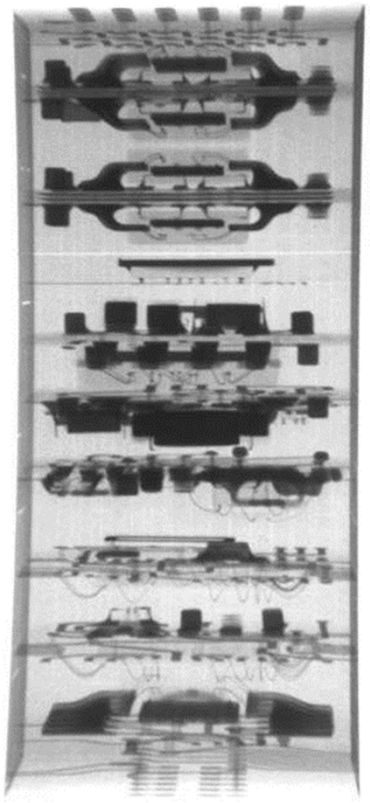
- *MSL3 – 245°C*
- *Verticale Interconnections non visible*
- *Connectic: Gull Wing, BGA*
- *Height/Nb level: 2,5 à 7mm/ 2 à 8*
- *IC devices: BGA, QFN, LGA,….,*
- *Passive size 0402*
- *Rth Jonction-Board: reduced*
- *Performances: increased*
- *Reliability: improved*
- *Certification: ESA*
- *Customer Satisfaction : improved*

What could be future application coming from ADELES program? For Space Application

- Example : Wireless Autonomous measurement sensors networks for data acquisitions (vibration, temperature,..) to measure and record parameters during flight

(source : e-cubes project EEC)

- Extreme miniaturization (8x8x14 mm)
- Robust
- Long time data retention
- Very low power consumption
- Easy mounting on the aircraft



Multi Generational Plan & Multi projects

PID 7 | PID 9 | PID 10 | PID 11

01/2013 — 01/2015 — 01/2017

Technical Developments & Evaluation
10/2012 – 01/2015 (PID10)

Industrial Developments & Qualification
01/2014 – 12/2015 (PID11)

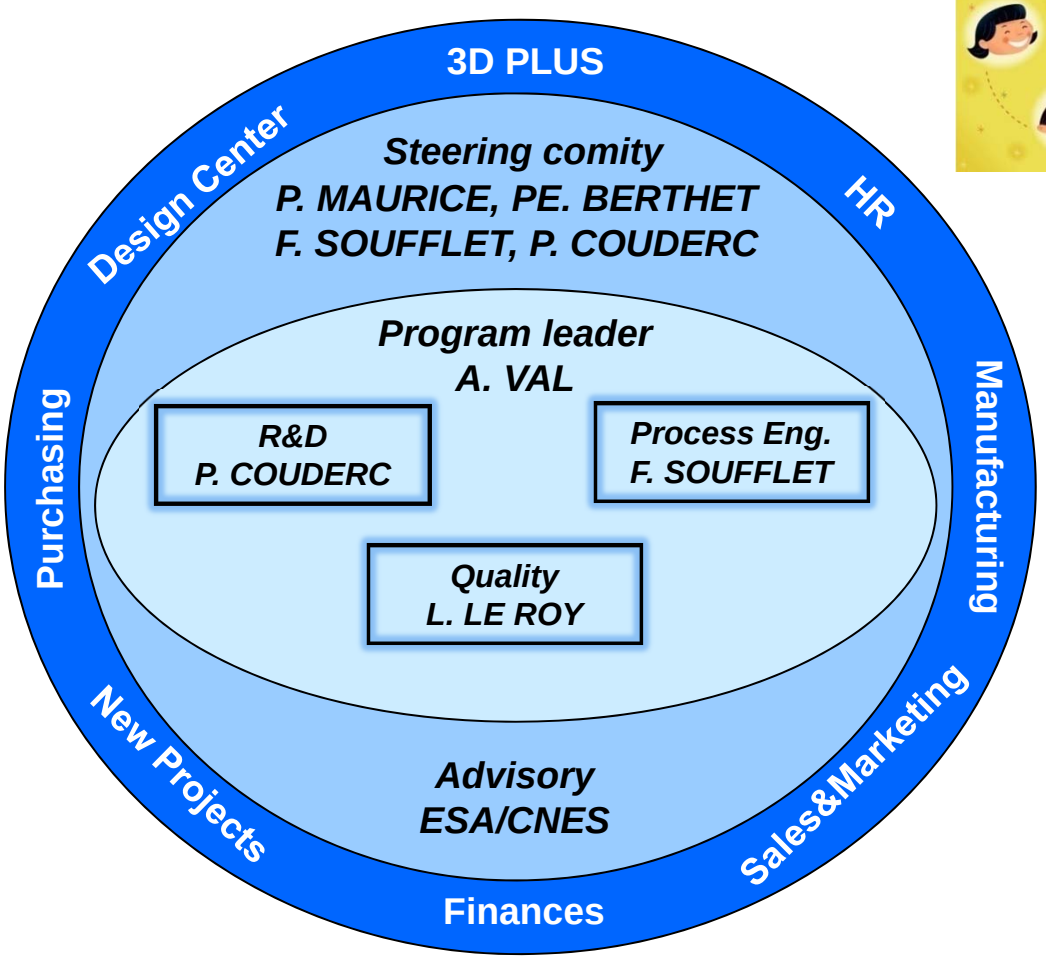
Deployment and Monitoring
01/2015 – 12/2016

Transversal Developments
01/2013 – 12/2015

Management
(Projects, Benchmarking, Intellectual Property,…)
06/2012 – 01/2017

Timeframe : 4 Years
Estimated Budget : 4 M€

Work group? Human Resources and responsibilities? Steering comity?



Team & responsibilities

A Val : Program Manager

P Couderc : R&D Manager

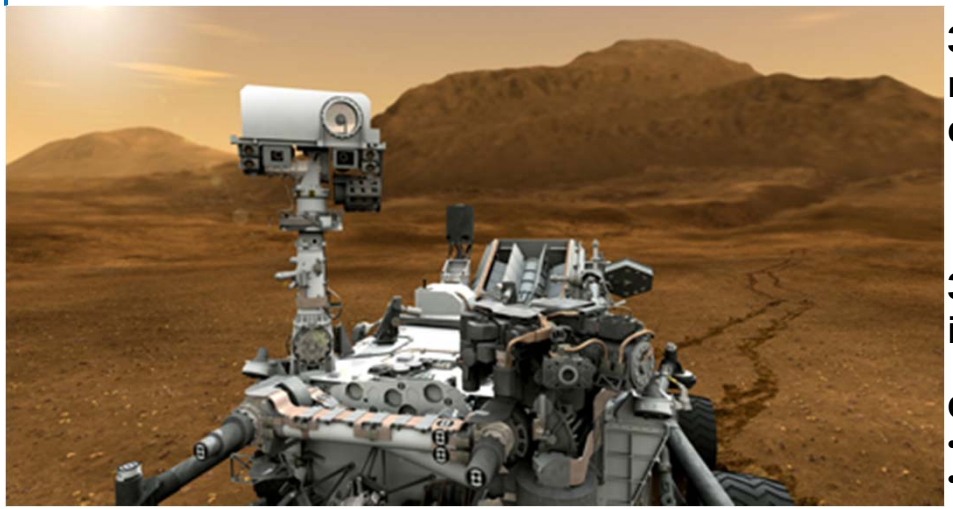
F Soufflet : Process Engineering Manager

L Le Roy : Quality Director

External contributors

ESA / CNES : Advisory board

Whole people is involved in the program – Multidiscipline team



3D Plus provides key modules for the operating memory of the avionics computers that controlled the landing:

- **2Gb SDRAM**
- **256Mb Nor Flash**

3D Plus provides complex SiP for CHEMCAM instrument:

On-Board Processor SiP

- 1MGate FPGA
- 6Gb SDRAM
- EEPROM
- Power supply and supervision electronics

CCD Camera SiP

- CCD Sensor
- Driving electronics
- Amplification & A/D conversion
- Pre processing & transmission

For further information on ADELES:
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