Highly reliable and low voltage actuated Ohmic RF MEMS switch with waver level packaging

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Page 1 Fraunhofer ENAS







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Contents

- Introduction and motivation
- RF MEMS technology
- Design and simulation
- Test and analysis
- Summary and future directions







Page 2 Fraunhofer ENAS

General failure risks of MEMS Switches

Sticking	Large areas of electrodes or switch capacitance come into intimate physical contact (low roughness) and there is too low force to separate the contacts . Welting of α -spot, A-fritting.
Charging	Dielectric materials in between electrodes accumulate surface charges or charges are trapped in the material from fabrication (e.g. anodic bonding) or from operation.
Contact wear	Contacts physically destroyed/ deformed because of plastic deformation of too weak or too thin contact material, inclusions of dielectric residuals into the metal after mechanically breaking the insulating flayers.
Contamination	Organic residuals from fabrication/ packaging, water, oxide or hydrocarbons crack products on contact surface lead to high contact resistance when the contact force is not sufficiently high.
Hermeticity	Un-sufficient hermeticity leads to increased switch time (gas damping) and to risk of contact contamination.
Overload	Break trough of open contact leads to physical damage of the comparably extreme small sized contact tips. Current overload results in melting of contact material, welding and generation of alloy (e.g. AuSi) witch high specific resistance .
ESD	Driving electrodes and contact may be damaged by electrostatic discharge during fabrication (anodic bonding) or while handling.

Page 3 Fraunhofer ENAS







Goals of this Work:

Page 4

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The target is potentially **high reliability of switch devices by novel technology and suitable design**.

- 1. No dielectric material between movable and fixed structures, **no charging.**
- 2. Wafer level vacuum encapsulation, and contact material deposition in on of the last fabrication steps, **lowest possible contamination.**
- 3. High force when closing and when closed, achieve stable and low contact resistance.
- 4. High force for separation, prevent sticking.







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MEMS Technology for RF Applications

- Air gap Insulated Micromachining (AIM) Process
- Highly resistive Si-wafers, no SOI-wafer necessary
- 50 µm deep movable structure, large electrode area
- Contact metal sputtering in contact area trough shadow mask





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Cost-efficient packaging (0 level) by wafer bonding in vacuum or in inert gas



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Photograph of a single chip



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Chip layout and special features



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Simulation of Force and Motion





Analysis and optimization by FDTD



S-Parameter Magnitude in dB

Measurements

4 GHz type





Isolation: -30 dB @ 3 GHz Max. insertion loss: 0.5 dB including bond wires

> Page 11 Fraunhofer ENAS



Switches in actuated state



Measurements

80 GHz type





Isolation: -20 dB @ 60 GHz Max. insertion loss: 2 dB @ 60 GHz



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Test sequences for life time test



Test phases are consecutively run till manually finishing the test e.g. after 1 Billion cycles.









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Life time test results











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Summary, Future Directions

Reliable and proven MEMS technology

- Large electrode area, high force even at low voltage (>100 µN contact force with <5V and < 30 nA)
- No dielectric material between electrodes
- Wafer level hermetic vacuum package



Design and test

- •Mechanical design and simulation
- •Optimization of force and switch time
- •Analysis of µwave / mm-wave performance
- •Reliability test (cold switching)



Future directions

- Improvement of isolation and insertion loss by modified mm-wave line concepts
- Improvement towards maximum power handling capability of 30 dBm
- Non-linearity: IP3 >>60 dBm

