8th ESA Round Table on Micro and Nano Technologies for Space Applications, 15-18 October 2012

Electrical Characterisation of Gamma-ray Irradiated High-κ Metal-Insulator-Metal Capacitors for Space Applications Evaluation

#2631229, 11.45am, Tuesday 16 October 2012

Session 4: Radiation & Miniaturisation

ESA/ESTEC, Noordwijk, The Netherlands

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Outline

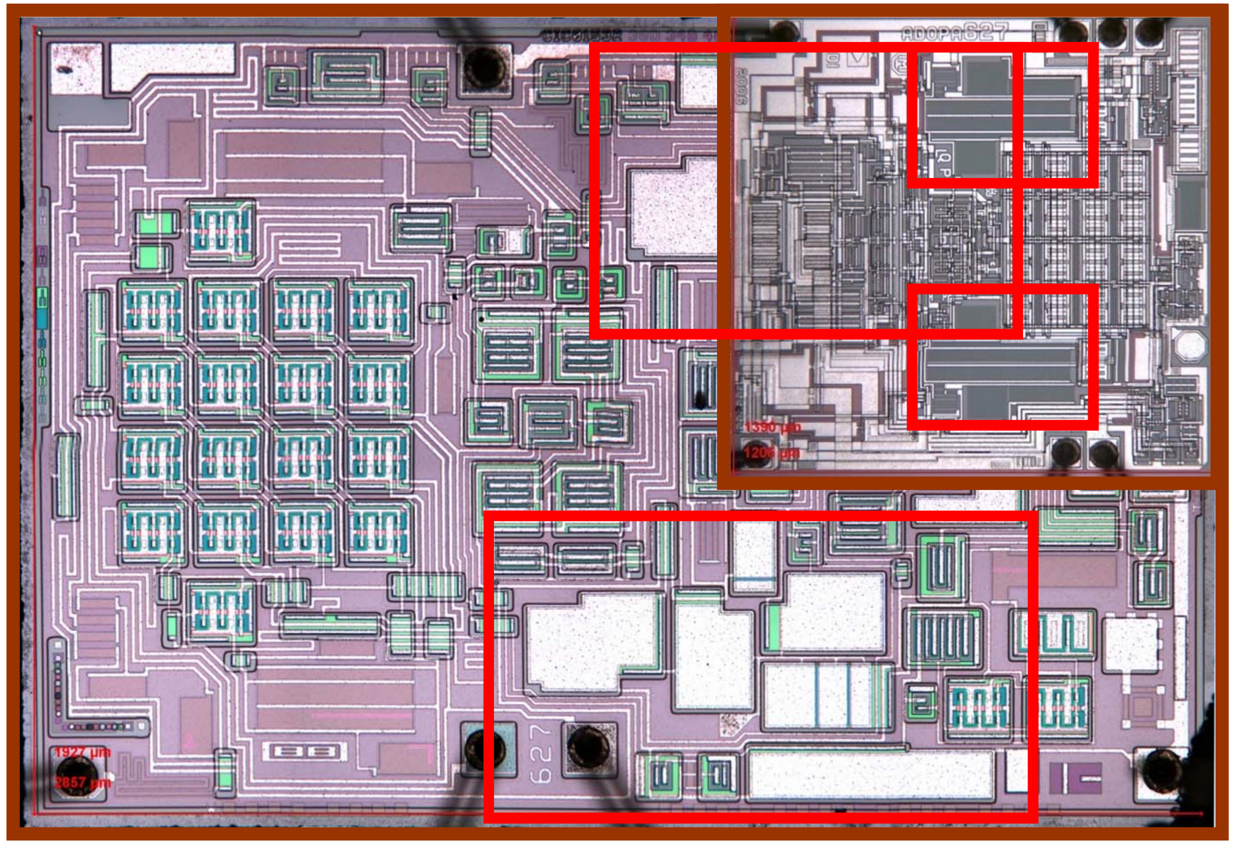
- Introduction
  - o Why high-*k* capacitors?
  - o Low-*k* dielectrics
  - o High-*k* dielectric challenges
  - o Barriers to high-*k* solutions
- "MISO" high-*k* invention
  - o Patent application
  - o Electrical results
  - o General properties
- Initial irradiation results
- Further irradiation research
- Conclusions and future plans

Tyndall III-V/Si Lab

Introduction

Why high-*k* capacitors?

- $C_{tot}=n\times k\varepsilon_0 A/t,\ k\sim 4k_0$
- $A_0/4=A$ for same C_{tot}
- Single MIM, $n=1$

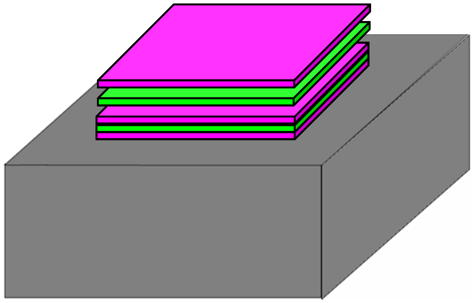


- Capacitors could have
  - Integration capability
  - Small surface area
  - Redundancy > 4×
  - Low power & weight

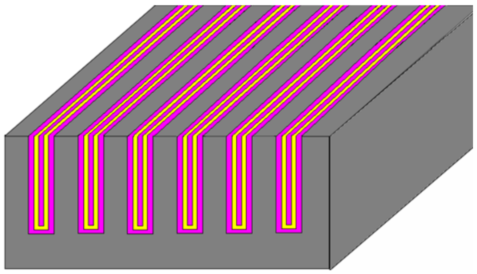
Introduction

Why high-*k* capacitors?

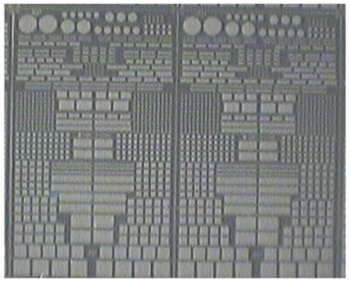
- Stacked MIMs, $n>1$
- Small 2D surface footprint



- 3D MIM, $n=1$, $A>>A_0$
- Stacked 3D MIMs
  - o $n>1$ **<u>and</u>** $A>>A_0$
- **Smaller surface footprint**



- Capacitors could have
  - o Integration capability
  - o Very small surface footprint
  - o Redundancy >> 4×
  - o Low power & weight



Our MIM device mask

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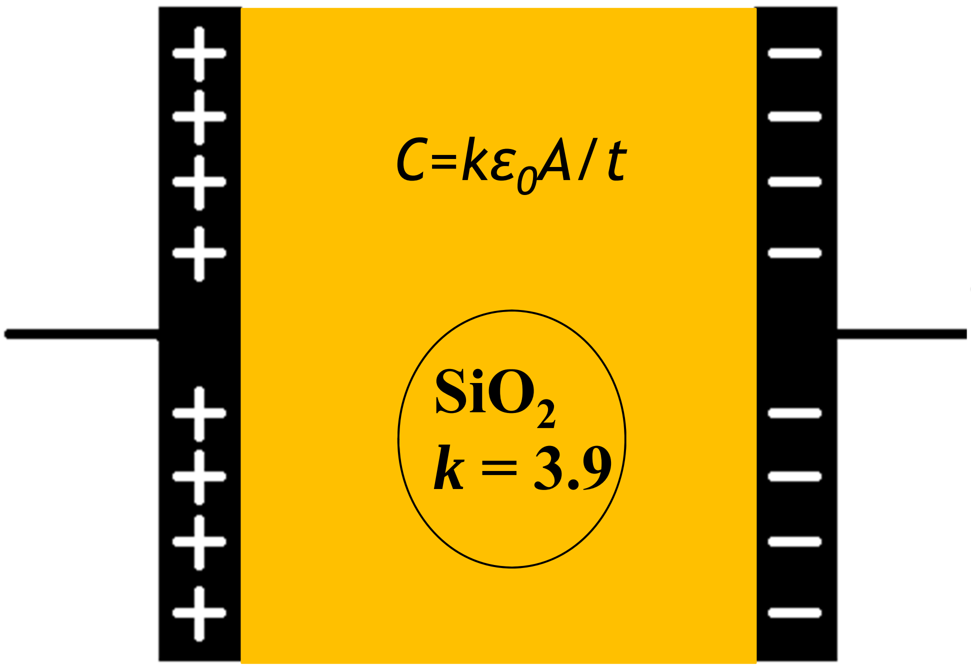
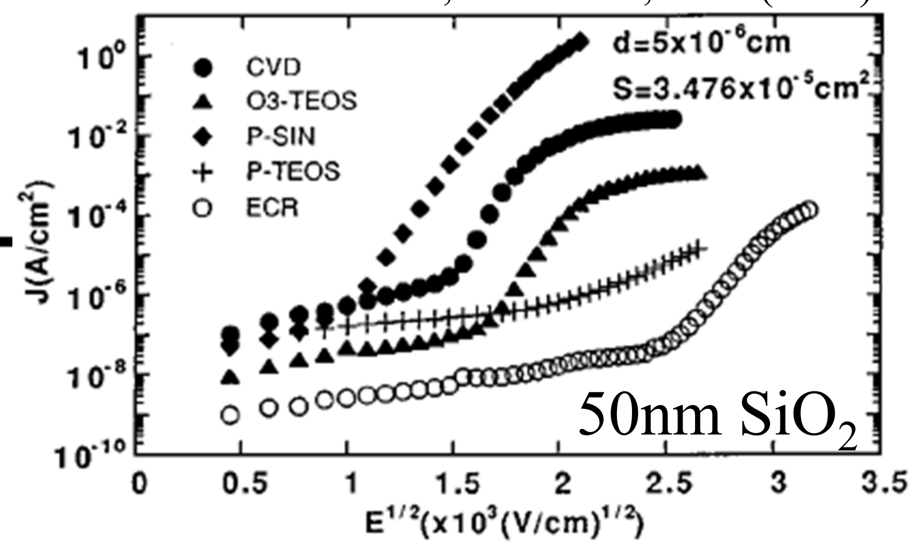
Introduction
Low-*k* dielectrics



K. Machida *et al.*, JVSTB **13**, 2013 (1995)



- **<u>Positives</u>** <u>of low-*k* dielectrics…</u>
  - Low leakage, low loss, high breakdown, irradiation hard
  - High temperature stability and linear capacitance with *V*, *f*, & *T*
- **<u>Negatives</u>** <u>of low-*k* dielectrics…</u>
  - Low capacitance/charge/energy storage → Large area capacitors
  - Poor for scaling, integration, low power and redundancy

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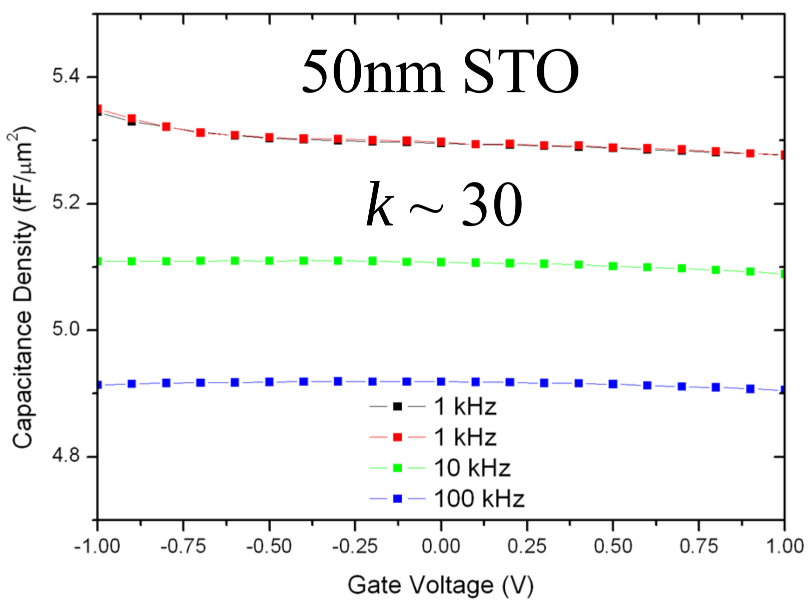
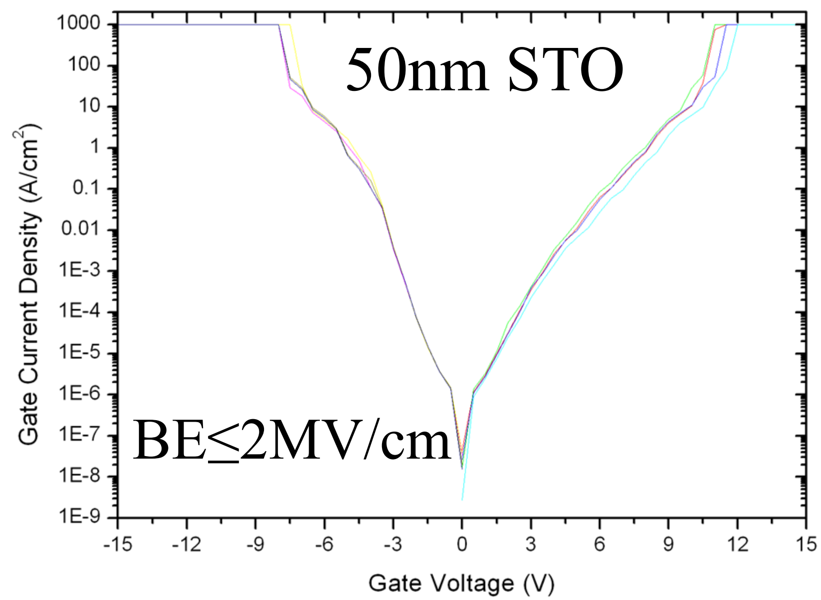
- **<u>Negatives</u>** <u>of high-*k* dielectrics…</u>
  - Greater leakage, higher dielectric loss, and lower breakdown
  - Low temperature instability and electrically poor when irradiated
  - Non-linearity of capacitance with *V*, *f*, & *T*
- **<u>Positives</u>** <u>of high-*k* dielectrics…</u>
  - High capacitance/charge/energy storage → Small area capacitors
  - Good for scaling, integration, low power and redundancy





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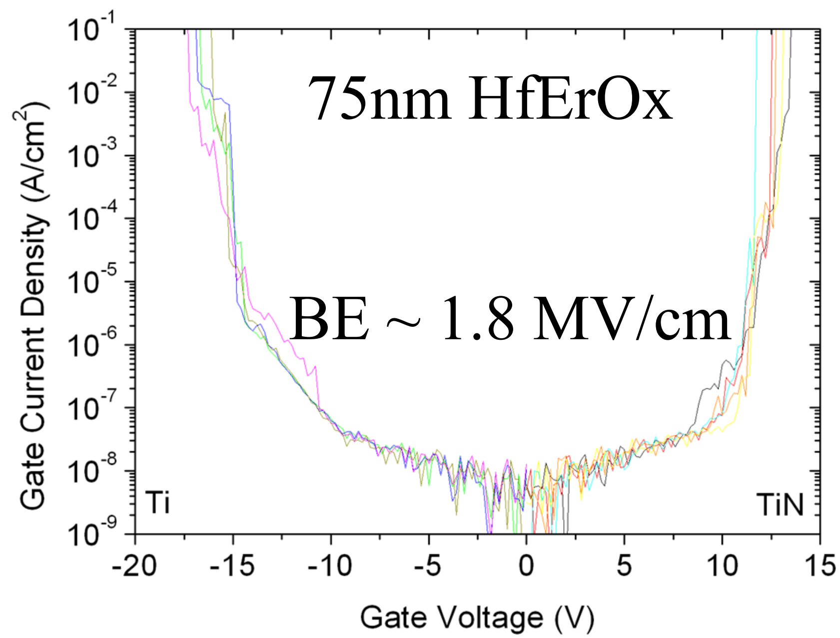
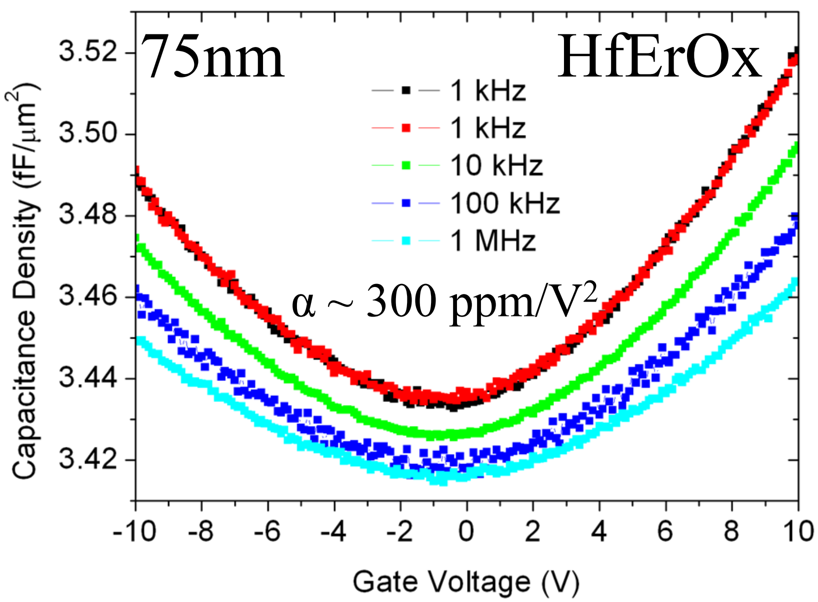
Introduction

Barriers to high-*k* solutions

- High operational leakage
- Transport mechanism variability
- Soft-breakdown events
- Low hard-breakdown voltage
- Variability in breakdown voltage
- Electrically poor when irradiated





- Capacitance non-linearity ($\alpha >> 50 ppm/V^2$) and injection asymmetry
- Frequency dispersion of capacitance
- High dielectric loss (low Q(*f*)-value)
- Low temperature instability <450°C

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"MISO" high-*k* invention

Patent application

- Metal-in-silicon-oxide (MISO)
- Based on $M_xSi_{1-x}O_2$ system
- M = Hf and/or Zr
- Other elements possible
- Atomic Layer Deposition
- Patent in progress*
- CMOS compatible material
- Stable at high temperatures
- Non-contaminant system
- Structures, *x*, ALD processes
  - o Confidential until patent process is complete

Cambridge NanoTech Fiji ALD Tool

University College Cork's Invention of the Year 2010 in ICT
Awarded: April 2011

*S. Monaghan and I. M. Povey, patent filed on 21 October 2011 (EPO#EP11186166.2; USPO#61549751)

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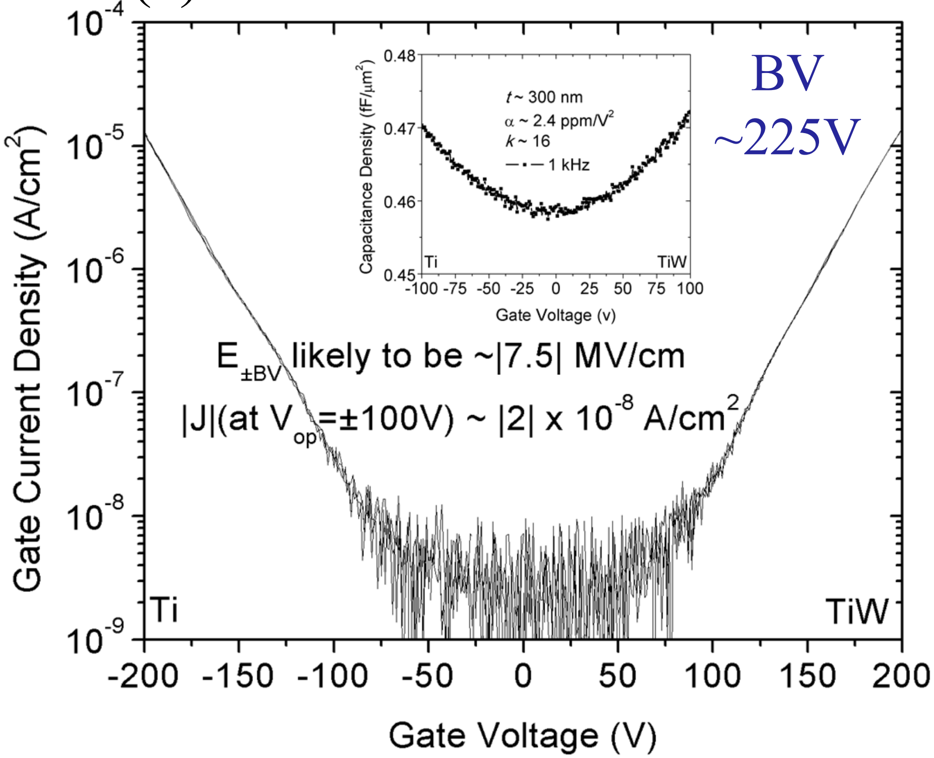
“MISO” high-*k* invention

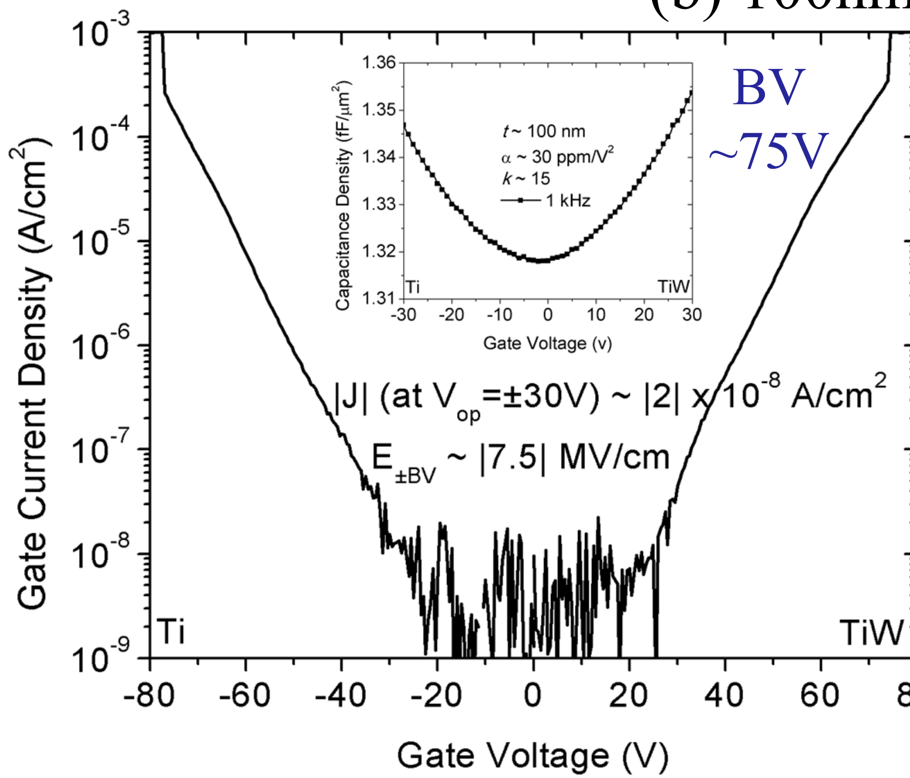
Electrical results

300nm and 100nm As-deposited Samples

(a) 300nm



(b) 100nm

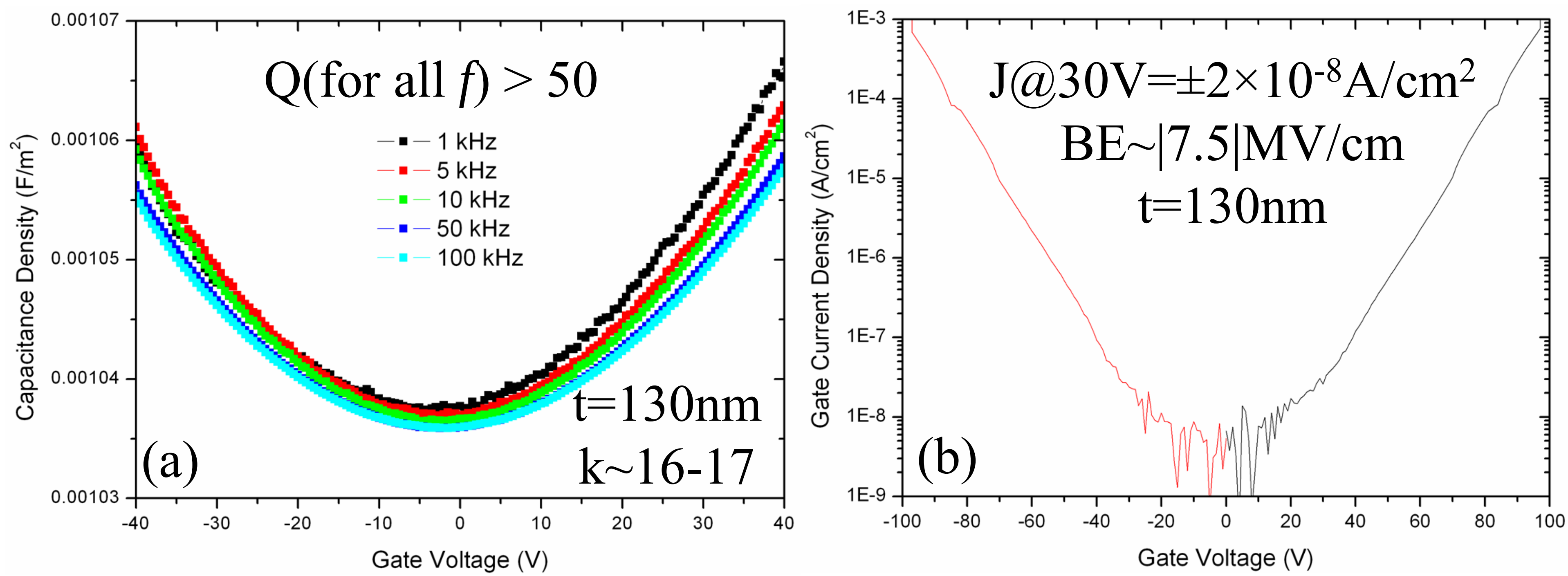


- JVs & CVs (insets) for as-deposited MIMs: (a) 300nm & (b) 100nm
- Leakage, breakdown, and general IV characteristics excellent
- Capacitance at 0V implies an effective *k*-value of ~15-16
- Linearity (α) is ~2.4/30 ppm/V^2 for (a) and (b) respectively

"MISO" high-*k* invention

Electrical results

130nm As-deposited Samples

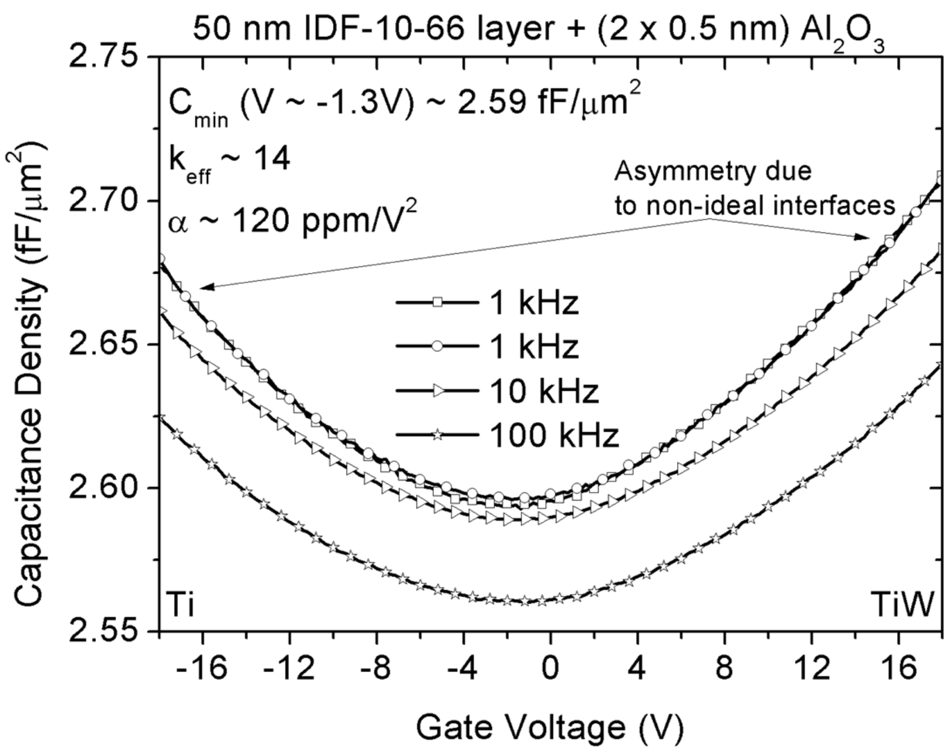


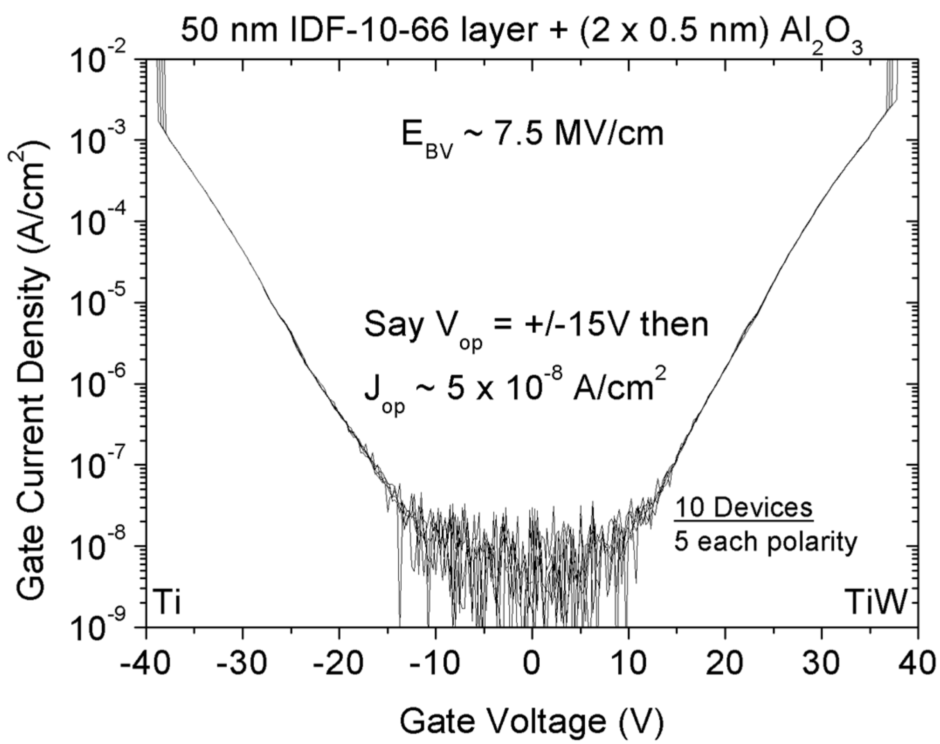
- As-deposited 130nm MIMs with Al electrodes: (a) CV (b) JV
- Capacitance at 0V implies an effective *k*-value of ~16-17
- Linearity (α) is ~15 ppm/V^2 and Q(*f*) > 50
- Leakage, breakdown, and general IV characteristics also excellent

"MISO" high-*k* invention

Electrical results

<u>50nm As-deposited Sample</u>





- As-deposited 50nm MIMs with TiW/Ti electrodes: (a) CV (b) JV
- J/BE excellent, general IV good, non-ideal interface effects in BV
- At ≤55nm interface effects begin to dominate CV behaviour
- Improved interfaces required to reduce effect on α and ΔBV

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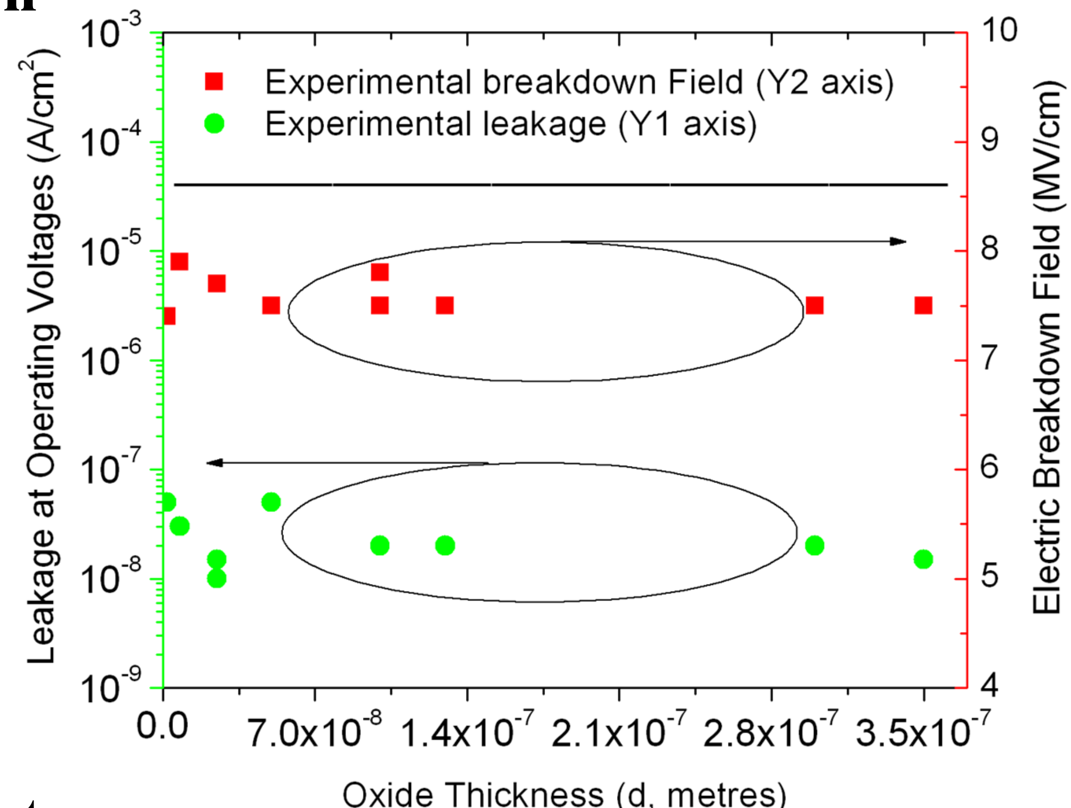
"MISO" high-*k* invention
General properties

- Constant J, E_{BD} for all t = 2nm – 350nm – **this is not common for high-k dielectrics!**
- High breakdown field ~ 7.5 MV/cm
- Low operating leakage ~1-5×10^{-8}A/cm^2
- No soft-breakdown & high temp stability
- Excellent reliability results (not shown)

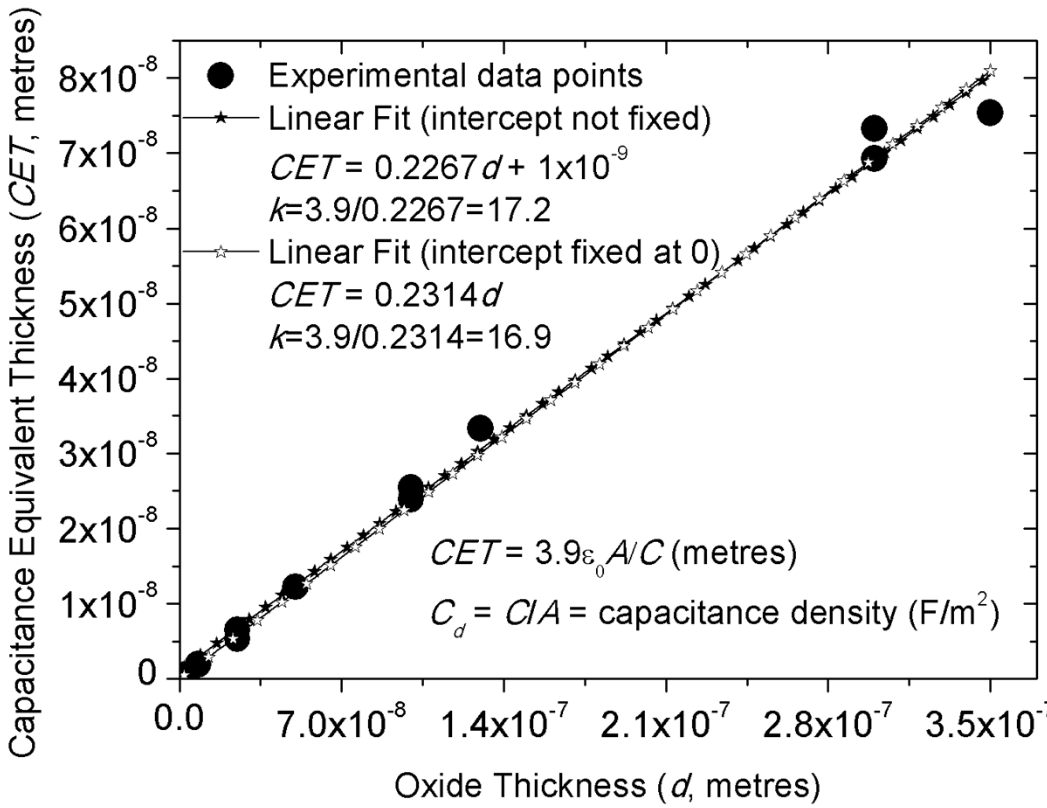


S. Monaghan and I. M. Povey, *Electronics Letters* **48** (4), 230 (2012)

“MISO” high-*k* invention

General properties

- Excellent repeatability
- CET v thickness linear
- Extracted *k*-value ~ 17
- Capacitance linearity
- Non-ideal interfaces



S. Monaghan and I. M. Povey, *Electronics Letters* **48** (4), 230 (2012)

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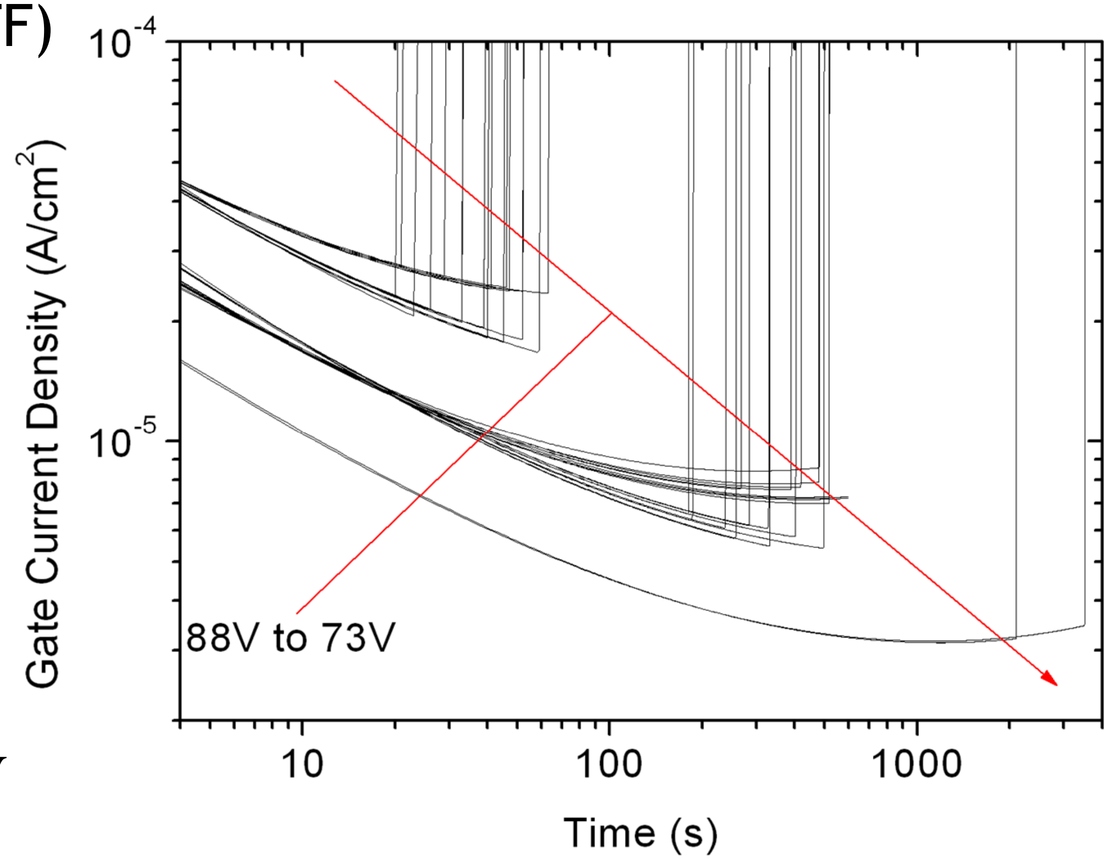
Initial irradiation results

Summary

- 130nm Al/MISO/Al tested
- Mean-Time-To-Failure (MTTF)
- MTTF for control sample
- MTTF for 78krad sample
    - o **Zero bias irradiated**

Mean of total sampling at each voltage taken to get *t* versus BV



<u>Irradiation conditions*</u>

Control samples retained

Gamma rays from ^{60}Co at 0V

Total 16krad (210rad/min)

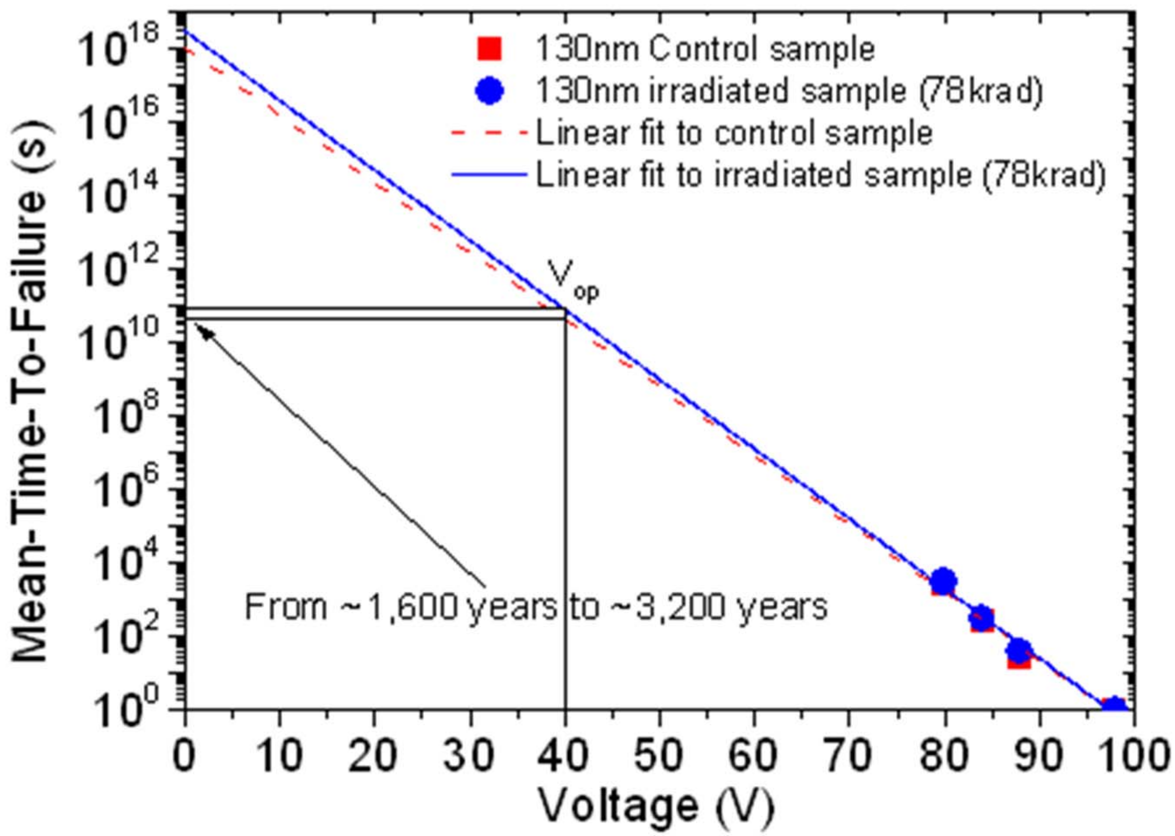
Total 78krad (210rad/min)

*Thanks to ESA and co-authors OZO, RD

Initial irradiation results

Summary

- Each point mean of sampling
- Operating voltage = 40V
- MTTF similar for both samples
- Lifetime at 40V is ~1-3k years
- **No degradation after irradiation**



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Further irradiation research

Funding required for test expansion

- Develop an extended MIM sample matrix for a DoE
- Oxide thickness, area/perimeter ranges, anneals, etc.
- MISO MIM structures tested in ESA components
- Gamma irradiation again from ^{60}Co
- Bias devices for different *V* at different total doses
- Dose levels to test shielded LEO*/GEO** capability
- Higher dose levels to test unshielded LEO/GEO capability
- Maximise radiation variety to assess effects of
    - o Trapped electrons and protons
    - o Solar energetic particles
    - o Cosmic rays
    - o Secondary radiation

LEO*: Low Earth Orbit GEO**: Geostationary Orbit

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Conclusions and future plans

- A high-*k* material that remains stable at high CMOS temperatures
- CMOS process compatible and a non-contaminant
- Electrical properties constant with scaling from ~350 nm to ~2 nm
    - Constant k-value of ~17
    - Constant high breakdown field (~7.5 MV/cm)
    - Constant low leakage (~1-5×10^{-8}A/cm^2 @ operating voltage)
    - Capacitance linearity with *V*, *f*, *T* (when bulk dominates)

Conclusions and future plans

- Presently working at increasing the ALD rate >4× for industry
- Research on going to boost *k*-value further & reduce interface effects
- Initial gamma irradiation tests (at 0V) show no effect on MIMs
- MTTF gives lifetime prediction of ~1-3k years at operating voltage
  - **However, only 130nm investigated in a limited way so far**
- Funding support needed for full irradiation testing
- Potential for integration, scaling, redundancy & low power

inspire

Integrated NanoScience Platform for Ireland

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Go raibh maith agaibh! (Thank you all!)

We acknowledge (1) the European Space Agency (ESA) for irradiation tests that were performed as part of the NPI activity between Tyndall-UCC and ESA on the reliability of RF MEMS capacitive switches; (2) INSPIRE (PRTLI5, HEA, NDP 2007-2013, and the ERDF) for the PhD funding support to co-author BJAH; and (3) Enterprise Ireland, via projects DIELECTRIkAPS (CF-2011-1700Y) and ALECTRIkA (CF-2012-2002)