TOTAL DOSE RADIATION TEST REPORT

High Dose Rate

Part Type : NPSE-TC9 chip

1M-bit SRAM Cut 1 - 6T SRAM cell.

1M-bit SRAM Cut 2 - 6T2Cdram rSRAM cell.

Manufacturer : STMicroelectronics

STMicroelectronics Purchase order No PD 4000083535 dated 13/01/04

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TOTAL DOSE RADIATION TEST REPORT on NPSE-TC9 chip Cut 1 & 2

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1 INTRODUCTION

This report presents the results of a Total dose radiation evaluation (TID) test program carried out on two memory cuts, Cut 1 and Cut 2 of NPSE-TC9 chip, from STMicroelectronics.
This work was performed for STMicroelectronics under STMicroelectronics Purchase order No PD 4000083535 dated 13/01/04.

4 samples have been tested up to an accumulated dose of about 1Mrad(Si) at a dose rate between 15 to 40 Krad(Si)/hour.

In addition 2 samples have been further submitted to an annealing sequence at room temperature, then at 100°C.

2 REFERENCE DOCUMENTS

RD1. RD-1. NPSETC9_1 testchip, Version 1.4, Central R&D Crolles, 26 August 2003
RD2. RD-2. 7/28/2003 – Netlist, NPSE testchip, NPSEin5PM03255_Rev3.txt
RD3. RD-3. SUBSTRATE PBGA 27X27-256+16 BALLS PAD 10.25X10.25MM, 7186129 Rev B, 16–DEC–2002
RD4. RD-4. RAPIDOV2, version 2.0, Testchip&Tools Team, 8 November 2001
RD5. Hirex proposal ref. HRX/PRO/0826 Issue 2;

3 DEVICE INFORMATION

3.1 NPSE-TC9 chip

1M-bit SRAM Cut 1 - 6T SRAM cell with deep buried layer (NISO).
1M-bit SRAM Cut 2 - 6T2Cdram rSRAM (LIL strap) cell with deep buried layer (NISO).

Each cut is organized as 1 Bank of 32768 words of 32 bits (mux 32) of 1024 rows and 1024 columns
Address size is 15bits

4 Test Definition

4.1 Test Set-up

Hirex test equipment is composed of a modular rack coupled with a generic memory test board :

This modular rack is derived from Hirex BILT modular instrumentation system and present 8 slots for modular instruments.
Dedicated to the test of memories, the generic test board is based on a 12 MIPs on-board processor which controls the test sequence and the communication with the rack.
The board include programmable logic circuits with a total capacity of 30000 cells and 960 macrocells. This logic circuitry can work at high speed (up to 100 MHz) while being compatible with thermal requirements imposed by vacuum environment.
Today, the board has a capacity of 80 pin-drivers , using transceivers able to interface memory devices with voltage supply requirements between 1 and 7 volts. The DUT can have two different power supplies.

4.2 Bias conditions under exposure

Test is performed at room temperature.
The two memory cuts are addressed in sequence.
A 2.5 cable allows providing a unique power supply to the DUT (current is monitored in situ) as well as the different signals for read/write operations.
The DUT was tested in static conditions, which consist in the following cycle, repeated continuously.
Test cycle period was set to 60s (iteration).

- Send the write commands sequence to write the entire memory (cut1 then cut2)
- Wait for a given time period (60 s)
- Send the read commands sequence to read the entire memory (cut1 then cut2).

Test pattern consists in a repetitive pattern shown in Table 1. An offset in the pattern at each cycle allows to check that every word has been effectively rewritten with new data.
The table here below provides, for each group of 4 bits, the 14 words repetitive pattern.

	It k	It k+1	It k+2	It k+3	It k+4	It k+5	It k+6	It k+7	It k+8	It k+9	It k+10	It k+11	It k+12	It k+13	It k+14
address n	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000
address n+1	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010
address n+2	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101
address n+3	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111
address n+4	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001
address n+5	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110
address n+6	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101
address n+7	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000
address n+8	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010
address n+9	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101
address n+10	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111
address n+11	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001
address n+12	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110
address n+13	1010	0101	0110	1010	1001	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010
address n+14	0000	1111	0101	0101	0110	1010	1001	0000	1111	1010	0101	0110	1010	1001	0000

Table 1 – Test pattern

DUT current consumption is monitored all along the exposure.
VDD value was set to the nominal voltage (1V2).

4.3 Step Measurement conditions

To perform the functional check of the device, the DUT is mounted directly on the memory test board (without the 2.5m cable) and the two nominal current supplies are used.
Functional check consist in writing the two cuts then read to detect any single bit error. Several write/read cycles are performed and values of the two DUT current supplies are recorded.

4.4 Test plan

	CO-60 IRRADIATION							ANNEALING		
				Functional Check					Functional Check	
S/N #	Dose rate (krads/h)	Intermediate steps	In-situ DUT current monitoring	Initial	100 krads	500 krads	1000 krads	Annealing	Post annealing at Room Temp	Post annealing at 100°C
1	20	YES	YES	X	X	X	X	NO	-	-
2	37.7	NO	YES	X	-	-	X	NO	-	-
4	37.7	NO	YES	X	-	-	X	DUT biased at 1V2, 91 hours at room temperature followed by 174 hours at 100°C	X	X
6	15.3	NO	YES	X	-	-	X	DUT biased at 1V2, 25 hours at room temperature followed by 174 hours at 100°C	X	X

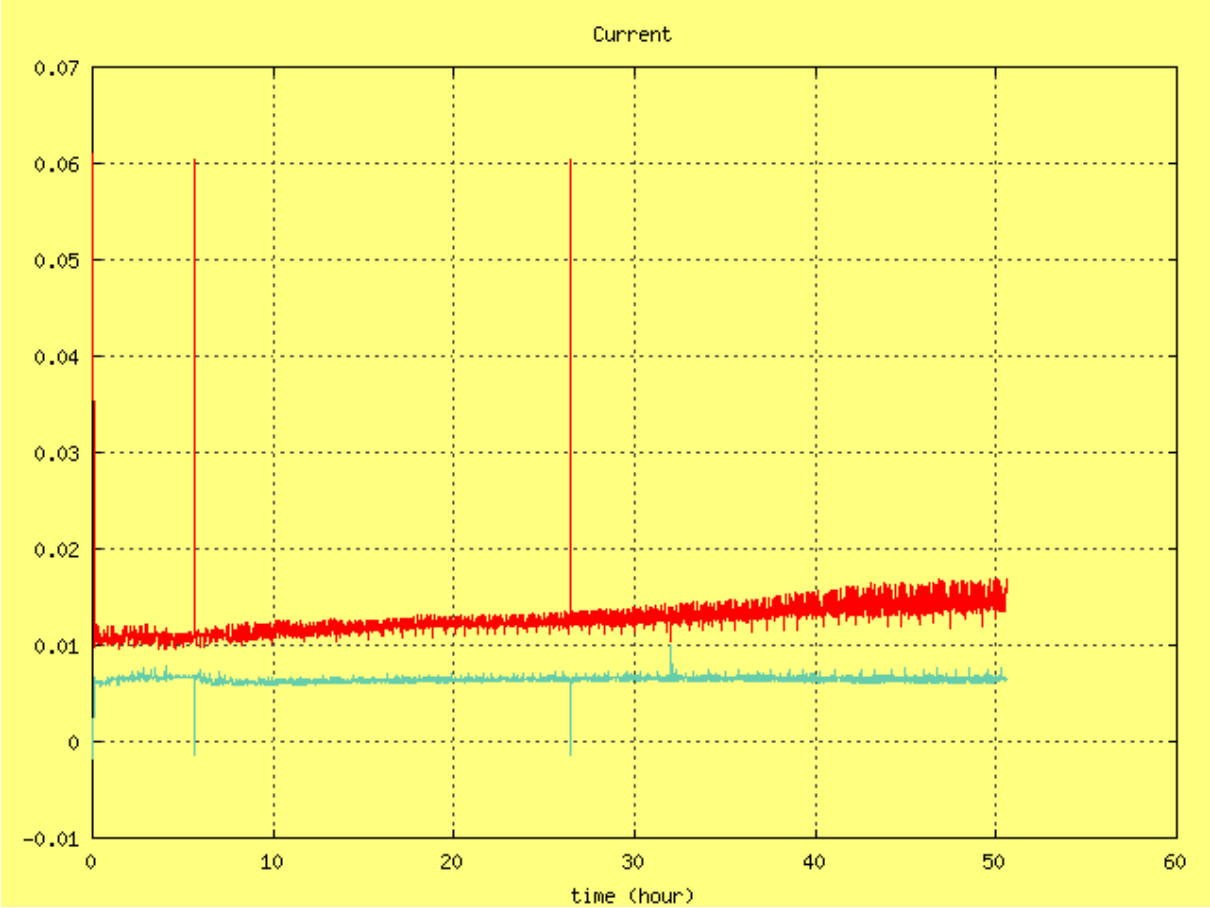
5 TEST FACILITY

Test was performed at ONERA Toulouse, using the Shepherd 2500 CO-60 source.
Dose rate could be set between 15 to 40 krads(Si) per hour.

6 RESULTS

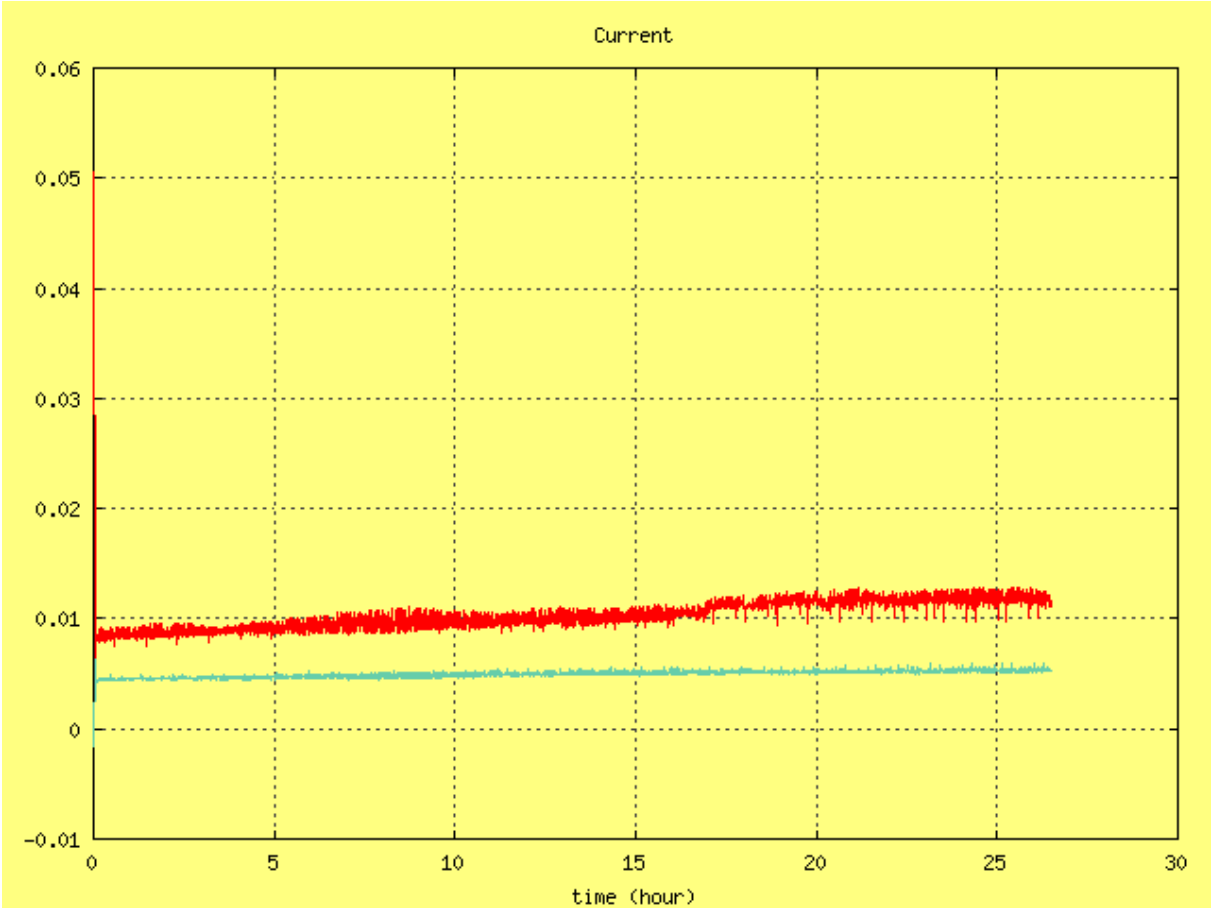
the 4 samples tested passed all functional checks of the 2 memory cuts and no bit error could be detected at any measurement step (see Test plan).
On the 2 samples which have been submitted to annealing steps, the 2 DUT current supplies values did not change between the final irradiation step at 1Mrad(Si) and after the annealing at ambient but recovered the initial value after the 168 hour annealing at 100°C.

In situ current monitoring results are provided for the 4 samples in Figure 1 to Figure 4.



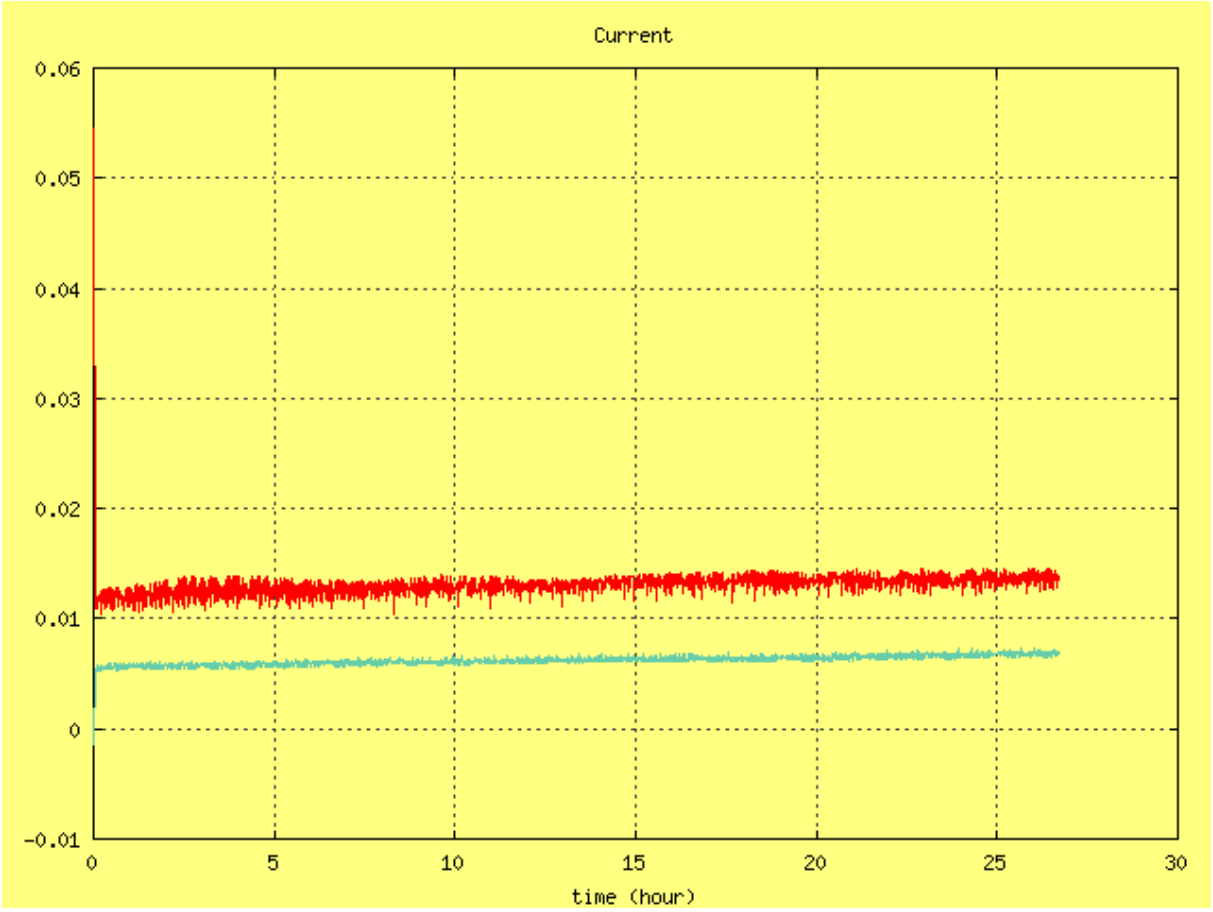
DUT supply current variation versus exposure time. (Max (red) and min (blue) values are plotted on the figure. One can see the current peak related to the DUT power-on at the beginning of each exposure step (0, 100 and 500krads).

Figure 1 – In-situ current measurement versus exposure time (Sample No1).



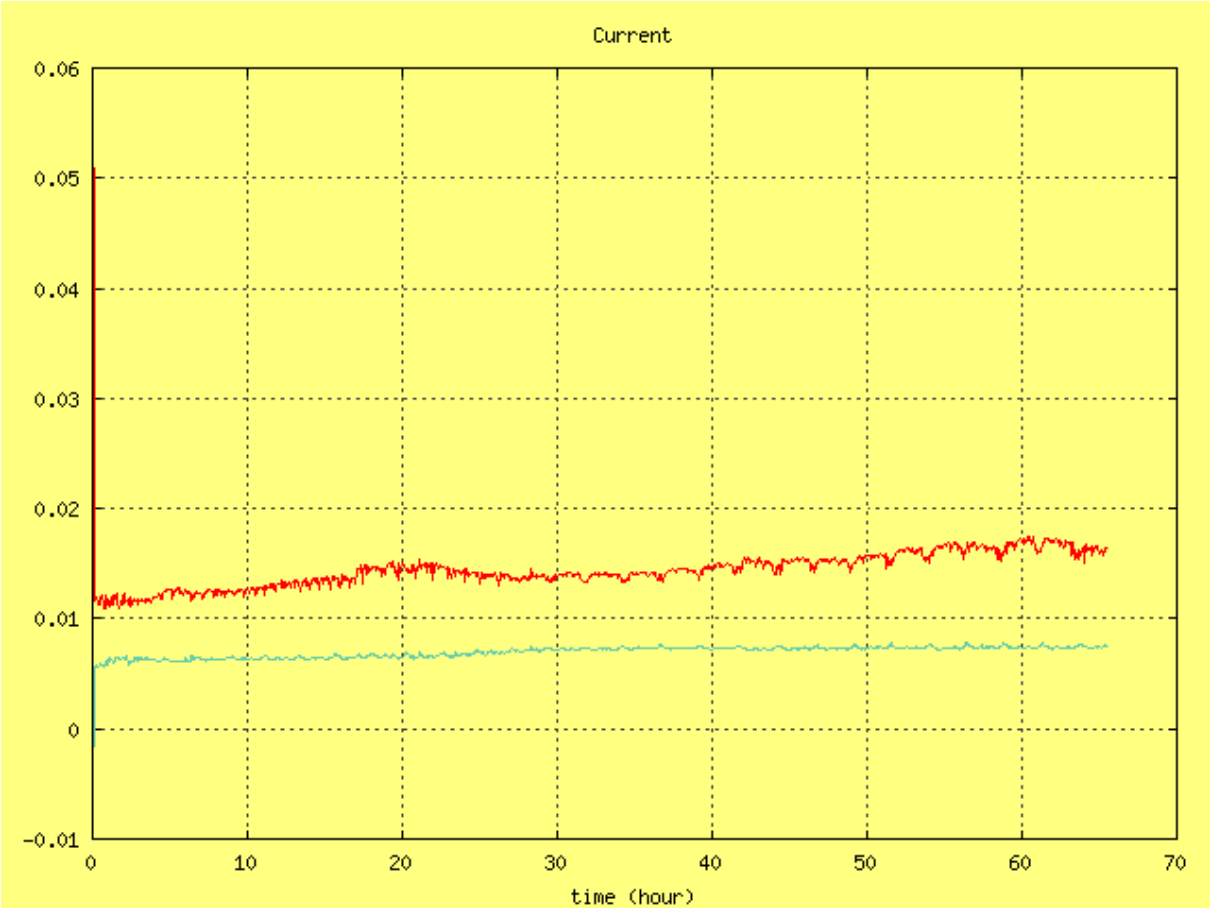
DUT supply current variation versus exposure time. (Max (red) and min (blue) values are plotted on the figure.

Figure 2 – In-situ current measurement versus exposure time (Sample No2).



DUT supply current variation versus exposure time. (Max (red) and min (blue) values are plotted on the figure.

Figure 3 – In-situ current measurement versus exposure time (Sample No4).



DUT supply current variation versus exposure time. (Max (red) and min (blue) values are plotted on the figure.

Figure 4 – In-situ current measurement versus exposure time (Sample No6).

7 CONCLUSION

A Total Ionizing Dose assessment was carried out by Hirex Engineering under STMicroelectronics contract on two memory cuts of NPSE Test chip.

4 samples were exposed to radiation using a dose rate between 15 and 40 krads(Si) per hour at room temperature up to a cumulative dose of 1Mrads.

DUT supply current has been plotted for the total exposure time for each sample.

Moreover the two cuts under consideration (see 3.1) were found to be fully functional after being exposed to a cumulative dose of 1Mrads(Si) for the 4 samples.

DUT Current supplies recovered initial values after 168 hour annealing at 100°C (2 samples annealed).

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