ESA-CNES
deep sub micron program
ST 65nm

ESCCON 2013
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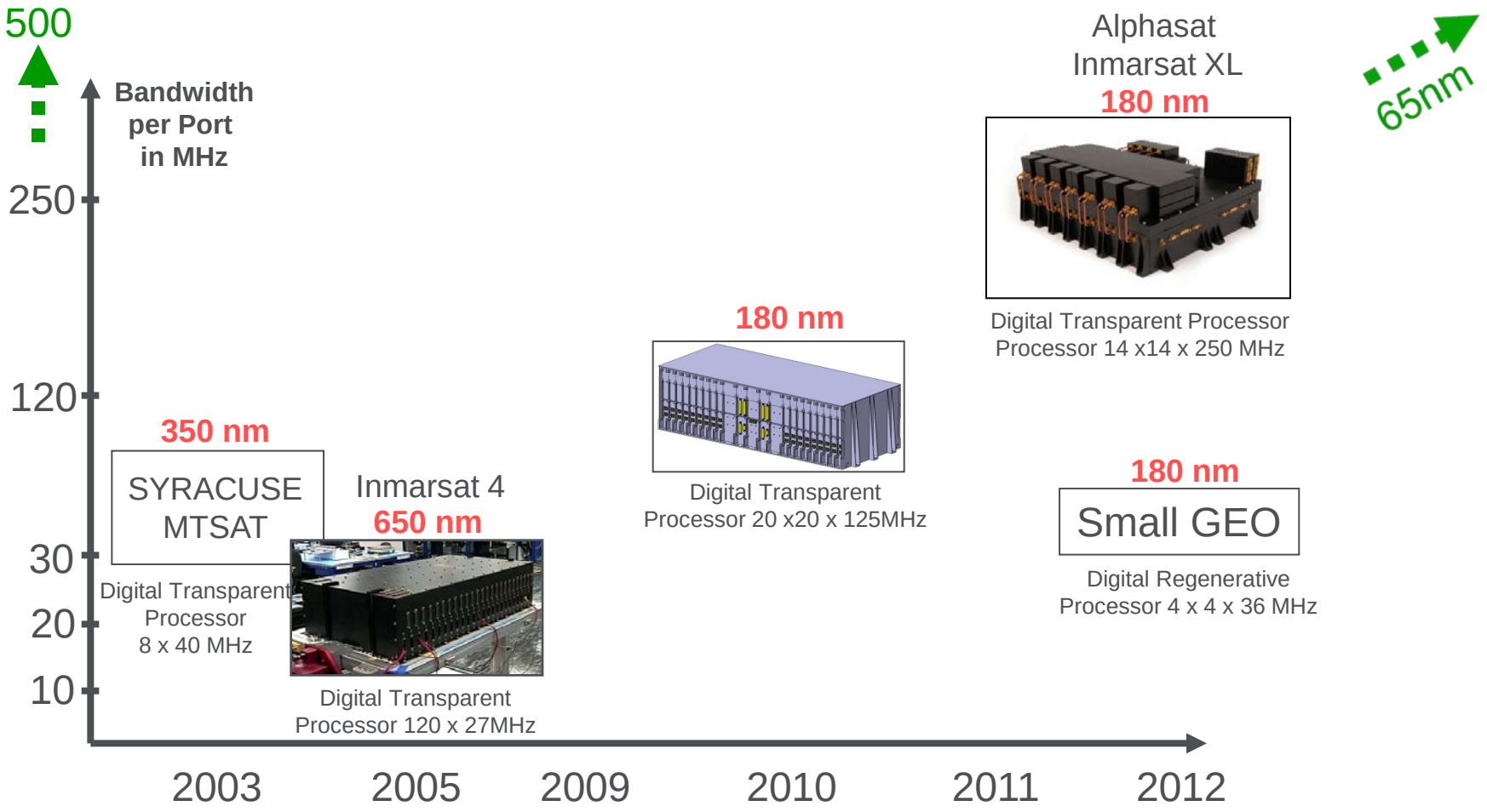
Agenda

- **Motivation for DSM program**
- Rad Hard library development
- High speed serial link development
- PLL development
- Test vehicles
- Conclusion

Digital telecom processors trend



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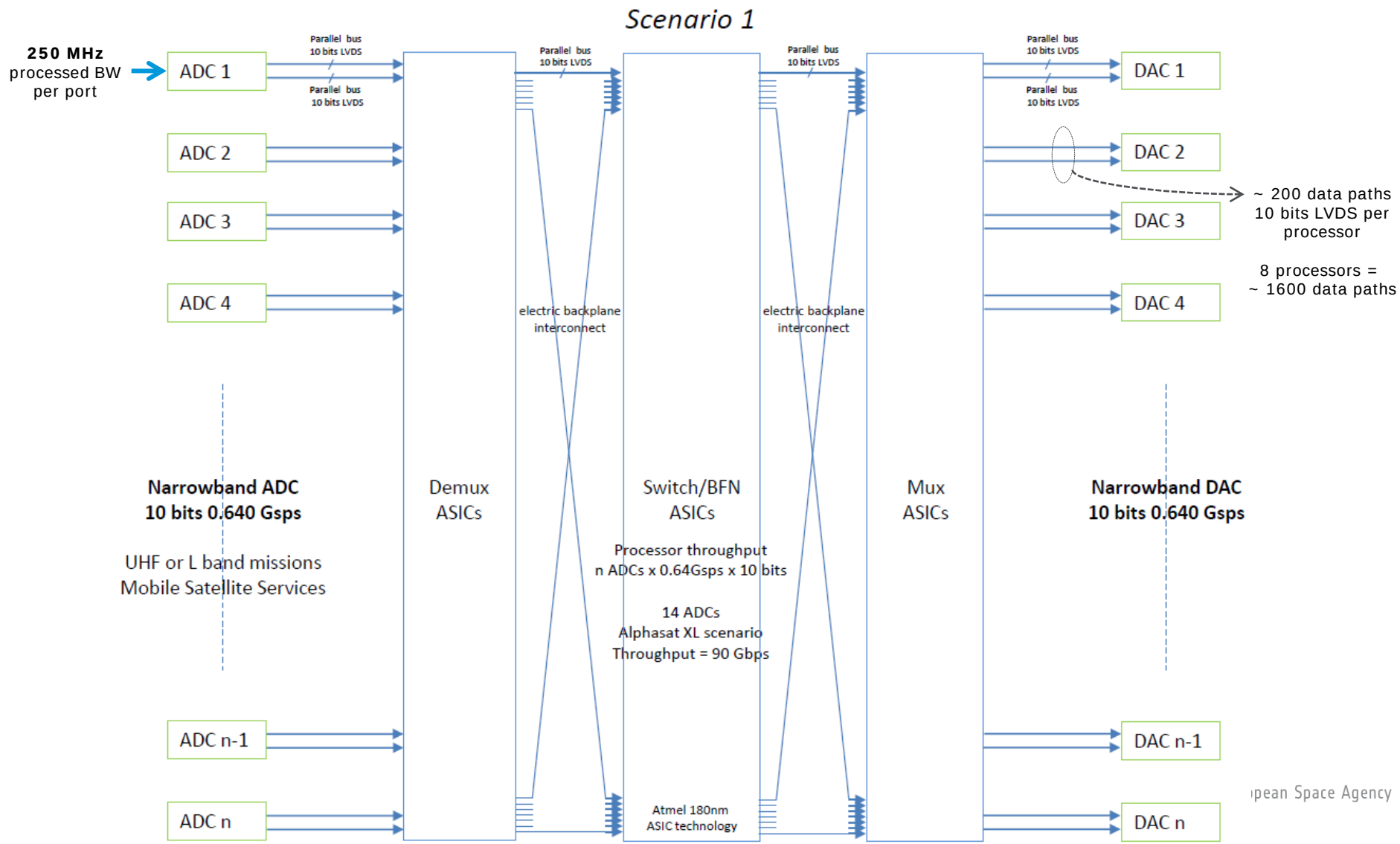
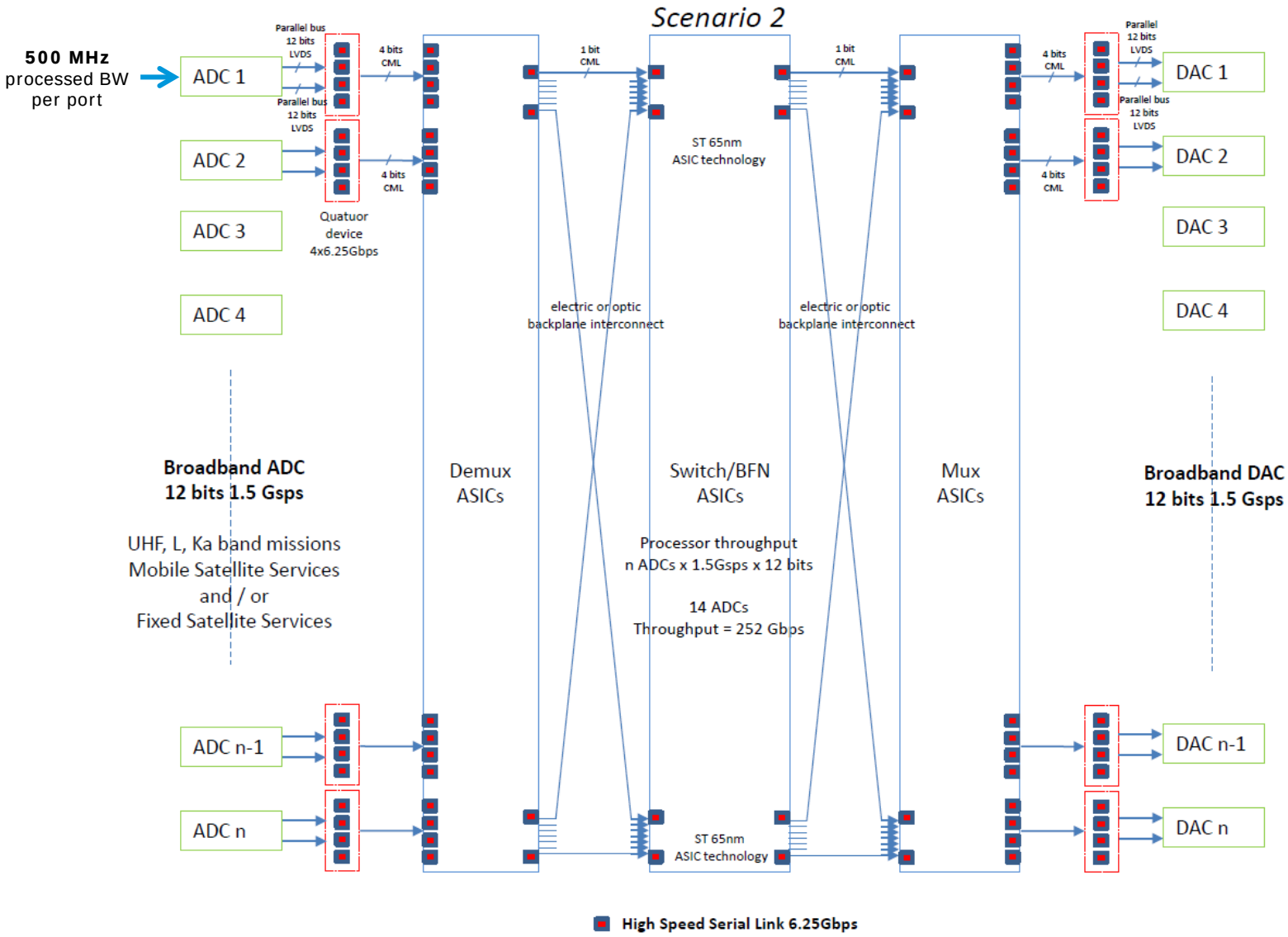
Current narrowband processor architecture with parallel busses interconnect



Future broadband processor architecture with high speed links interconnect



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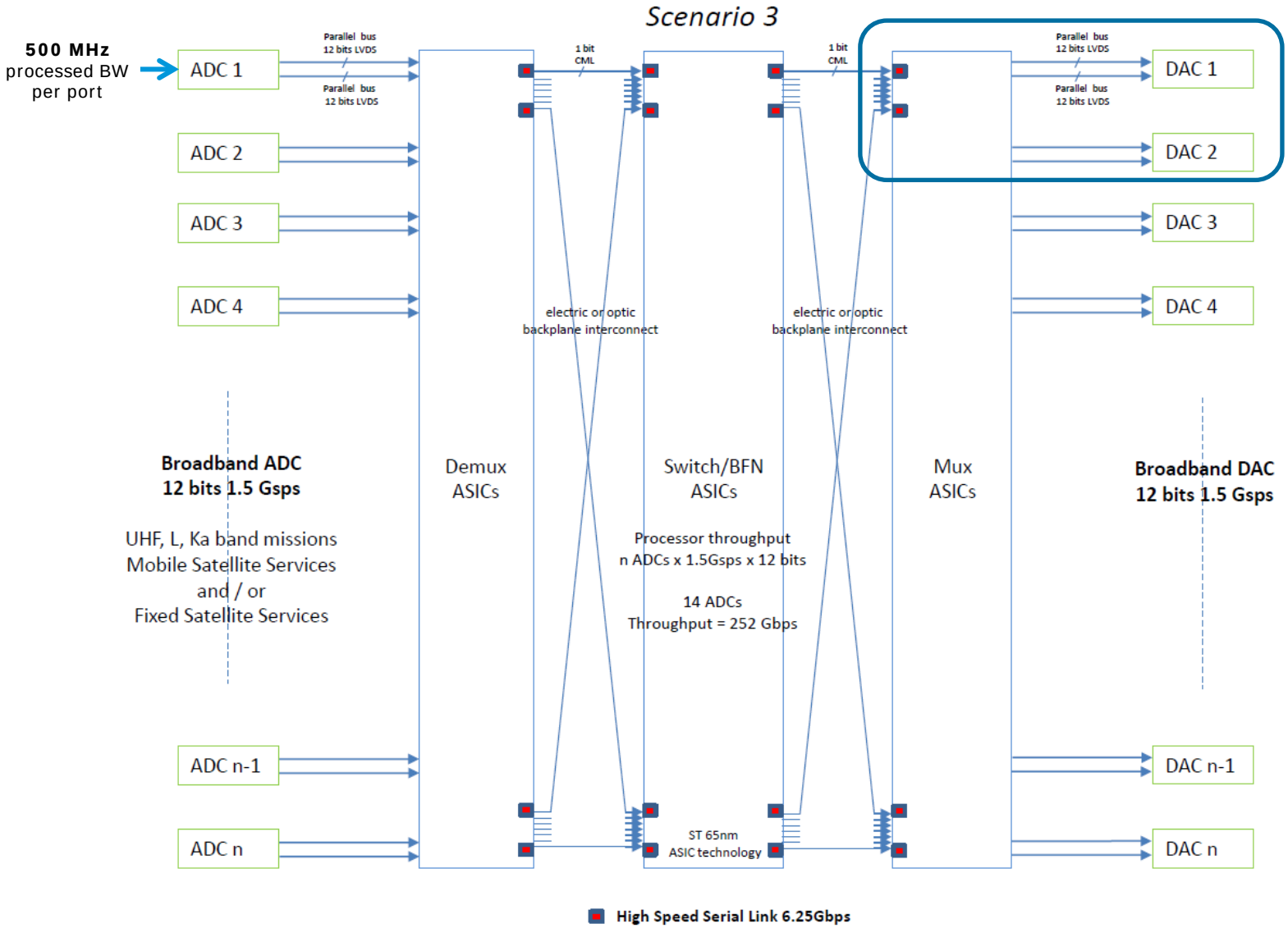
Future broadband processor architecture hybrid parallel-high speed links interconnect



HSSL interfaces as an enabling technology for processor modularity and scalability

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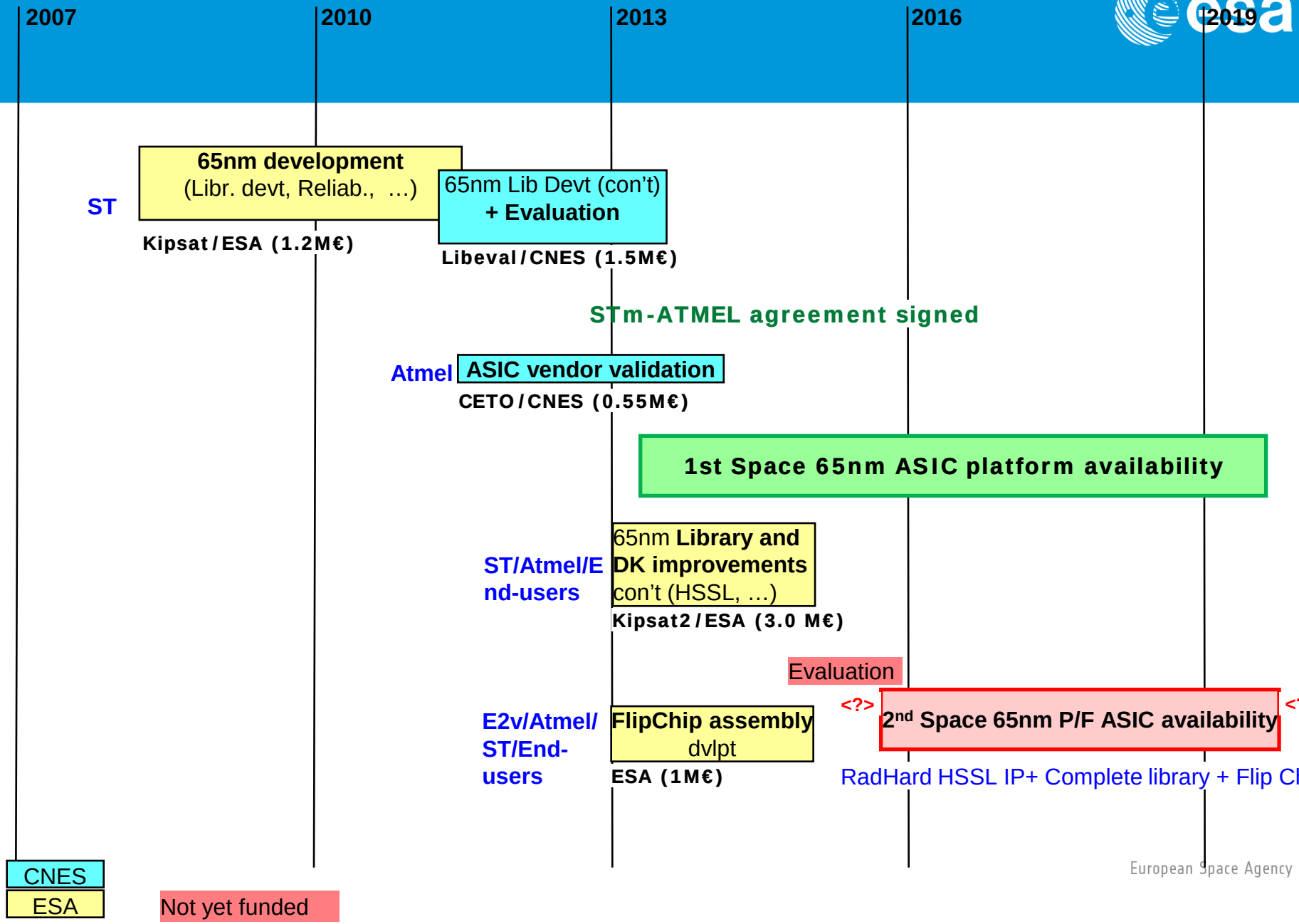
65 nm DSM program : Development Plan



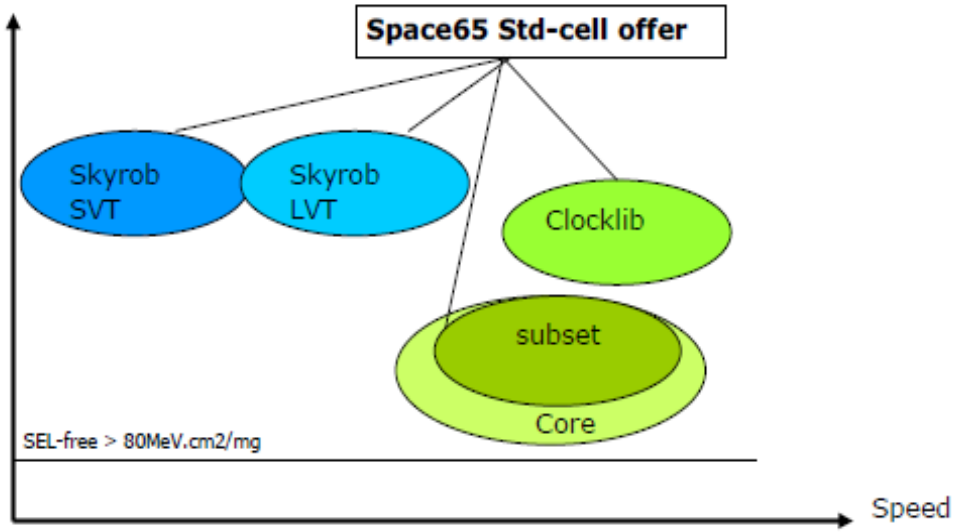
ST 65nm commercial process

- 65nm-LP CMOS from ST France : European technology, ITAR free
- 65nm CMOS commercially qualified in 2007
- 65nm CMOS Core Process :
  - Dual / Triple Gate Oxides
  - Dual / Triple Threshold Voltages for MOS Transistors
  - 7-9 Full Copper Dual Interconnect Levels
  - Low K

- performances:
  - 750 kgates/mm2
  - 2GHz stdcells
  - 5.7nW/(MHz x gates)
  - 1.25-7.5GBit/s HSSL modules

❖ ST Rad Hard offer based on CMOS 65nm-LP commercial process
❖ Reliability and Radiation maximisation performed at design stages

ST 65nm rad hard library



ST technology readiness definitions

MAT5: Product specified
MAT10: Product validated in CAD
MAT20: Silicon following specification and CAD
MAT30: Silicon following specification and CAD after aging tests

- **SKYROB65LPSVT** – radiation hardened library based on standard Vt transistors. SEU/SET improved by a factor ~ x100 compared to the commercial cells (CORE65LPSVT). Cells fully characterised under heavy ions during RADEF test campaign in December 2010. ST MAT20 (cells manufactured and characterised)
- **SKYROB65LPLVT** – duplication of the previous library with low Vt transistors (faster). Cells fully characterised under heavy ions in Q2-2012 under CNES LIBEVAL contract.
  ST MAT20 (cells designed and characterised)
- **CLOCK65LPSVT** – Clock-tree cells designed to mitigate duty cycle distortion on clock trees networks; this library is ST MAT30 (mass production)
- **CORE65LPSVT** – library offering a wide range of combinational and sequential cells for area/power optimisation, without specific radiation hardening; this library is ST MAT30, ready for mass production – only a subset of this library is proposed. The final cell list will be based upon results of characterization on extended reliability operating points (HTOL tests CNES LIBEVAL contract).

ST 65nm rad hard library

Technology	Std cells libraries	Total Cells-drives	Target
65 nm SPACE	CLOCK65LPSVT	110	Clock Network
	CORE65LPSVT	866	General purpose
	SKYROB65LPSVT	15 (DFF) 58 (Combinatorial)	Radiation Hardened
	SKYROB65LPLVT	15 (DFF) 58 (Combinatorial)	Radiation Hardened
	PRHS65	154	Place & route cells

- All cells latchup immune (characterised up 80Mev)
- Rad Hard cells, SEU rate enhanced by a factor ~ 100 compared to commercial cells
- Library cells ageing models extended to 20 years (Space library)
- Ageing models sustaining temperature ranges from -40°C to +125°C Tj
  Extreme corners simulations supported:
  MAX (125°C Tj/Process Slow/Voltage MIN/20 year ageing)
  MIN (-40°C Tj/Process Fast/Voltage MAX/0 year ageing)
- -55°C measurements carried out under CNES contract LIBEVAL on test-chips
- 20 years at 110°C Tj reliability verified under CNES contract LIBEVAL on test-chips
- Design flow based on CAD commercial tools is available

ST 65nm rad hard library
Hardened DFF characterisation

"SEU rate improvement factor with SKYROB ranging from 80 to 500"

	Cell type	library	Upset rate in GEO (SEU/bit/day)	Improvement factor compared to standard commercial DFF		description
				best	worst	
	Standard DFF from CORELIB with latchup protection (DNW)	CORE65LPSVT (Standard Vt = Slow)	1.6E-7 (best)	x	x	Reference DFF (commercial lib - CORELIB)
	Standard DFF from CORELIB with latchup protection (DNW)	CORE65LPLVT (Low Vt = fast)	4.1E-7 (worst)	x	x	Reference DFF (commercial lib - CORELIB)
✓	SKYROB65_LSDGURFD 12_DFPQX6	SKYROB65LPSVT (Standard Vt)	0.812E-9	197	**504**	Harden DFF with drive 6. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
	SKYROB65_LSDVURDF 12_DFPQX3	SKYROB65LPSVT (Standard Vt)	0.896E-9	178	457	Harden DFF with drive 3. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
✓	SKYROB_LSDGFD12S_ SDFPRQTX10	SKYROB65LPSVT (Standard Vt)	1.23E-9	130	333	Harden DFF with drive 10. Scan-out D flip-flop with 1 phase positive edge clock, reset active low, Q and TQ outputs
	SKYROB_LSDVFD12V_ DFPQX9	SKYROB65LPSVT (Standard Vt)	1.45E-9	110	282	Harden DFF with drive 9. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
✓	SKYROB_LSDGFD12S_ DFPQX18	SKYROB65LPSVT (Standard Vt)	1.82 E-9	87	225	Harden DFF with drive 18. D-type flip-flop with 1 phase positive edge triggered clock, Q output only
	SKYROB_LSDGFD12DP _DFPQX10	SKYROB65LPSVT (Standard Vt)	1.98E-9	**81**	207	Harden DFF with drive 10. D-type flip-flop with 1 phase positive edge triggered clock, Q output only

✓ Cells selected to be integrated in the final offer

Data computed with tool web based CREME96

- GEO orbit @ solar quiet
- Shielding 100mils Aluminium
- ions up to element Z=92
- Weibull fit from experimental results at RADEF (December 2010)

ST 65nm rad hard library
Hardened DFF versus commercial DFF

	CORELIB Commercial library (reference)	SKYROB (Ultra Robust – Slow - SVT) characterised in Q4-2010	SKYROB (Robust – Fast - LVT) characterised in Q2-2012
SEU rate SEU/bit/day (Geo) shielding 100mils Al	1.6E-7 (best)	1.23E-9 x130	1.8E-9 x90
Timing Set-up + delay (ps)	536	636 ~ 20% slower	536 As fast
Area (um^2)	13	26 x2.0	23 x1.8
Energy (pJ)	2.05	4 x2.0	3.8 x1.8

Comparison with a DFFX10 cell from commercial library (CORELIB)

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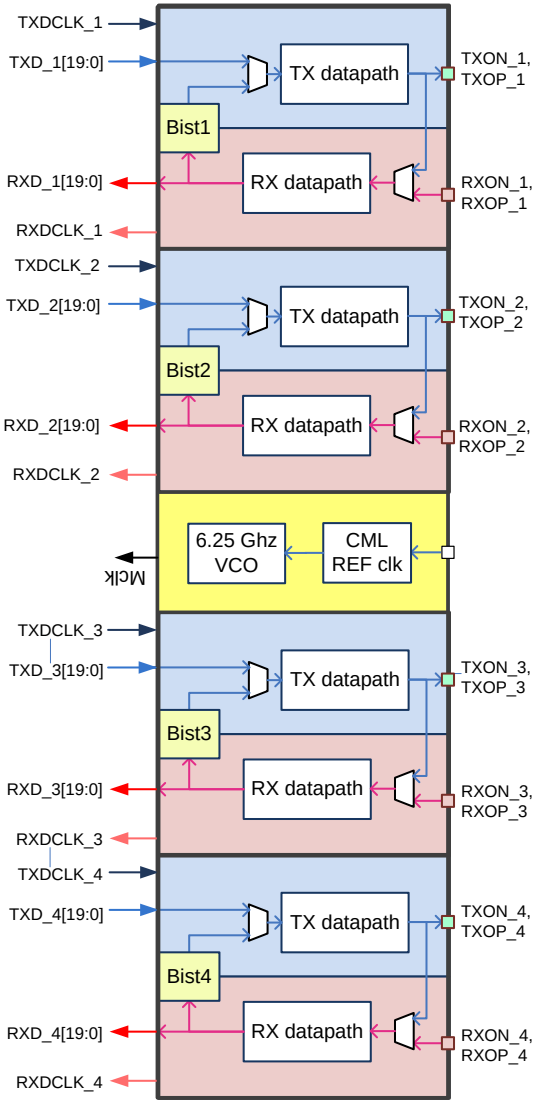
HSSL IP = 4 data slices + one clock slice



Note: data slice = Tx lane + Rx lane

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HSSL general features

- ✓ Independent TX and RX lanes throughput of 6.25 Gbps, 3.125 Gbps or 1.5625 Gbps
- ✓ BER < 10^{-14} (in terrestrial conditions)
- ✓ Independent global and per link TX & RX power downs
- ✓ Tx (or Rx) link aggregation is possible but requires external control logic for lane control and sync pattern encoding/decoding
- ✓ Programmable through a control bus
- ✓ Single 1.2V power supply
- ✓ HSSL is a CML serial communication PHY
- ✓ SPACEFIBRE codec compliancy will be analysed in 2013
- ✓ HSSL will be delivered as an IP part of ST 65nm Rad Hard offer
- ✓ HSSL will be provided as a Flip chip ready layout IP (hard macro)

- ✓ Rad hardening targets:
  - ✓ Minimize BER sensitivity under Heavy Ions
  - ✓ No Single Event Functional Interrupts (SEFIs):
    - ✓ Self recovery of Single Event Transients (SETs) and Single Event Upsets (SEUs) in the signal processing path
    - ✓ TMR protection on configuration registers
  - ✓ Full immunity to Single Event Latch-up (SEL) failures for the IP and the whole Test Vehicle versus Heavy Ions with a LET up to 80MeVcm2/mg, at 125°C Tj and maximum voltage supplies values

Clock slice & TX features

Clock slice:

- ✓ Very stable internal clock based on LC VCO frequency synthesizer
- ✓ 156.25 MHZ CML AC coupled external differential reference clock

TX data lane:

- ✓ Output: Differential CML signaling with programmable bit polarity and order inversion
- ✓ Programmable output amplitude
- ✓ Programmable 100 ohms differential terminations
- ✓ Programmable pre-emphasis
- ✓ Support up to ± 50ppm data rate offset versus reference clock frequency (plesiochronous mode)
- ✓ Programmable input word width: 20, 10 and 5 bit

RX features

RX data lane:

- ✓ Input: RX Differential CML signaling with programmable bit polarity and order inversion
- ✓ Programmable 100 ohms differential terminations
- ✓ Linear Equalizer and gain control with up to 15 dB equalization at Nyquist frequency
- ✓ Programmable output word width: 20, 10 and 5
- ✓ Separate sampler for eye mapping & extraction of ISI coefficients for equalizer adaptation
- ✓ Signal loss detection circuitry based on signal amplitude, transition density, and eye opening
- ✓ Independently configurable per link multi-rate digital RX Clock & Data Recovery (CDR)
- ✓ Support up to ± 50ppm data rate offset versus reference clock frequency (plesiochronous mode)

HSSL test vehicle: S7RADVAL

S7RADVAL : Versatile IC dedicated to electrical and under radiation characterization

Dual S7RADVAL configuration

Plesiochronous test configuration

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PLL features

Maximum Power : 26 mW
Analog Supply : 1.1V – 1.3V
Digital Supply : 1.1V – 1.3V
Input Frequency : 20MHz - 200MHz
PFD Frequency : 20MHz - 100MHz
VCO Frequency : 200MHz - 1200MHz
Output Phases : 6 (60 degrees apart)
Pk-pk Period jitter : +/-60ps@200MHz output

HIGHLIGHTS

Rad-hard 1.2V PLL (for both analog and digital supplies)
Programmable VCO frequency with
Very wide VCO frequency Range
6 equidistance output clock phases
Supports clock de-skew (with delay up to 4ns)
Digital lock detection for coarse frequency lock
Analog lock detection for fine phase lock

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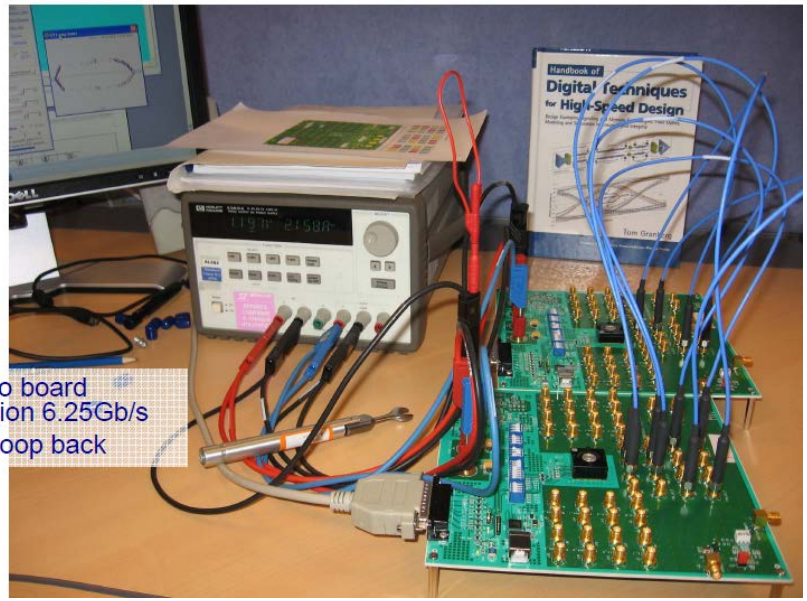
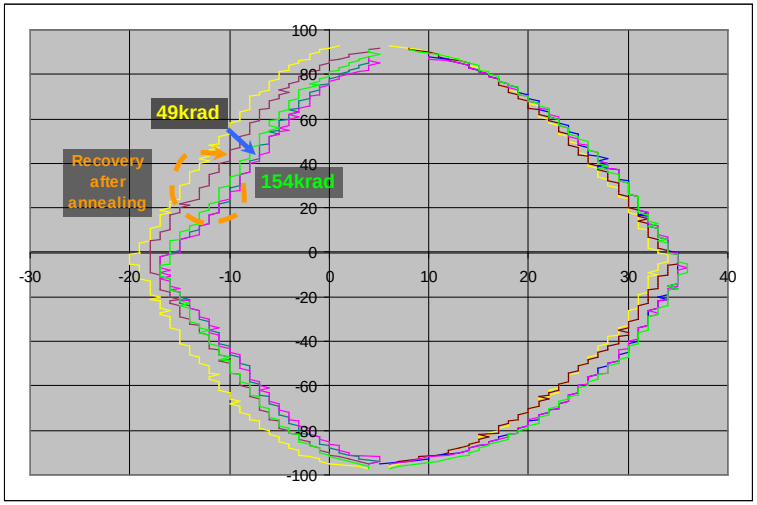
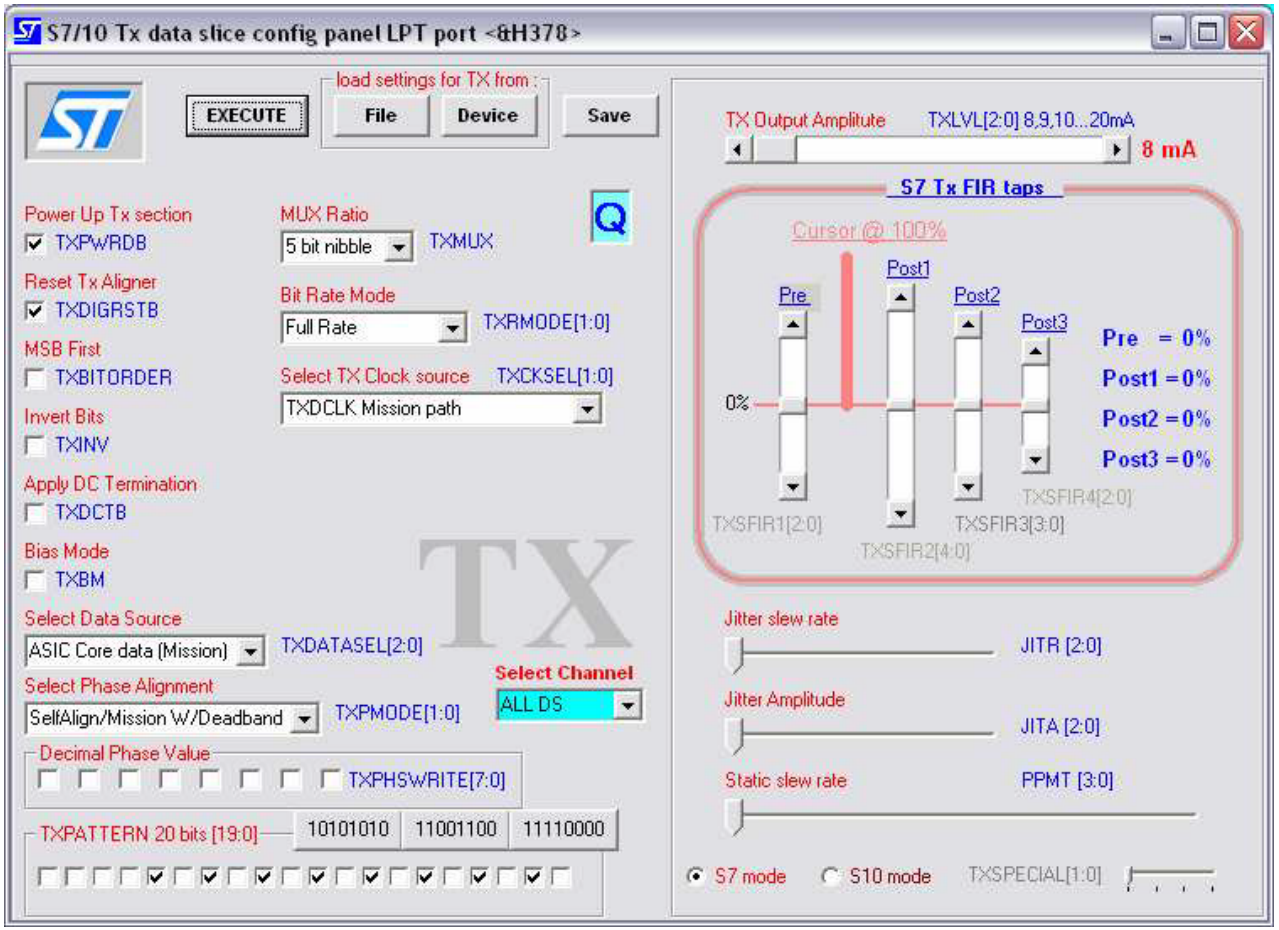
High speed serial link characterisation on Quatuor test vehicle



Receiver eye diagram opening
TID test campaign performed at
ENEA December 2009
Device fully operational at 300 Krads
+
heavy ions test campaign performed at
RADEF December 2010
(ESCC 25100 guidelines)



Quatuor configuration software (GUI)



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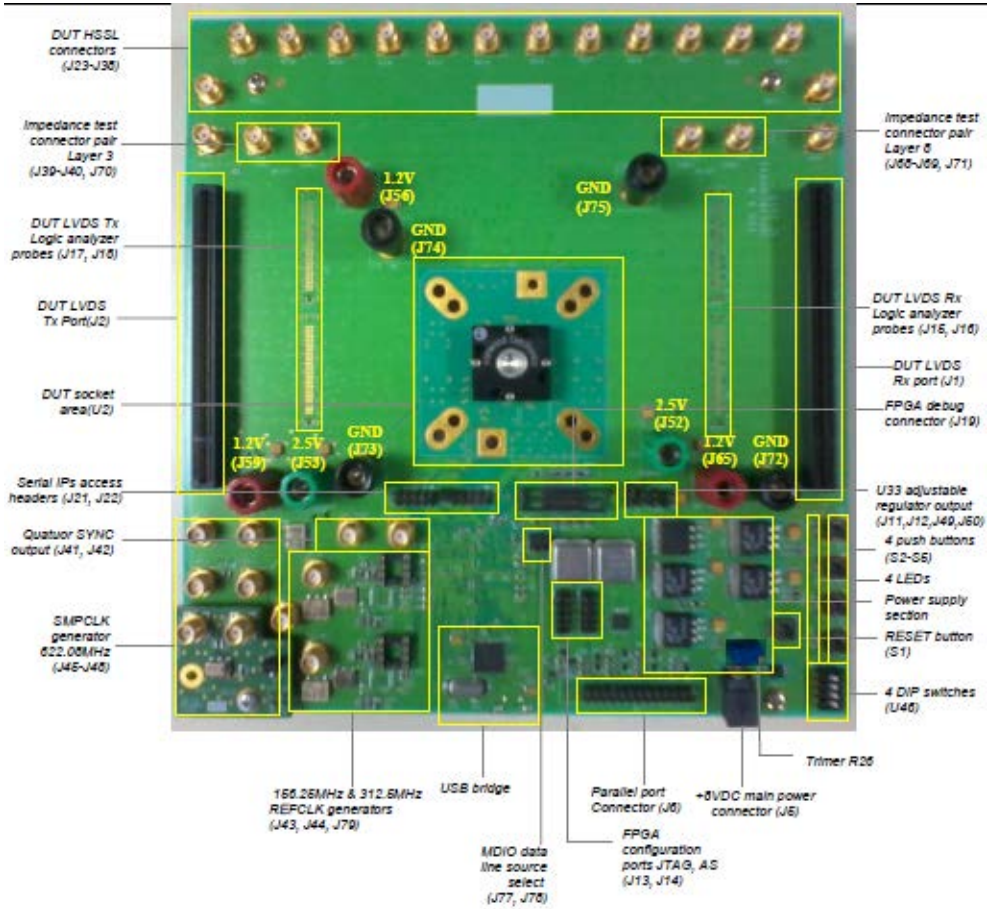
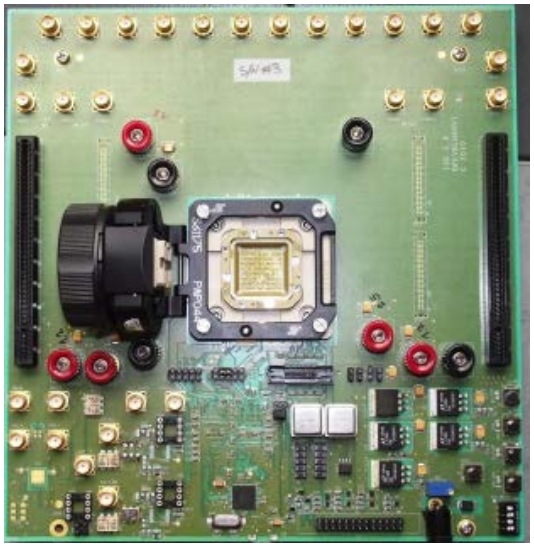
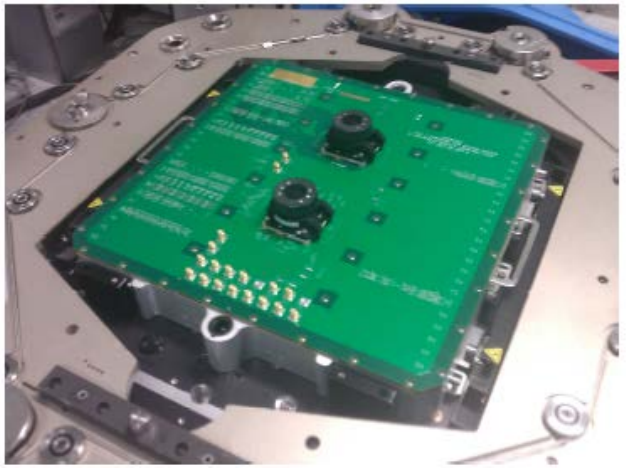
High speed serial link validation boards



Quatuor electric characterisation board



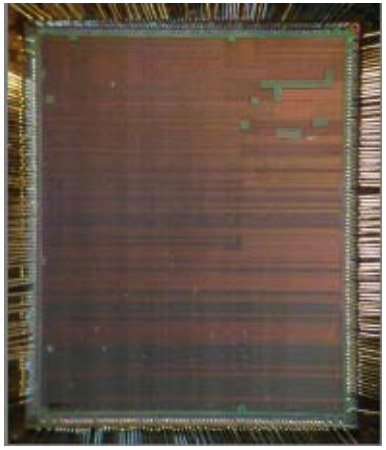
Quatuor radiation & reliability characterisation board



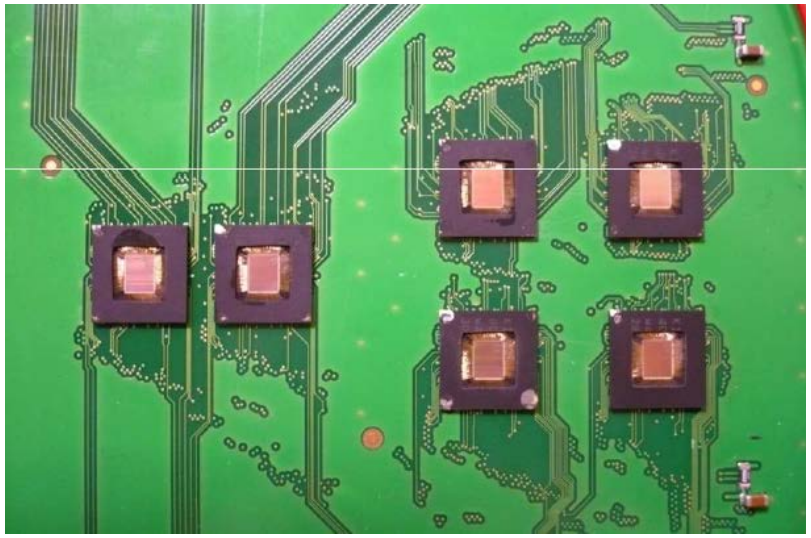
Quatuor automated test equipment board (ATE)
ST Integraflex tester

ST 65nm rad hard library radiation validation board

"Key IP SAT" 1.0 layout (KIPSAT)



KIPSAT 1.0 die (~ 24 mm^2)



KIPSAT radiation test board
heavy ions test campaign RADEF December 2010

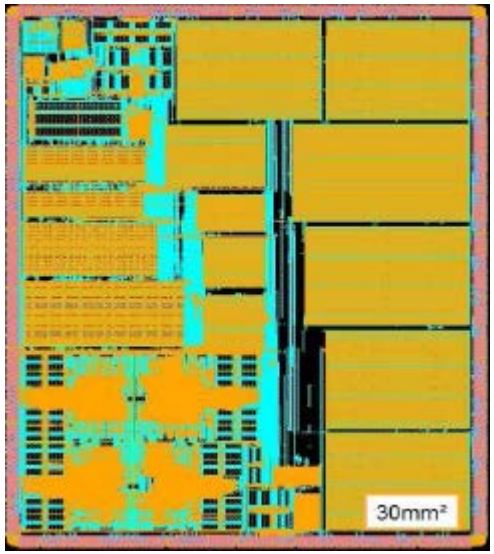
KIPSAT 1.0 main features

- 7 shift registers (40k and 80k DFFs)
- 4 ECC SRAMs with different MUX ratio (4, 8, 16)
- 1 TMR shift register (120k DFFs)
- 1 CAD modelling block (library silicon correlation)

ST 65nm test vehicles already characterised ESA-CNES contracts

TC1 (rad hard digital library - KIPSAT1.0):

- SKYROB65 ALLCELL blocks
- SKYROB65/CORE65 ROs
- FF shifters SKYROB65LP
- SRAM compilers
- Application digital blocks

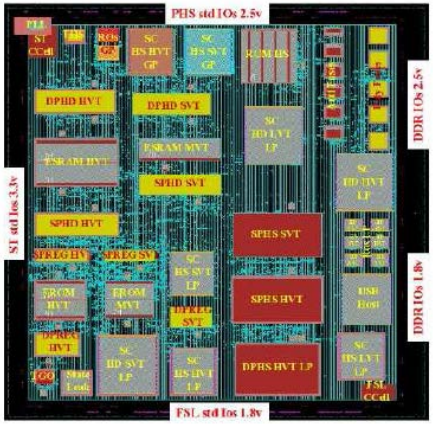


TC2 (rad hard IOs and PLL):

- high performance multiphase hardened PLL covering frequency range from 50MHz … 1.2 GHz (6 phases)
- special IOs
  - cold spare CMOS
  - cold spare LVDS
  - Signal
  - I2C

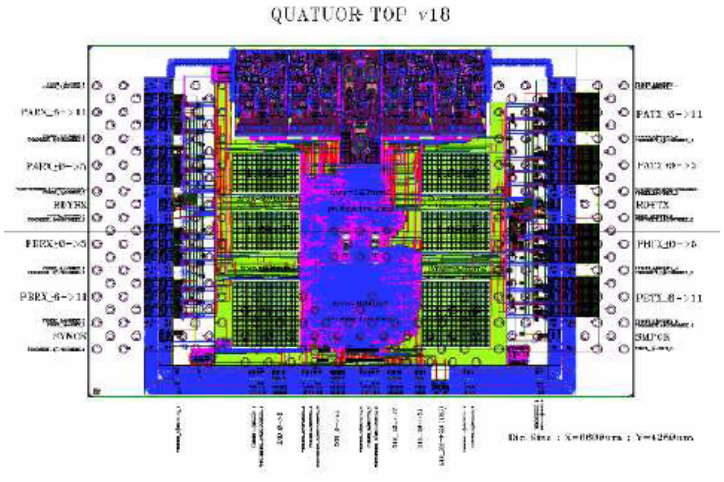
TC4 (C65 commercial libraries):

- commercial library full set (~ 1000 cells)



TC3 (high speed serial link / HSSL):

- Quatuor / 4 x 6.25 Gbps



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Conclusion

- ✓ Technology developments will continue in 2013 & 2014
  - ✓ DSM Phase2.1
    - improvement of Rad Hard standard cells offer
    - development of a second PLL
    - CAD flow validation
  - ✓ DSM Phase2.2
    - completion of hardened HSSL IP
    - definition of HSSL standalone product (ASSP)
- ✓ ST-Atmel partnership settled
  - ✓ Contract signed in Q4-2012
  - ✓ Wafers supply agreement signed in Q1-2013
  - ✓ ST design kit enablement at Atmel premises done in February 2013
  - ✓ Atmel will be the commercial interface with Space Customers
  - ✓ Atmel will provide the design kit to Space Customers
  - ✓ Atmel will provide ASIC services (layout and back end flow)
- ✓ Deployment to Alpha users effective in 2013 (Telecom applications)
  - ✓ Thales France
  - ✓ Astrium UK
- ✓ First “tape out” planned in Q4-2013

Conclusion / perspectives

- ✓ DSM 65nm is an enabling technology the next generation telecom processors (broadband digital)
  - ✓ Thales France
  - ✓ Astrium UK
- ✓ However many other applications may benefit as well from advances made thanks to DSM 65nm
  - ✓ Next generation FPGA
  - ✓ Next generation micro processor / micro controller
  - ✓ Next generation DSP processor
  - ✓ Space Fibre (successor of Space Wire)

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THANK YOU ☺