

The NASA Electronic Parts and Packaging (NEPP) Program – Parts, Packaging, and Radiation Reliability Research on Electronics

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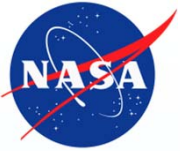
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Co- Managers, NEPP Program

NASA/GSFC

<http://nepp.nasa.gov>

Unclassified



Outline

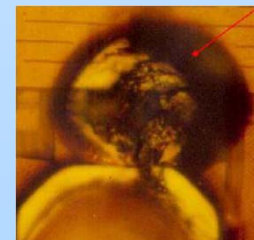
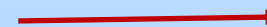
- **Overview of NEPP**
 - What We Do and Who We Are
 - Flight Projects
 - Technology
 - Working With Others
- **Recent Highlights**
- **Plans for FY13**
- **Challenges**
- **Summary**



NEPP – What We Do

- **NEPP provides two prime functions for NASA**
 - Assurance infrastructure for NASA
 - Research on advanced/new electronic devices and technologies
- **We work with**
 - Active and passive semiconductors
 - Electronic device packaging
 - Radiation effects on electronics
- **We collaborate with others in technical areas such as**
 - Workmanship
 - Alert systems
 - Standards development and maintenance
 - Engineering and technology development
- **We provide an *independent* view for the safe use of electronic integrated circuits for NASA**

Electrical overstress failure
in a commercial electronic device





NEPP's Two Functions

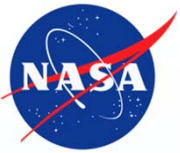
- **Assurance**
 - Customer: *Space systems in design and development*
 - **Issues applicable to currently available technologies (aka, mature technologies)**
 - **Examples**
 - Cracked capacitors
 - Power converter reliability
 - **NASA Electronic Parts Assurance Group (NEPAG) - a subset of NEPP**
 - Communication infrastructure
 - Audit and review support
 - Investigation into reported failures (when of potential wide-reaching impact to NASA flight projects)
- **Advanced/new electronics technology research**
 - Customer: *Space systems in early design or conceptualization*
 - **Issues applicable to new technologies (or those with potential Mil/Aero applicability)**
 - **Examples**
 - Commercial field programmable gate arrays (FPGAs)
 - Sub 32nm electronics
 - **Technology evaluation**
 - **Development of test methods and qualification recommendations**



NASA EEE Parts Assurance Group (NEPAG)

- Formed in 2000
- Weekly Telecons
 - Typical participation ~ 25
 - Share knowledge and experience
 - Address failures, requirements, test methods
 - Monthly international
- Audit support
- Coordinate specification and standards changes





NEPP and NASA Flight Projects

NEPP

- Works general device qualification standards
- Develops the knowledge-base on **HOW** to qualify a device used by flight projects
 - Test methods
 - Failure mode identification
 - User guidelines and lessons learned
- Works issues that are relevant across NASA

Flight Projects

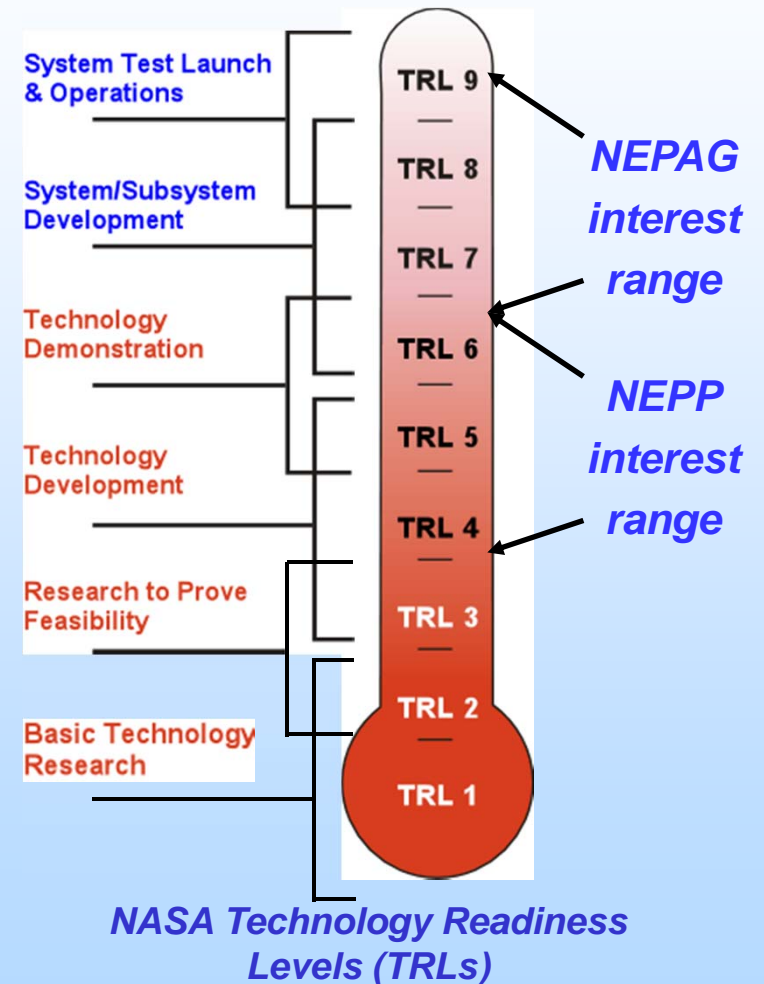
- Work mission specific requirements
- Qualify a device to mission requirements or to a standard
 - Uses NEPP knowledge to perform qualification
- Work issues relevant to a specific project

NEPP provides products for use by flight projects



Maturity of Technology – *The NEPP Model*

- NASA flight project timelines are insufficient to learn how to qualify a new technology device
 - *Sufficient time may exist to qualify a device, but not to determine **HOW** to qualify*
- For 2016 launch, technology freeze dates are typically 2013 or earlier
- Technology development and evaluation programs need to be in place prior to mission design
 - **NEPP's strategic advanced planning on technology evaluation is critical to allow timely and safe flight project insertion of new technologies**





Sample NEPP Technology Challenges

Key Question: Can we “qualify” without high cost and schedule?

Silicon

- <32 nm CMOS
- new materials such as CNT
- FINFETs
- 3D ICs

Device Architectures

- system on a chip
- interconnects
- power distribution
- high frequencies
- application specific results

Packages

- inspection
- lead free
- failure analysis
- stacking

Passives

- embedded
- higher performance
- BME capacitors

Board Material

- thermal coefficients
- material interfaces



Connectors

- higher-speed, lower noise
- serial/parallel
- ruggedized, electro-optic

Power Conversion

- widebandgap devices
- distributed architecture
- thermal modeling
- stability

Design Flows/Tools

- programming algorithms, application
- design rules, tools, simulation, layout
- hard/soft IP instantiation

Workmanship

- inspection, lead free
- stacking, double-sided
- signal integrity

Related areas (non-NEPP)



Sharing NEPP Knowledge

- **NEPP success is based on providing appropriate guidance to NASA flight projects**
 - Interaction with the aerospace community, other government agencies, universities, and flight projects is critical.
- **NEPP utilizes**
 - NEPP Website: <http://nepp.nasa.gov>
 - NEPP 4th Annual **Electronics Technology Workshop (ETW)**: Week of June 10th 2013
 - Standards working groups
 - Telecons (NEPAG weekly and monthly international)
 - Documents such as Guidelines, Lessons Learned, Bodies of Knowledge (BOKs)



Consortia and Working Groups

- **NEPP realizes the need to work in teams to provide better and more cost-effective solutions**
- **NEPP utilizes working groups for information exchange and product development**
 - **External examples:**
 - JEDEC commercial electronics and TechAmerica G11/12 Government Users
 - **Internal (NASA-only) examples:**
 - DC-DC converters, point-of-load convertors, GaN/SiC, and connectors
- **NEPP supports university-based research when funds allow**



NEPP Recent Highlights (1 of 2)

- **Continued leading Qualified Manufacturer's List (QML) MIL-PRF-38535 Class Y development**
- **Released documents:**
 - **Single event effects (SEE) Test Guideline for FPGAs**
- **Firsts and significant results**
 - **1st data on helium leak intercomparison study**
 - **Base metal electrode (BME) reliability data – positive results**
 - **Combined radiation/reliability tests of GaN devices, DDR-class and Flash memories**
 - **Radiation tests of**
 - **28nm TriGate processor (proprietary data)**
 - **32nm SOI processor (AMD)**
 - **IPad™ generation 4**
 - **Destructive SEE observed on Schottky Diodes**
 - **Independent SEE test of Xilinx Virtex-5QV**

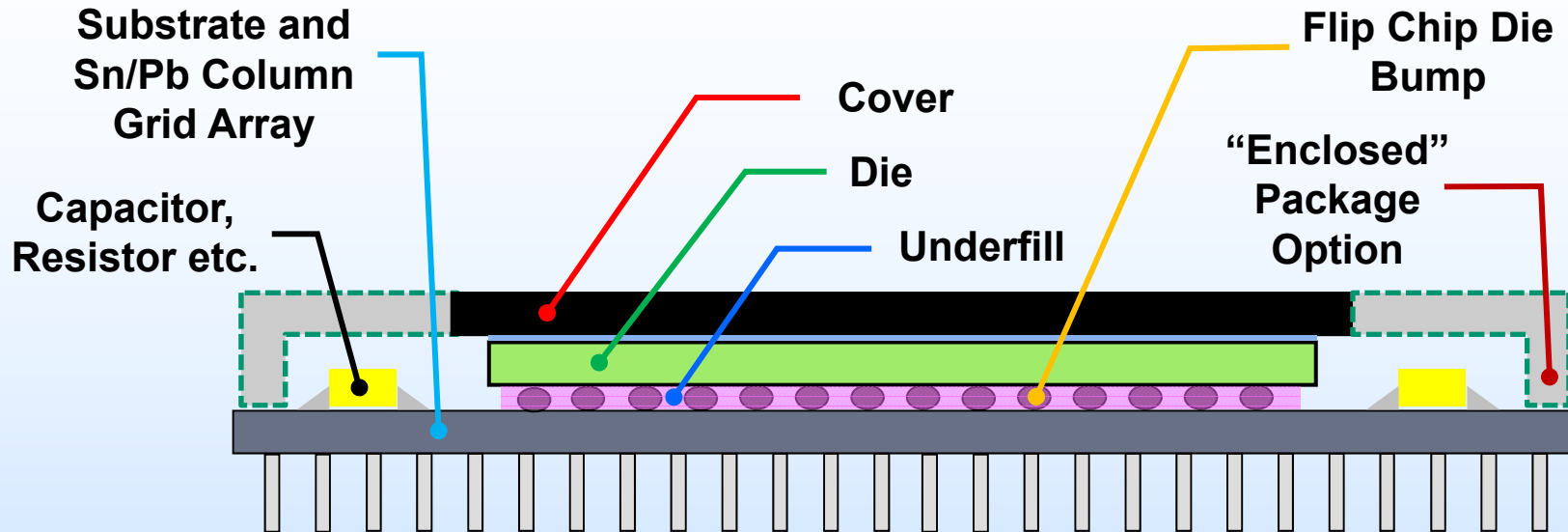


NEPP Recent Highlights (2 of 2)

- **3rd NEPP Electronics Technology Workshop (ETW) - June 2012**
 - 2.5 days of presentations
 - ~250 attendees including 50% via the web
- **Assurance Efforts**
 - Cracked capacitor evaluation
- **Recent test focuses (on-going)**
 - Power devices
 - GaN, SiC, and Si Power Device (radiation and combined effects)
 - FPGAs
 - Xilinx Virtex-5QV and Commercial Virtex-5 (radiation)
 - Underfill (reliability)
 - Point-of-load (POL) Converters



Non-hermetic IC Package, with “Space” Features(CCGA?)



Space Challenge	Some Defenses
Vacuum	Low out/off-gassing materials. Ceramics vs polymers.
Shock and vibration	Compliant / robust interconnects - wire bonds, solder balls, columns, conductive polymer
Thermal cycling	Compliant/robust interconnects, matched thermal expansion coefficients
Thermal management	Heat spreader in the lid and/or substrate, thermally conductive materials
Thousands of interconnects	Process control, planarity, solderability, substrate design
Low volume assembly	Remains a challenge
Long life	Good design, materials, parts and process control
Novel hardware	Test, test, test
Rigorous test and inspection	Testability and inspectability will always be challenges

Classy



Hermeticity Correlation Study

- **MIL-STD-750, TM 1071.8 tightened the leak rate limits for transistors and diodes**
 - Change successfully fixed inconsistent Internal Gas Analysis results and improved package integrity
 - Traditional helium mass spectrometers (HMS) were not capable of testing reliably to the tighter limits
 - New piece of equipment, the Cumulative Helium Leak Detector (CHLD) was added to 1071.8 – it is capable
 - Most manufacturers are using Krypton 85 (Kr85) radioactive tracer gas method
 - Optical Leak Testing (OLT) is also allowed for TM 1078.1
 - No correlation study for Kr85, CHLD or OLT
 - HMS to Kr85 study done ~ 40 years ago
- **Space users want to tighten MIL-STD-883, TM 1014 but manufacturers opposed**
 - NASA has HMS, CHLD (2) and Kr85 and has been doing a “round robin” comparison to support our case
 - OLT equipment manufacturer is participating



Kr85 Bomb Station



CHLD System



OLT System



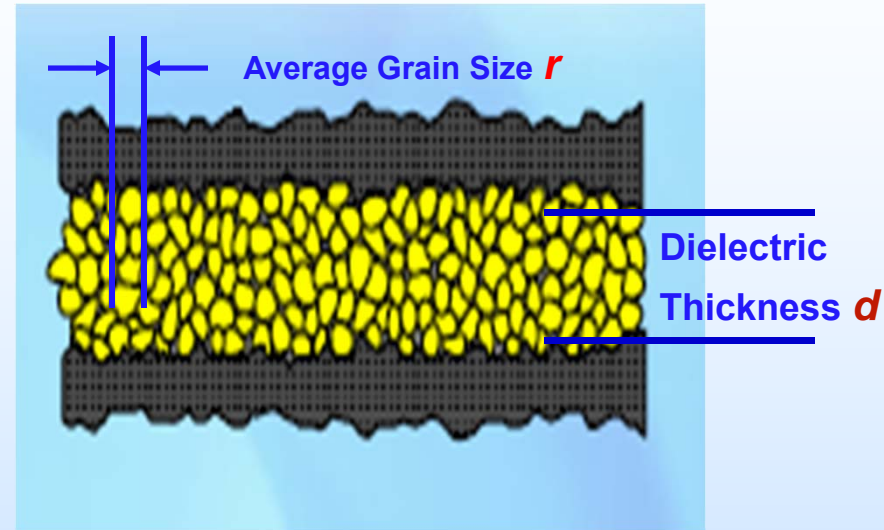
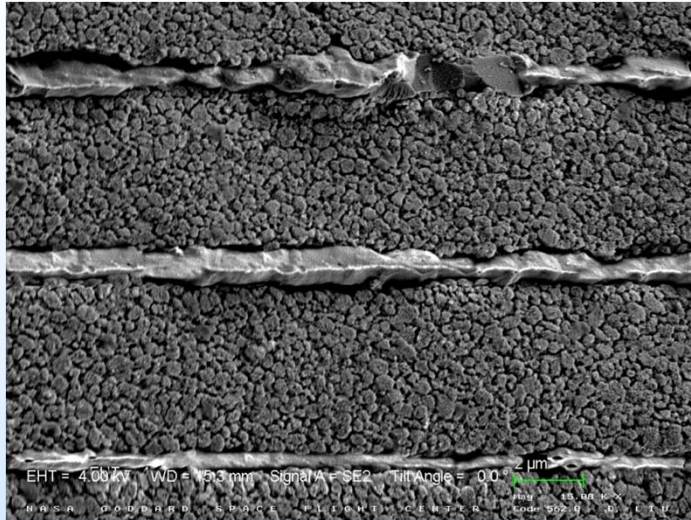
Base Metal Electrode (BME) Ceramic Capacitor Overview

- BMEs are commercial not all can be qualified for hi-rel applications.
- Requirements used for making high-reliability PME capacitors are not all applicable to BME capacitors. BME capacitors have more complicated structures than PME capacitors:
 - Number of dielectric layers N in a BME capacitor is extremely high;
 - Dielectric thickness d is extremely thin;
 - Grain size varies from 0.5 mm down to 0.1 mm.
- The reliability of a BME Multi-Layer Chip Capacitor (MLCC) has been found to be directly related to the microstructure parameter N (# of dielectric layers) and $\left(\frac{d}{\bar{r}}\right)$ (# of stacked grains per dielectric layer).
- A reliability model utilizing the microstructure of a BME MLCC has been developed and has been applied to screen out BME capacitors with potential reliability concerns.



What Determines the Reliability of a X7R MLCC?

Microstructure Parameter $\left(\frac{d}{\bar{r}}\right)$



- Important microstructure parameter for a single-layer capacitor:

$$\left(\frac{d}{\bar{r}}\right) = \text{Number of stacked grains per dielectric layer}$$

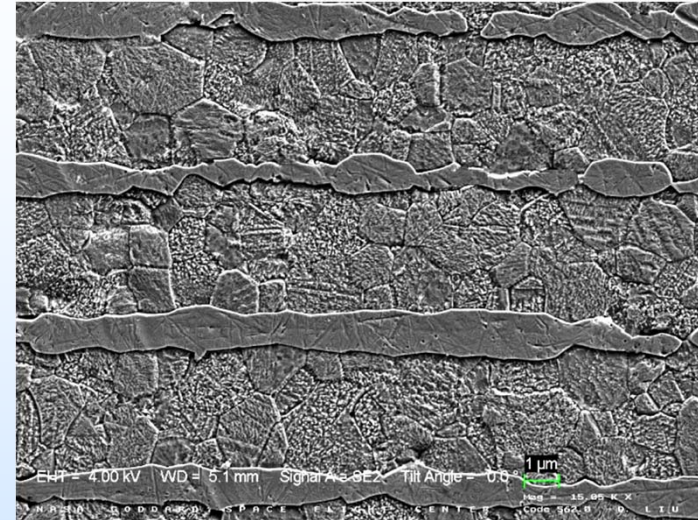
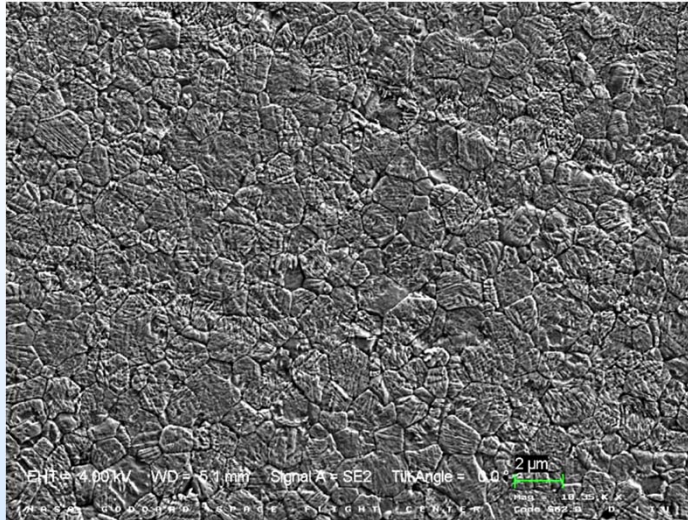


BME Ceramic Capacitors with C0G Dielectric

- **C0G (or NP0) type MLCCs are characterized by capacitance almost independent from temperature ($TCC \leq 30\text{ppm}$ from -55°C to 125°C) and frequency**
- **These BME C0G ceramic capacitors are made using a CaZrO_3 -based dielectric and Ni electrodes ($K \sim 32$)**
 - **High and stable dielectric strength allows for thin dielectric which offsets the low K to some extent**
 - **Much higher volumetric efficiency than regular C0G**
- **Dielectric aging is negligible!**
- **The dielectric is non-ferroelectric and with zero VCC and no piezoelectric effect (non-ferroelectric material)**
- **Excellent candidate for impedance match, RF tuning, temperature compensation, and possible CPU/IC decoupling**



Excellent Microstructures



- **Cross-section SEM photos reveal an excellent microstructure with dense, uniform grain structure**
- **CaZrO₃-based dielectric is highly reduction-robust (no oxygen vacancy concerns)**
- **Very good processing compatibility between nickel electrode and dielectric material**
- **These capacitors appear to be “bulletproof”**

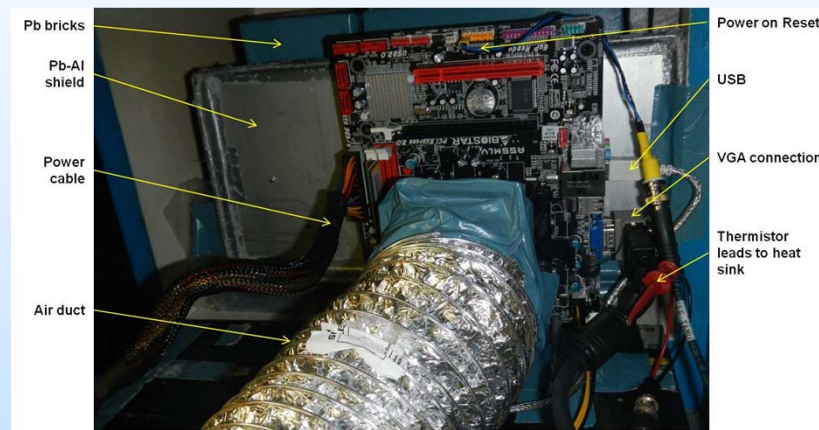


NEPP – Radiation Highlight (1)

- Total dose and dose rate evaluations were performed on a AMD state-of-the-art processor (fabrication: 32nm CMOS SOI technology from Dresden, Germany).
- U.S. ITAR criteria were used as a metric with the processor device tolerance exceeding these levels.



AMD A4-3300 series microprocessor



- Total dose results: **NO processor** failures observed (1,4 and 17 Mrad(Si), respectively). 17 is NOT a typo.
 - Failures observed on peripheral devices on motherboard as low as 1.1 krad(Si)
- Dose rate: no latchup observed. Upset observed on processor above ITAR levels. Motherboard peripherals (graphics) upset at levels below ITAR.



NEPP – Radiation Highlight (2)

- Initial radiation testing of 4th generation iPad™ - a test to simulate radiation exposure for true 100% COTS systems (i.e., very limited knowledge of electronics)

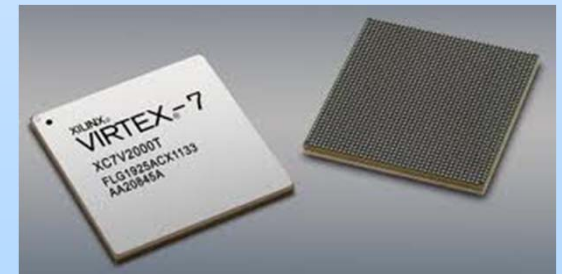


- Preliminary total dose testing performed on devices in standby mode and “on” followed by a suite of “app” tests for video, audio, GPS, etc...
 - Initial failures between 2 and 8 krad(Si) on battery charging circuitry
 - Display image degrades until unusable at ~ 10 krad(Si)
 - Processor appears to be fully functional at these low TID levels
- Proves the adage that COTS will have a wide range of radiation failure levels depending on technology and function

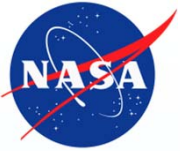


NEPP Task Focuses – FY13

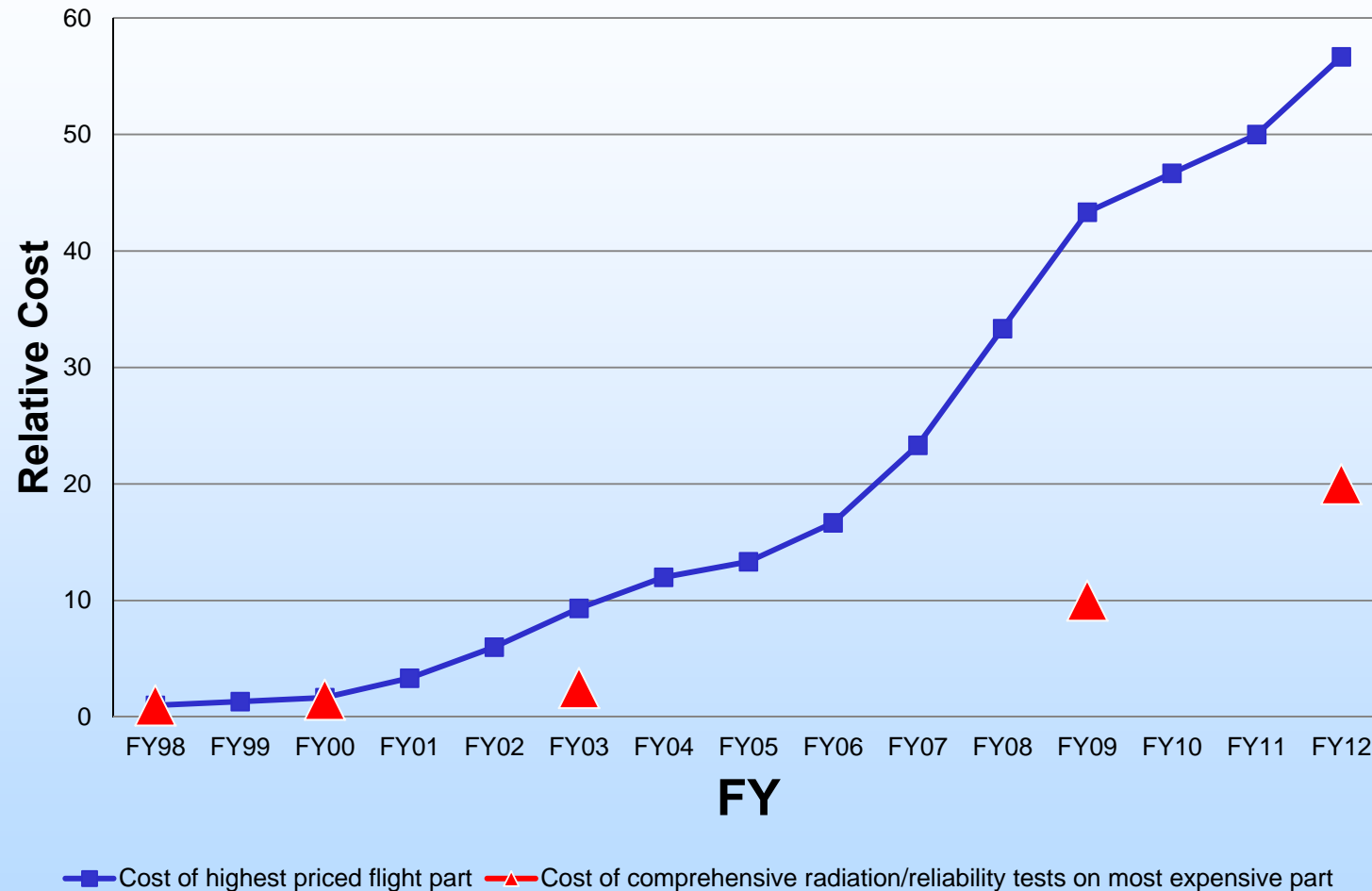
- **Goals: Develop guidelines for qualification and radiation testing**
 - Class Y Qualification (non-hermetic area array)
 - Flash Memory Qualification (reliability)
 - Flash Memory Testing (radiation) – in final review
 - Solid State Recorder (radiation) – in final review
 - DDR-class Memory (reliability)
- **Evaluate state-of-the-art commercial electronics (reliability, radiation)**
 - Memories, FPGAs, SOC Processors
 - Xilinx Virtex-7
 - Sub-32nm CMOS
 - Ipad™
 - BME Capacitors



Courtesy eetimes.com



Estimated Test/Parts Costs Normalized to FY98



Bottom line:

Test costs have risen significantly, unfortunately NEPP budget hasn't!

To be presented by Kenneth A. LaBel and Michael J. Sampson at 16602-13 - European Space Components Conference ESCCON 2013, Noordwijk, NL, March 12-14, 2013, and published on <http://nepp.nasa.gov/>.



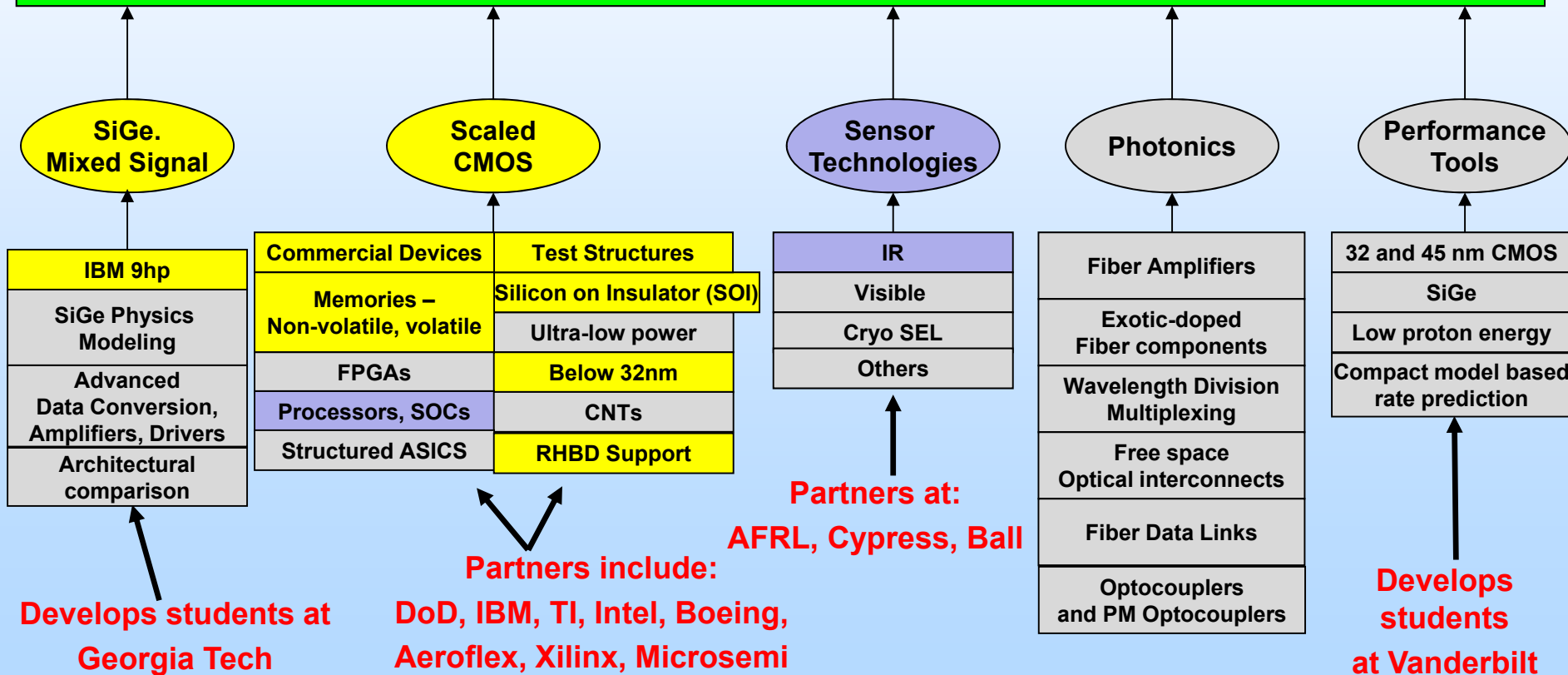
Sample NEPP Areas – Radiation Effects

Core Areas are Bubbles;

Boxes underneath are variable tasks in each core

Legend	
DoD and NASA funded	
NASA-only funded	
Unfunded in FY13	

NEPP Research Categories – Active Electronics (1 of 2)





Budget Challenges for FY13

- **The NEPP Program had a significant budget cut in FY13**
- **Reduction in efforts from FY12:**
 - **Areas unfunded or very limited in FY13 include**
 - **Photonics**
 - **Sensors/imagers**
 - **Mixed signal electronics**
 - **Commercial systems**
 - **University grants (research)**
 - **Fewer technology evaluations/tests**
 - **Commodities expertise at risk**
 - **Travel reduction impacts number of audits and meetings supported**



Summary

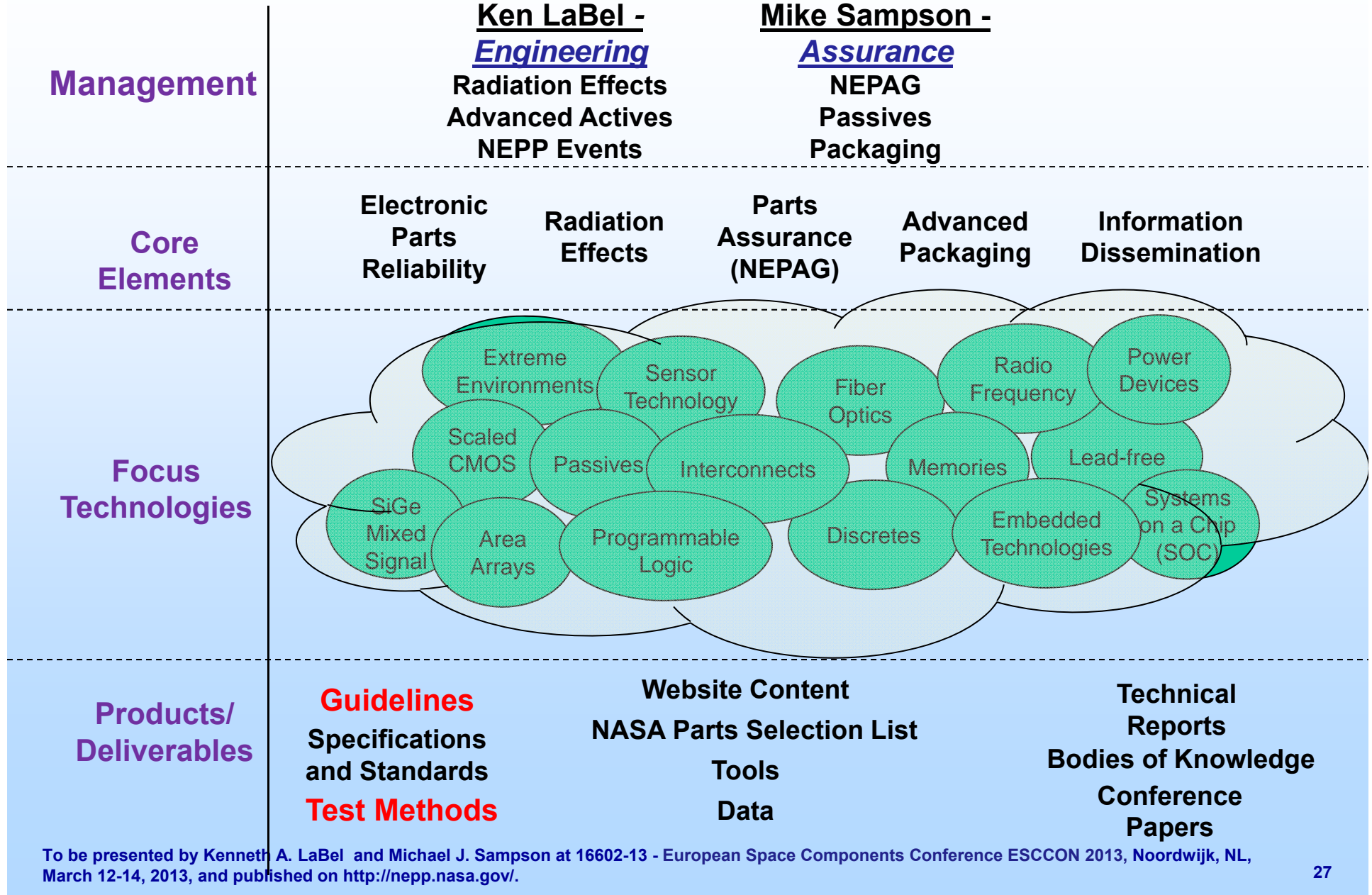
- NEPP is an agency-wide program that endeavors to provide added-value to the greater aerospace community.
 - Always looking at the big picture (widest potential space use of evaluated technologies),
 - Never forgetting our partners, and,
 - Attempting to do **“less with less”** (rising test costs versus NEPP budget reduction).
- We invite your feedback and collaboration and invite you to visit our website (<http://nepp.nasa.gov>) and join us at our annual meeting in June at NASA/GSFC or via the web.
- Questions?



Backups



The NEPP Program in a Nutshell

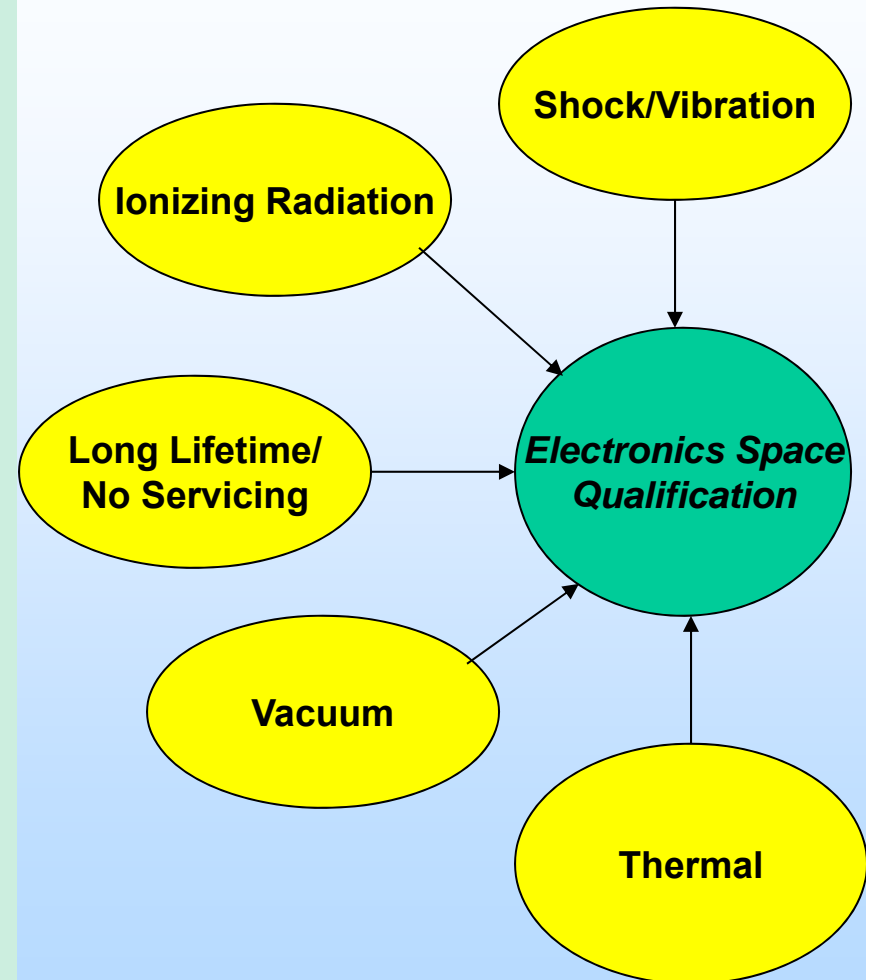




Qualifying Electronic Technologies

NEPP Perspective

- Electronics in space face hazards significantly beyond the terrestrial/commercial environment
- *Qualification requires repeatable and statistically significant testing over relevant environments to ensure mission success*
- NEPP provides the basis for understanding the “how to” for electronics qualification
- Is this needed for commercial devices?
 - Previous independent review/testing has repeatedly shown discrepancies between industry claims versus independent test results that impact reliable usage in space





FY12 NEPP Technology Efforts – Part 1

Radiation Hardness Assurance (RHA) and Guidelines

Low proton energy SEE test guide –
Jonathan Pellish, NASA/GSFC

Ultra-ELDRS and ELDRS on Discretes –
Dakai Chen, NASA/GSFC

IR Array Lessons Learned – Cheryl Marshall, NASA/GSFC
FPGA Standard SEE Test Guide –
Melanie Berg, MEI Technologies – NASA/GSFC

Flash Memory Qualification Guide - Doug Sheldon, JPL
NVM Standard Radiation Test Guide –
Tim Oldham, Dell – NASA/GSFC
NVM Combined Radiation and Reliability Effects –
Tim Oldham, Dell – NASA/GSFC
DDR2 Combined Radiation and Reliability Effects -
Ray Ladbury, NASA/GSFC
Updated Solid State Recorder Guidelines –
Ray Ladbury, NASA/GSFC
Correlation of LASER to Heavy Ion Millibeam with FLASH
Memories - Tim Oldham, Dell – NASA/GSFC

SEE Test Planning Guide – Ken LaBel, NASA/GSFC

Hydrogen and ELDRS – Philippe Adell, JPL

Devices

FPGA – Xilinx Virtex 5QV (SIRF) Independent SEE Testing -
Melanie Berg, MEI Technologies – NASA/GSFC
FPGA – Commercial Virtex 5 SEE –
Melanie Berg, MEI Technologies – NASA/GSFC
FPGA - Microsemi RTAX4000DSP SEE and ProASIC TID/SEE
- Melanie Berg, MEI Technologies – NASA/GSFC

FPGA – Microsemi ProASIC Reliability – Doug Sheldon, JPL
Class Y (non-hermetic area array packaged device
qualification) and related tests (Xilinx and Aeroflex
packages/devices) – Doug Sheldon, JPL
FLASH Memory Radiation Effects – Tim Oldham, Dell –
NASA/GSFC and Farohk Irom, JPL
Alternate NVM – MRAM/FRAM Reliability –
Jason Heidecker, JPL
DDR2/3 Radiation Effects and Combined Effects –
Ray Ladbury, NASA/GSFC

DDR2/3 Reliability – Steve Guertin, JPL
Newly Developed Si Power MOSFETs – Leif Scheick, JPL
and Jean Marie Lauenstein, NASA/GSFC
System on a Chip (SOC) Radiation Testing –
Steve Guertin, JPL
Newly Developed POLs Radiation and Reliability –
Dakai Chen, NASA/GSFC and Philippe Adell, JPL



FY12 NEPP Technology Efforts – Part 2

CMOS Technology

IBM Technology and Radiation– Jonathan Pellish,
NASA/GSFC w/ IBM, SNL, and NRL

INTEL Technology and Radiation (22nm FinFET processor –
TID/Dose Rate) –

Ken LaBel, NASA/GSFC w/INTEL, NAVSEA Crane

Tower Jazz Radiation Testing – Jonathan Pellish, NASA/GSFC
and Melanie Berg, MEI – NASA/GSFC

Lyric Semiconductor Radiation –
Jonathan Pellish, NASA/GSFC

Complex CMOS Device SEE Modeling –

Vanderbilt University and Melanie Berg, NASA/GSFC

Physics-Based Modeling for SEE - Vanderbilt University

CMOS Radiation Testing TBD Others: TI, ON, Cypress, STM

III-V, Widebandgap, and RF

90nm SiGe Radiation Effects (IBM 9hp) – Georgia Tech and
Paul Marshall, NASA/GSFC – Consultant

SiC and GaN Power Device Radiation Testing –
Megan Casey, NASA/GSFC and Leif Scheick, JPL
RF Device Screening Practices (Reliability) –
Mark White, JPL

SiC and GaN Power Device NASA Working Group –
Leif Scheick

SiC and GaN Reliability Testing –
Richard Patterson, NASA-GRC

Miscellaneous SiGe Device Radiation Testing – NASA/GSFC
TBD GaAs HEXFET Radiation – NASA/GSFC:
We are tracking ESA research and determining
applicability



FY12 NEPP Technology Efforts – Part 3

Qualification and Packaging

Class Y related packaging tests CCGA/PBGA, underfill, etc... –
Doug Sheldon, JPL (w/many others)

Cryogenic Connector Failure Analysis – NASA/JPL
Body of Knowledge (BOK) documents on multiple
packaging-related areas (TSV, 3D packages, X-ray and
Workmanship, etc) – NASA/JPL
BME, Tantallum, and Polymer Capacitor
Reliability/Screening – NASA/GSFC
DC-DC Converter NASA Working Group – John Pandolf,
NASA/LaRC
NASA Connectors Working Group – Carlton Faller, NASA-JSC

Other

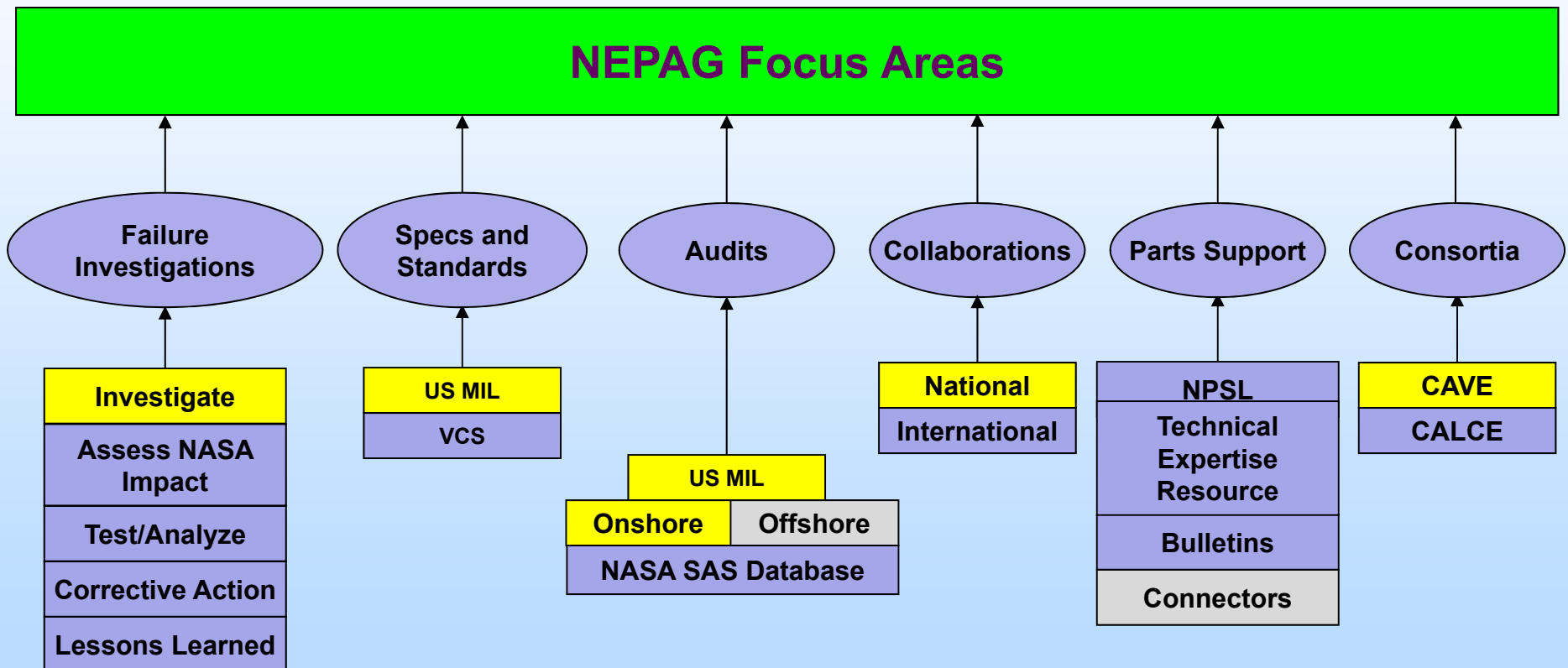
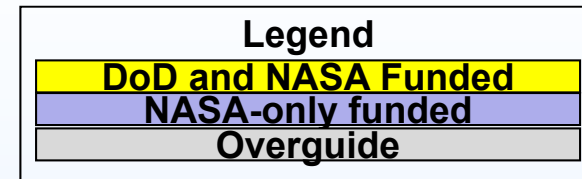
Infrared focal plane array lessons learned –
Cheryl Marshall, NASA/GSFC
Development of SEGR Power MOSFET predictive technique
– Jean Marie Lauenstein, NASA/GSFC
SEE Failures and Results Related to DC-DC Converter
Design– Robert Gigliuto, MEI Technologies – NASA/GSFC
Point of Load NASA Working Group –
Dakai Chen, NASA/GSFC
Optoelectronic Connectors and Transceivers –
Melanie Ott, NASA/GSFC



NASA Electronic Parts Assurance Group (NEPAG)

Core Areas are Bubbles;

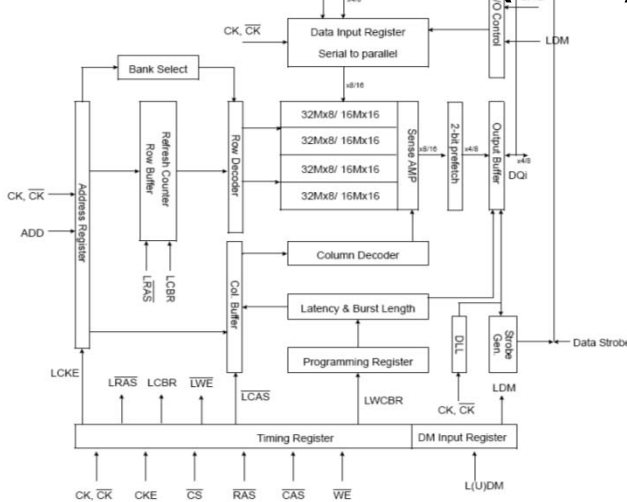
Boxes underneath are elements in each core





Disclaimer: Statistics and “Radiation Qualification”

Device Under Test (DUT)



Commercial 1 Gb SDRAM

- 68 operating modes
- can operate to >500 MHz
- Vdd 2.5V external, 1.25V internal

Single Event Effect Test Matrix

full generic testing

Amount	Item
3	Number of Samples
68	Modes of Operation
4	Test Patterns
3	Frequencies of Operation
3	Power Supply Voltages
3	Ions
3	Hours per Ion per Test Matrix Point

66096

Hours

2754

Days

7.54

Years

Doesn't include temperature variations!!!

Devices/technology are more complex: testing is as well

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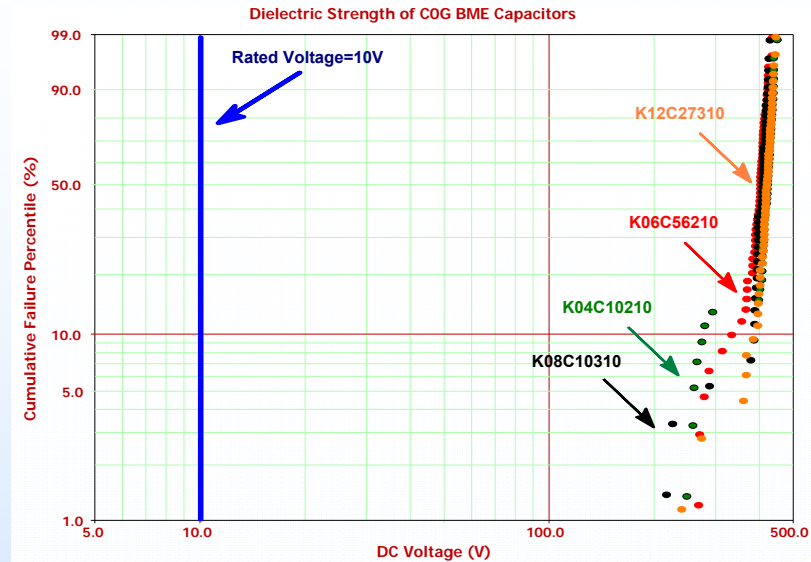
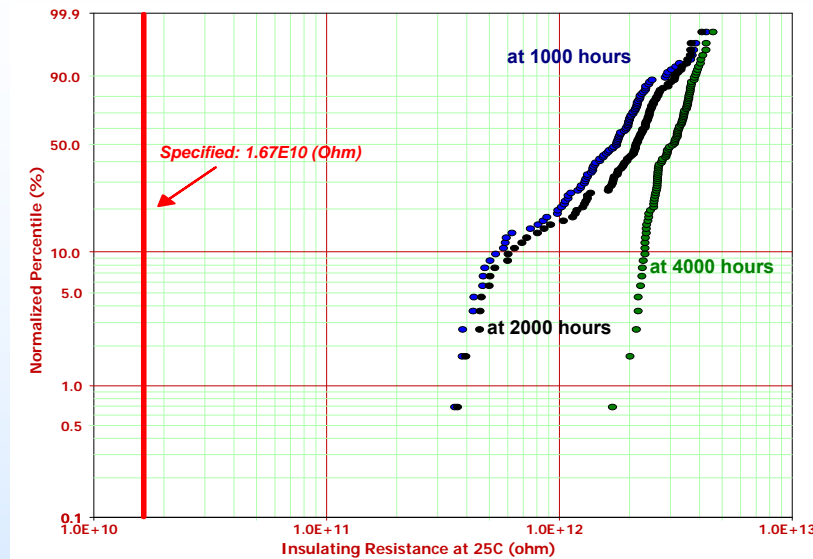
High Capacitance Per Volume

EIA Chip Size	0201	0402	0603	0805	1206	1210
Max Cap for BME C0G (pF, 25V)	100 pF	2,200	15,000	47,000	100,000	220,000
Max Cap per PME X7R (pF, 50V)	N/A	3,900	22,000	82,000	220,000	390,000

- Chart compares capacitance between commercially available BME C0G at 25V and PME X7R at 50V
- The PME data are from GSFC Document S-311-P-829C (1/2010) which allows the use of PME capacitors with small chip size and lower rated voltage. However, 50% voltage de-rating is still applicable.
- The BME C0G MLCCs can reach >50% capacitance that a same chip size PME X7R can provide (after de-rating)



Excellent Reliability Performance



- A 4000-hour life test did not reveal any failures
- Insulating resistance was more than 10 times greater than MIL-PRF-123 requirement, both at 25°C and at 125°C
- No dielectric wearout failures were generated when the capacitors were tested under accelerated stress conditions as high as 175°C and 500V for a group of 50 C0G BME capacitors
- DC breakdown voltage is at least 20 times greater than the rated voltage



Summary

This low-cost, commercially available BME capacitor with a CaZrO_3 -based COG dielectric is one of a few existing commercial products that can significantly exceed the NASA requirements for high-reliability space applications and that can be directly recommended for use in NASA flight projects!